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Analysis of Non-isolated Soft Switching DC-DC Buck Converter

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***Abstract* - A novel zero-voltage switching (ZVS) step-down converter with a tapped inductor is proposed in this paper. Tapped inductor provides better power density as compared to isolation buck converter. With a simple structure, the tapped-inductor buck converter shows promise for extending the duty cycle. This converter is cost effective and attractive for high performance. Furthermore, with the replacement of transformer by tapped inductor, its efficiency may be maximized for low power application and power quality is improved as low harmonics at input as well as output. The peak current of the main switch is reduced by tapped inductor operation, thus the conduction loss and switching loss levels of the main switch are lowered. Consequently, this tapped inductor scheme alleviates the severe power stress and enhances device utilization. This soft-switching buck converter is suitable for extremely low step-down ratio applications. The principle of the proposed scheme, analysis of the operation, and design guidelines are included. Finally, the experimental result of the 10W prototype DC/DC converter is given for hardware verification.**

***Keywords*: ZVS, Tapped inductor, DC/DC, power quality.**

I. INTRODUCTION

The latest microprocessors to emerge from Intel, Motorola, and others are forcing fundamental changes in the power supplies for desktop and portable computers. Not only does the µPs demand lower and more precise supply voltages, but their main clocks also exhibit start/stop operation that causes ultra-fast load transients. As a result, the relatively simple 5V/12V supply has been transformed into a system with five or more outputs featuring unprecedented accuracy and 50A/µs load-current slew rates This extreme conversion ratio causes the duty cycle to also be extremely high or low. In buck converter case, the operation with small duty cycle influences the performance of both steady state and transient state. This small duty cycle degrades the power efficiency and the transient dynamics with the effect of the minimum pulse width of MOSFET gate drivers. In order to remove these problems, the increase of duty cycle is introduced by employment of a transformer. The utilization of the transformer has some benefits such that the duty cycle of the converter can be adjusted to a desirable value in order to prevent the extreme duty cycle at the high step-up or low step-down ratios through the proper selection of the winding ratio. This extra degree of freedom enables the switches to avoid high-peak current, and contributes to a reduction of the switching loss and conduction loss of the converters. However, the isolation type converters keep a low efficiency level due to the transformer loss itself and the bulky size with an increasing number of extra components to reset the transformer. To obtain both the extreme voltage conversion and high efficiency, the application of a tapped inductor (TI) has been considered as one of the effective alternatives in previous researches [1]–[3] since the tapped inductor operates as an autotransformer without the need of a reset circuit. Furthermore, an autotransformer employment utilizes less copper than an isolation-type transformer. However, there are still some difficulties in applying the TI to converters because the ringing between the leakage inductance of the inductor and the parasitic capacitances in switches leads to higher voltage

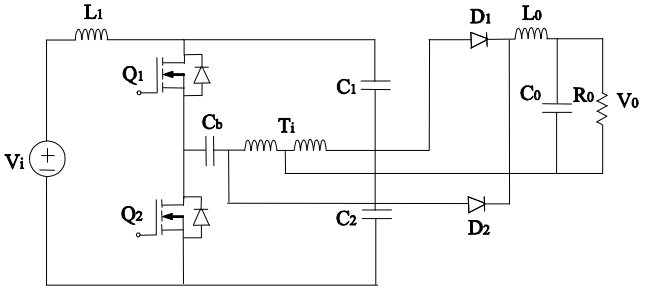

Figure 1. The proposed converter

stress across switching devices and more EMI. These problems prevent the tapped inductor employment from being the optimal solution for extreme conversion ratio applications.

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In order to remove these problems, it is necessary to apply the soft-switching technique to TI applications [4]-[6].

In this paper, a new zero-voltage switching (ZVS) buck converter with the tapped inductor is proposed. The proposed converter improves the performance. The clamp capacitor and the tapped inductor do soft switching operation, so the stresses across the switch are reduced to increase the efficiency at the low power output. The improvement includes another soft switching technique by two capacitors C_1 and C_2 which gives another design freedom for the selection of the turn-ratios and enables the optimal design of the TI so that both the switching loss and the conduction loss may be minimized. This soft-switching converter is suitable for applications with wide input ranges leading to extremely low step-down ratios. The principle of operation and the design process will provide elaborately in the following sections of the paper. The results of the 10-W prototype dc-dc converter will be given for hardware verification.

The paper is divided into sections. In Section II, features of topology are presented. Section III presents detail analysis of operation principles and section V describes design process. In Section V simulation results and experimental results are compared and verified with theoretical concepts. At the last section list of references are given.

II. TOPOLOGY ADOPTED

The new soft switching proposed topology is shown in the fig.1. This topology is basically designed to improve its efficiency with reduced switching and conduction losses. Tapped inductor is used instead transformer, for energy transferring from higher side to lower side. Two MOSFET switches are used to make switching operation faster comparison to IGBT switches. Dead time is controlled by blocking capacitor C_b, to avoid voltage and current stress on switches which is occurred due to resonance between capacitors C_b, C_1 and C_2 and the inductance of tapped inductor. The sudden flow of current during transition periods is controlled by using an inductor in series with the supply.

On the secondary side rectifier circuit is used to maintain the output current in unidirectional. Two diode simultaneously cannot conduct. The performance of the propose converter is compared with the conventional converter and with previously proposed converter.

III. CONVERTER FEATURES

1. Ripple free input current and output currents yielding better power quality.
2. Suitable for wide load range.
3. Switches are turned on under ZVS due to clamping capacitors and turned off under ZCS due to tapped inductor, which results optimum power utilizations.
4. Economically effective.
5. Improved power density.
6. High efficiency at low power of 10 W.
7. Switching frequency is 1 MHz
8. Peak current is controlled by tapped inductor, so switching and conduction losses are minimized

IV. OPERATION PRINCIPLES

The following assumptions are made to simplify the circuit operations

- capacitance of the blocking capacitor is taken more as compared to other two capacitors used in this circuit;
- capacitances of other two capacitors are taken as same value;
- to make input current ripple free, inductance of tapped inductor L_{Ti} is designed properly;
- current flowing through transformer is continuous;

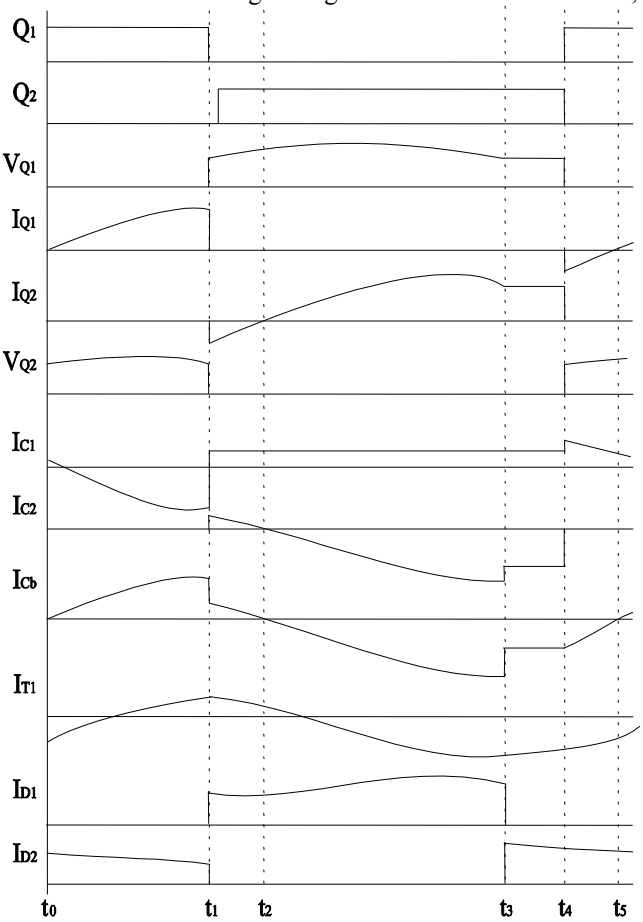


Figure 2. Key Waveforms of proposed converter.

The proposed converter scheme is shown in Fig.1. The circuit scheme includes two MOSFET switches Q1 and Q2. Two clamp capacitors C1 andC2. The tapped inductor T_i denotes the combination of the the fixed and variable inductance. The proposed dc-dc converter designed through AC link as energy

transfer devices. In steady-state, the proposed converter has five operation states during one switching cycle. The key waveforms and the equivalent circuits of each operation state are shown in Fig.2 and Fig.3, respectively.

Mode 1 (t_0-t_1) : At t = t_0, MOSFET Q1 is turned on by providing proper gate pulse. Now current starts to flow through the trapped inductor. The diode D_2 is forward biased, while voltage drop across tapped inductor will turn off diode D_1. Resonant condition occurs by the inductance L_{Ti} and equivalent capacitance of C_b and C1. But the resonant period is less, so high peak current and voltage stresses can not appear across the switch Q_2.

The switch is turned on under ZVS due to capacitor C_1, and turned off under ZCS due to tapped inductor inductance L_{Ti}. This mode ends when capacitor C_1 completely charges to its peak value. At this moment input
current completely flow through capacitor C_1, providing current through the switch equal to zero. So at this moment switch Q_2 can be turned off under ZCS. At end of this mode, Cb charged up to C_{b1} opposite to that of its initial value.

Mode 2 (t_1-t_2) : At t = t_1, stored energy of inductor is forced the body diode of switch Q_2 and rectifier diode D_1 starts to conduct. The tapped inductor discharged its stored energy through C_2-Dq_2-Cb and some part of energy transferred to load. Resonance occur between inductance L_{Ti} and capacitors C_2 and C_b. However, the resonant period is not more than the dead time. Dead time is controlled by capacitor C_b. The mode ends at t_2, when current through Cb becomes zero i.e. this blocking capacitor is charged upto its maximum value.

Mode 3 (t_2-t_3) : This mode starts with switch Q_2 turned-on under ZVS. This mode will come to end when the part of tapped inductor connected to load, has completely discharge its energy to load.. At end of this mode, Cb charged up to C_{b2} opposite to that of its initial value.

Mode 4 (t_3-t_4) : So at t = t_3, the rectifier diode D_1 will be off and from the other part of the tapped inductor energy will transfer to load through D_2. The tapped inductor forced the diode D2 conduct under ZVS and the diode D_1 stops conducting any more, which ensure the continuous flow of current at the output. At the end of the mode the body diode of the switch Q_1 is turned on due to the energy transferring property of inductor in the same direction in which it get charged.

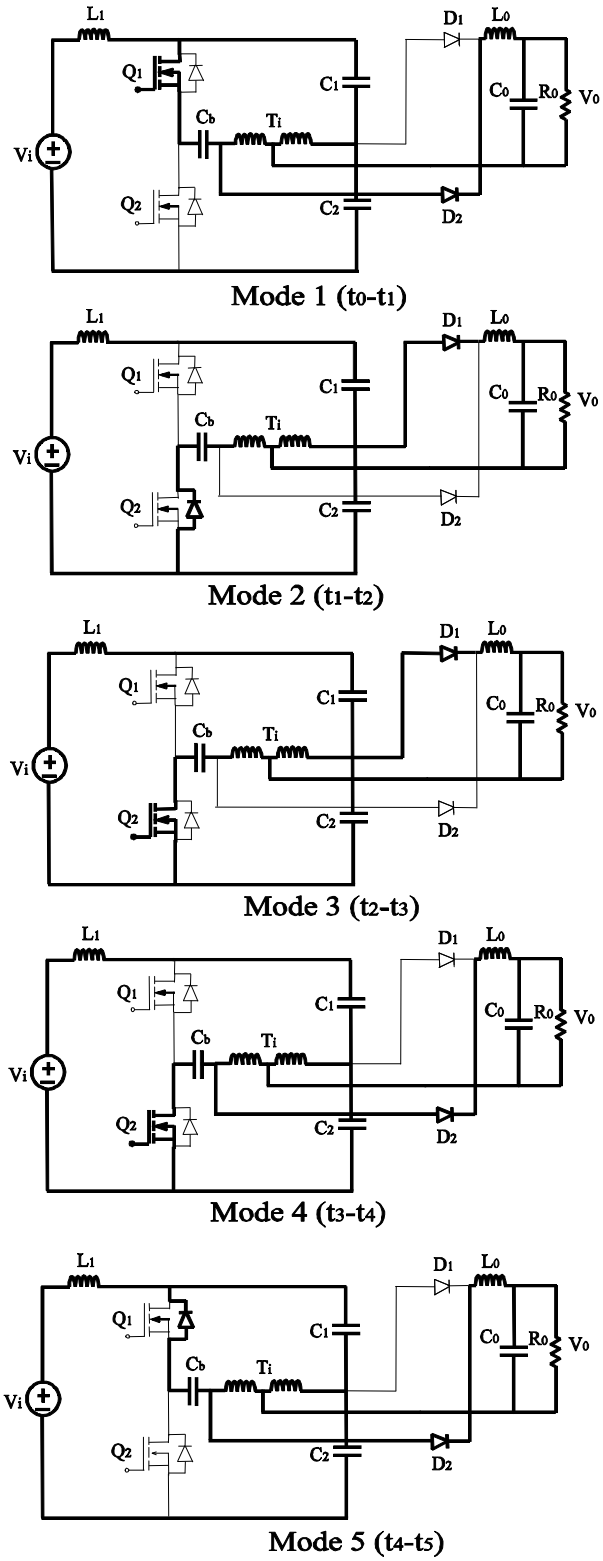


Figure 3. Modes of Operations.

Mode 5 (t_4-t_5) : Then the rectified diode D_2 will start to conduct. The body diode of the switch Q_1 is turned on due to the energy transferring property of inductor in the same direction in which it get charged.

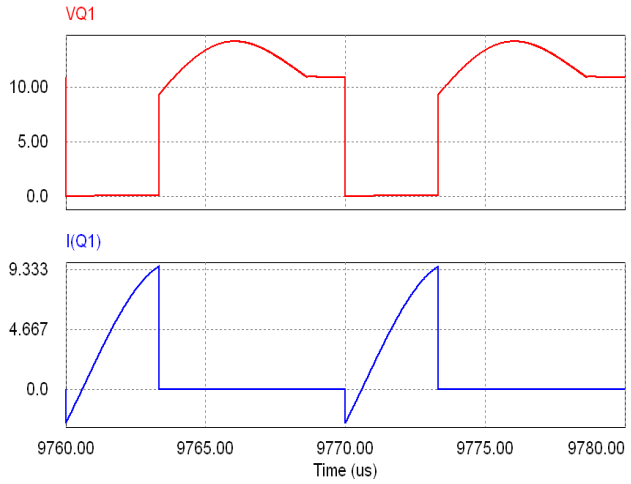


Fig. 4(a) Voltage and current waveforms of switch Q_1. Voltage is in Volts and current is in Amperes.

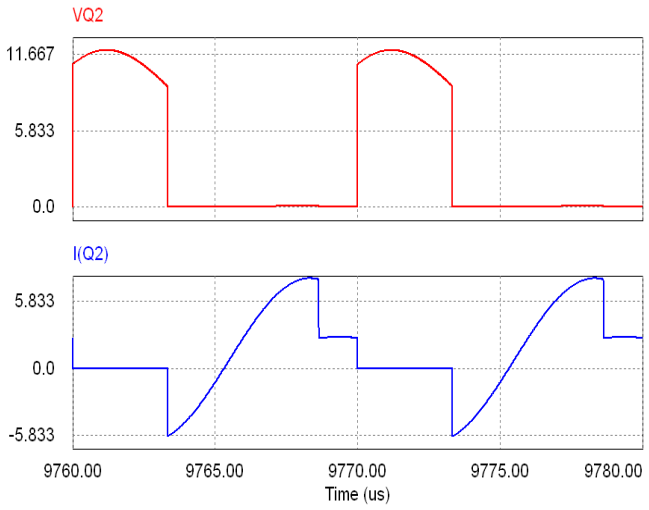


Fig. 4(b) Voltage and current waveforms of switch Q_2. Voltage is in Volts and current is in Amperes.

V. LOSS ANALYSIS

The majority of the power lost in power conversion is due to losses in the Power MOSFET switches. The loss profiles for the high side and low side Power MOSFET are quite different. The main parameters that impact on the high side losses are given by C_{iss} and Q_G. Instead the main parameter that impacts on the low-side switch is give by the $R_{DS(ON)}$. These low output voltage converters have low duty cycles, concentrating the majority of the conduction loss in the low-side MOSFET.

The power loss in any MOSFET is the combination of the switching losses and the MOSFET's conduction losses.

$$P_{MOSFET} = P_{SW} + P_{COND}$$

S_1 bears the brunt of the switching losses, since it swings the full input voltage with full current
through it. In low duty cycle converters (for example: $12V_i$ to $3.3V_o$) switching losses tend to dominate.

Calculating high-side conduction loss is straightforward as the conduction losses are just the I^2R losses in the MOSFET times the MOSFET's duty cycle:

$$P_{COND} = I_o^{\,2} \cdot R_{DS(ON)} \cdot \frac{V_o}{V_i}$$

$P_{COND} = 0.15$ watt.
where $R_{DS(ON)}$ is at the maximum operating MOSFET junction temperature.
During $t_{00'}$ and $t_{0'1'}$, the MOSFET is just fully enhancing the channel to obtain its rated $R_{DS(ON)}$ at a rated V_{GS}. The losses during this time are very small compared to t_0 and $t_{1'}$, when the MOSFET is simultaneously sustaining voltage and conducting current, so we can safely ignore them in the analysis. The switching loss for any given edge is just the power that occurs in each switching interval, multipied by the duty cycle of the switching interval:

$$P_{SW} = \left(\frac{V_i \cdot I_o}{2}\right)\left(t_{00'} + t_{0'1'}\right)\left(f_{SW}\right)$$

Now, all we need to determine are t_{01} and $t_{11'}$. Each period is determined by how long it takes the gate driver to deliver all of the charge required to move through that time period:

$$t_x = \frac{Q_{G(x)}}{I_{Driver}}$$

Most of the switching interval is spent in t3, which occurs at a voltage we refer to as "VSP", or the "switching point" voltage. While this is not specifically specified in most MOSFET datasheets, it can be read from the Gate Charge graph, or approximated using the following equation:

$$V_{SP} \approx V_{Th} + \frac{I_o}{G_M}$$

where G_M is the MOSFET's transconductance, and V_{Th} is its typical gate threshold voltage. With V_{SP} known, the gate current can be determined by Ohm's law:

$$I_{Driver(L-H)} = \frac{V_{DD} - V_{SP}}{R_{Driver(pull-up)} + R_{Gate}}$$

$$I_{Driver(H-L)} = \frac{V_{DD} - V_{SP}}{R_{Driver(pull-down)} + R_{Gate}}$$

The rising time (L-H) and falling times (H-L) are treated separately, since I_{Driver} can be different for each edge. The V_{GS} excursion during $t_{00'}$ is from V_{Th} to V_{SP}. Approximating this as V_{SP} simplifies the calculation considerably and introduces no significant error. This approximation also allows us to use the $Q_{G(SW)}$ term to represent the gate charge for a MOSFET to move through the switching interval. A few MOSFET manufacturers specify $Q_{G(SW)}$ on their data sheets. For those that don't, it can be approximated by:

$$Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2}$$

so the switching times therefore are:

$$t_{S(L-H)} = \frac{Q_{G(SW)}}{I_{Driver(L-H)}}$$

$$t_{S(H-L)} = \frac{Q_{G(SW)}}{I_{Driver(H-L)}}$$

(43)

The switching loss discussion above can be summarized as:

$$P_{SW} = \left(\frac{V_i \cdot I_o}{2}\right)\left(f_{SW}\right)\left(t_{S(L-H)} + t_{S(H-L)}\right)$$

P_{SW} = 0.3 watt.

Similarly switching loss for main switch is found out as 0.2 watt and conduction loss is equal to 0.28 watt.

There are several additional losses that are typically much smaller than the aforementioned losses. Although their proportional impact on efficiency is low, they can be significant because of where the dissipation occurs (for example, driver dissipation). They are listed in order of importance:

1. The power to charge the gate:

$$P_{GATE} = Q_G \times V_{DD} \times f_{SW}$$

2. The power to charge the MOSFET's output capacitance:

$$P_{COSS} \approx \frac{C_{OSS} \cdot V_i^2 \cdot f_{SW}}{2}$$

where C_{OSS} is the MOSFETs output capacitance, (C_{DS} +C_{DG}).

3. Reverse recover power for S_2's body diode:

$$P_{SRR} = Q_{RR} \cdot V_i \cdot f_{SW}$$

where Q_{RR} is the body diode's reverse recovery charge.

All the above three losses are in mwatt.

Switching losses are negligible, since S_2 switches on and off with only a diode drop across it, however for completeness we will include the analysis. Conduction losses for S_2 are given by:

$$P_{COND} = (1-D) \times I_o^2 \times R_{DS(ON)}$$

P_{COND} = 0.56 watt.

Where D is the duty cycle for the converter.

Low-side switching losses for each edge can be calculated in a similar fashion to high-side switching losses:

$$P_{SW(LS)} = \left(t_{00'} \cdot V_F + t_{0'1'} \cdot \frac{V_F + I_o \cdot 1.1 \cdot R_{DS(ON)}}{2}\right) I_o \cdot f_{SW}$$

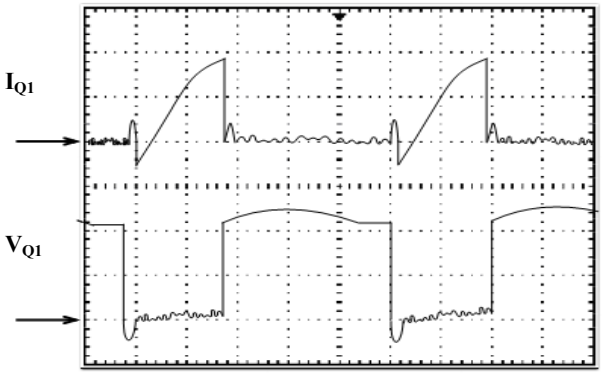
P_{SW} = 0.01 watt.

but instead of V_i we use V_F , the schottky diode drop (approximated as 0.6V) in the equation. Also, there is almost no Miller effect for the low-side MOSFET, since V_{DS} is increasing (becoming less negative) as we turn the device on, the gate driver does not have to supply charge to C_{GD}.

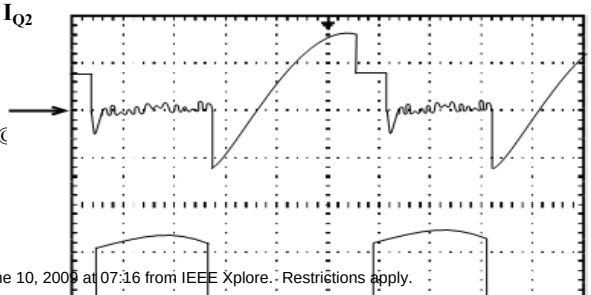
V. SIMULATION AND EXPERIMENTAL RESULTS

To demonstrate the validity and performance of the proposed converter, it was tested experimentally and was simulated. The 10 W 12V / 3.3V converter is chosen for the investigations. The proposed converter parameters are Ro = 0.8Ω, L_1 = 10μH, $C_1 = C_2 = C_b$ = 3 μF, L_{Ti} = 3μH, switching frequency = 1MHz..

The simulated converter delivers a load of 10W with efficiency of 95.2 %. The simulated waveforms shown in the fig. 4(a) and 4(b), are obtained by using PSIM 6.0. From the simulated waveform, it can be seen that both switches are turned on and turned off ZVS and ZCS. The experimental oscillograms are shown in fig. 5(a) and 5(b). Efficiency vs output power is shown in the figure in ZVS and without ZVS.



5(a)



V_{Q2}

5(b)

Fig. 5(a) Voltage and current waveforms of switch Q_1. Voltage is in 5 V/div and current is in 5 A/div. The X- axis is time axis in 5 microsecond/div. Fig. 5(b) Voltage and current waveforms of switch Q_2. Voltage is in 5V/div and current is in 4A/div. The X- axis is time axis in 5 microsecond/div.

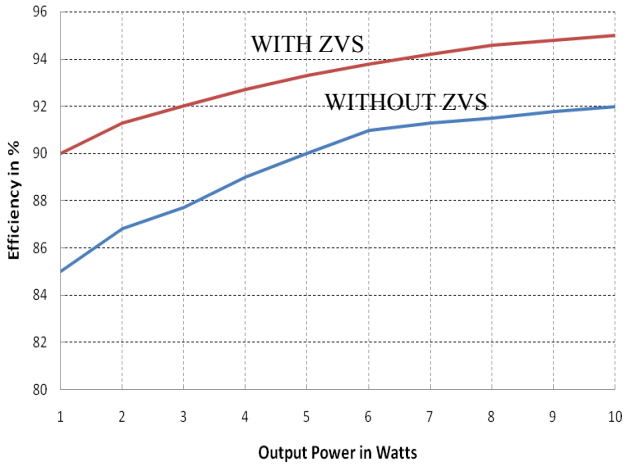


Fig. 6 Efficiency vs output power

VI. CONCLUSIONS

The proposed converter designed has several features and advantages: high efficiency, high power density, least size due to smaller components used, cheaper and faster switching frequency of 1 MHz.

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