A Hardware Implementation of Modified MAC Behaviour for Multimedia Traffic in Wireless LAN for QoS

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Abstract

A Modified MAC (Quality of Service Manager) VHDL implementation over wireless LAN is presented, which integrates wireless access block and user interfaces. Real-time application of multimedia system over wireless network can be easily implemented with a low cost and less complexity. To support priority issues of real-time traffic, dual queueing strategy is adopted. It also provides WLAN-PHY which supports high speed data access up to the IEEE 802.11 PHY standards. The VHDL hardware implementation of modified MAC is dedicated for the specified kind of real-time multimedia traffic.

1. Introduction

Over the past a few years, several communication services using WLAN (Wireless Local Area Network) are increasing. The IEEE 802.11 defines the functionality of medium access control (MAC) layer and physical (PHY) layer specifications for WLAN [1] [2]. Most of the 802.11 devices implement the DCF only because of the contention-based channel access nature, which supports best-effort service without guaranteeing any QoS [1] [2] [3] [4]. A wireless multimedia LAN approach has described in [8], which uses DCF and shortened contention window for QoS. The emerging 802.11e MAC, which is an amendment of the existing 802.11 MAC, provides QoS for best effort, voice and video with different queues [3].

This paper describes a hardware implementation of the software upgrade-based approach as in [4], to provide QoS for real-time multimedia service. In this scheme it implements a Quality of Service Management (QoSM) with quality and besteffort quque (Q_q and BE_q) on top of the 802.11 MAC controller. Basically, the Q_p and BE_p packets are classified and enqueued into one of the two queues. Then after a strict priority policy is used to forward the packets from two queues in order to give a priority to quality (real-time multimedia) packets from Q_q, the BE_q queue is never served as long as the Q_q is non-empty.

The rest of the paper is organized as follows. Section 2 discusses the Hardware Implementation of QoS Management system and VHDL simulation. We conclude in Section 3 by discussing the future work and references are added.

2. Hardware Implementation of QoSM

A hardware implementation of the QoSM is described here. The QoSM hardware was design and simulated using VHDL. Introducing this section, it is worth making a point regarding the design flow of QoSM. It operates with first in first out memory with strict forwarding mechanism. Taking into consideration the constraints of the target application, VHDL implementation of each block as in [4], has to be developed. As pointed out the specified service architecture for multimedia applications require particular hardware.

It requires two memory modules with FIFO (first in first out/first come first serve) mechanism for two queues (Q_q and BE_q). The input to these two memory blocks is assigned after checking whether it comes from the upper half of the address range or from the lower half of the address range. It also checks the memory status whether it is full or empty, if memory full then dropping of packet happens.

2.1. Simulation of QoSM

The hardware implementation of the proposed model simulated using *Xilinx 9.1i* [5] with devices and design having Family- Spartan2, Device-XC2S15, Package- CS144, Source Type- HDL, Synthesis Tool- XST (VHDL/Verilog), Simulator-ISE Simulator (VHDL/Verilog), Language- VHDL. The simulation time is taken to be 1000ns. The network on a chip (NoC) has been described in [10] with asynchronous VLSI. Here we simulate the proposed module using VHDL with a synchronous data transfer from the memory modules.

Writing data to memory module takes input data and stores it. Reading of data is done with a FIFO manner. All these are working with the clock pulse. The status of the memory block can be checked with full or empty ports. The two instance of the memory

module is created for two queues (module 1 and module 2). The output of data from the memory is done by checking the status of the memory port full and empty, i.e. if the port empty having value 0 then the forwarding of data is done from memory module 1 otherwise forwarding of data is done from memory module 2. The hardware implementation is being done using VHDL [9] and its related RTL schematic, RTL schematic modules, test bench wave form and Technology schematic is generated as in shown in the Figure. 1, 2, 3 and 4 respectively. Figure. 1 shows the RTL schematic with the ports taken for simulation in VHDL.

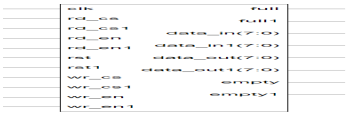

Figure1. RTL Schematic

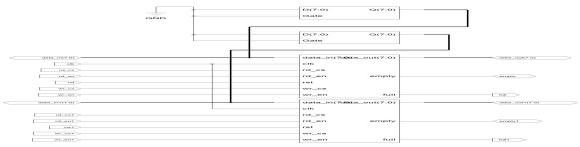

Figure2. Modules of RTL Schematic

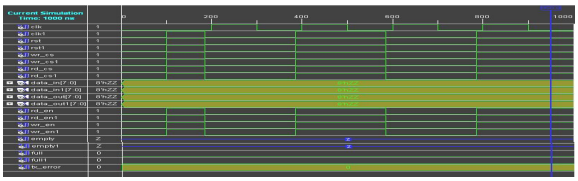

Figure3. Test Bench WaveForm

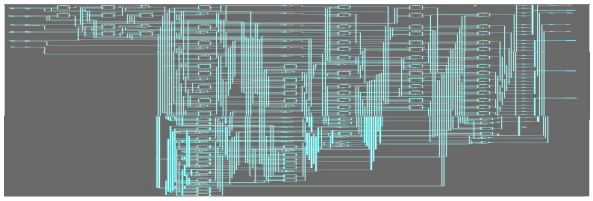

Figure4. Technology Schematic

Figure 2 shows the modular logic diagram of the RTL schematic, that how the input stream is recognized and assigned to the appropriate queue, output of the data from the memory is being done as per the status of the port empty and dropping of data can be found out by checking the status of the full port of memory module 1 and module 2 sends data out only when it found that port empty is high and encounters dropping of data when full1 is high. Test bench waveform generated from the VHDL simulation shown in Figure. 3 and 4 shows the Technology Schematic generated from the VHDL simulation. The hardware approach does not be overburden to CPU rather than it can able to perform its own task.

3. Conclusion

The implemented VHDL is intended for providing the real-time application system on wireless medium with less complexity and low cost. As it is capable to process on the chip so it will not use the CPU cycle. Using this hardware implementation can make the system for real time multimedia applications easily. As is a dedicated hardware for the specified purpose, so it'll not add any overhead to the software for processing the application.

4. References

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