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A novel current initialization scheme for parallel resonant dc link inverter

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In this paper a novel current initialization scheme is proposed for a parallel resonant dc link inverter. The method of current initialization is based on the state transition analysis of the system as a boundary-value problem. It is shown that, for a given load current, it is possible to force the dc link voltage to go to zero at a prescribed time by properly choosing the initial dc link current. This technique makes it possible to operate the resonant dc link inverter without any zero-crossing failure, which is the most important issue for satisfactory operation of such an inverter. The proposed current initialization technique is validated through digital computer simulation studies and practical implementation results.

1. Introduction

Resonant dc link inverters promise marked gains for adjustable speed drives, power supplies and active filtering applications. Among the various types of resonant link, the parallel resonant dc link is quite attractive for implementing zero voltage switching (ZVS) (Divan 1989). This is based on shunt resonance. This inverter is quite simple in the sense that it needs a minimum number of devices, it is easy to implement and requires simple control. This inverter, shown in figure 1 (*a*), requires an additional resonant inductor and a resonant capacitor compared with a regular pulse width modulated (PWM) inverter. The resonant circuit is connected between the dc source and the inverter so that the input voltage to the inverter oscillates between zero and slightly greater than twice the dc bus voltage. Figure 1(*b*) shows an approximate equivalent circuit during a resonant oscillation, assuming i_0 to be constant.

The advantages of this soft-switched inverter are well known. It reduces the dominant switching losses in inverter devices, allows higher switching frequencies at reasonably high power level and reduces noise and electromagnetic interference. Because of the minimal switching loss, the efficiency is high and cooling requirement is minimal. Additionally, the devices do not require any snubbers.

This simple topology, however, has a few drawbacks. These are higher device voltage stresses (when the output voltage is greater than twice the dc input voltage) and zero crossing failure unless the initial current in the resonant inductor is built-up properly. The voltage overshoot problem can be overcome by using an actively clamped parallel resonant dc link inverter (PRDCLI) (Divan and Skibinski 1989). It is possible to limit the voltage stresses of the inverter devices to 1.3–1.8 times the dc voltage. The actively clamped PRDCLI circuit also has a few disadvantages. The

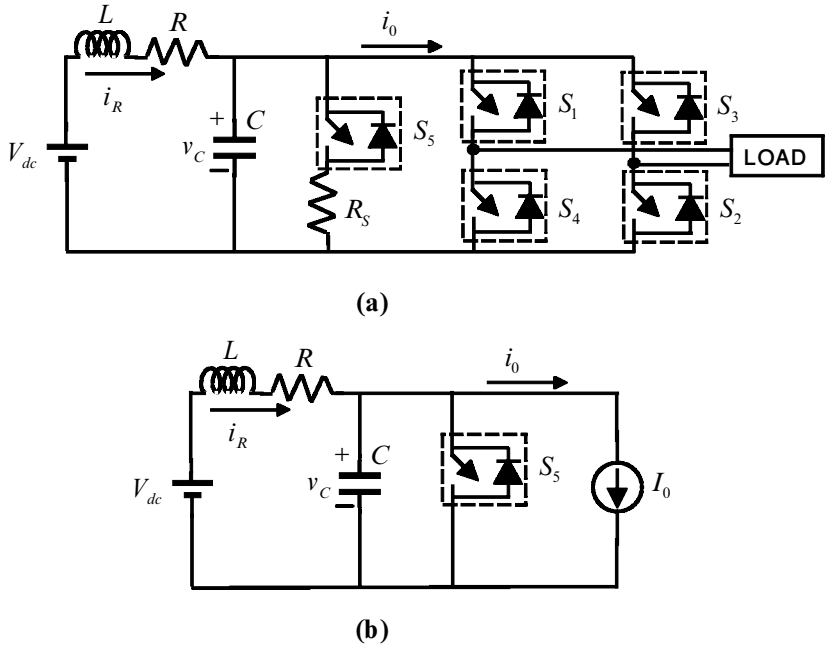
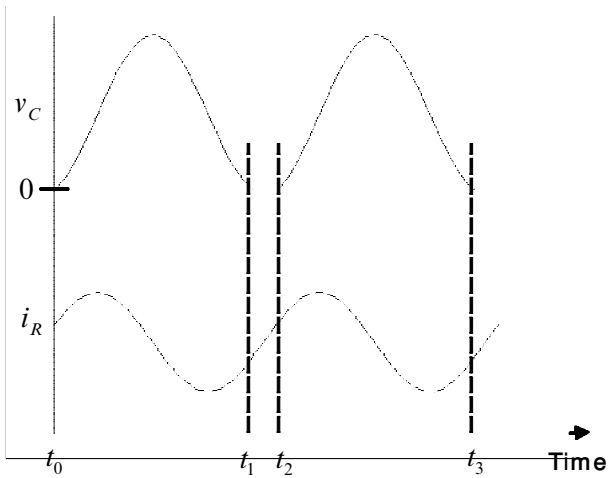


Figure 1. Single-phase parallel resonant dc link inverter: (*a*) schematic diagram; (*b*) approximate equivalent circuit.

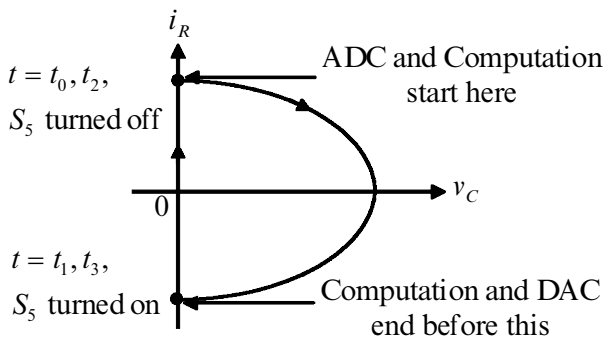
link frequency varies with variation in the dc link voltage; this shows up as large current jumps. This topology increases losses owing to introduction of the clamping circuit. The additional clamping device increases the complexity of the power circuit and the control circuit. Moreover, the control of the clamping device becomes extremely difficult at high frequencies.

In this paper the basic PRDCLI is considered. An important consideration for successful operation of the PRDCLI is that there should not be zero crossing failure. Zero crossing of the resonant link dc voltage is mandatory in every resonant cycle for successful operation of the inverter. Failure of the resonant link tends to occur because of the finite Q of the resonant circuit, where the capacitor voltage tends to build up in successive resonant cycles. Therefore, an appropriate initial current must be built up in the inverter which would then ensure a zero crossing of the voltage. This must be done in every resonant cycle. The build up of fixed initial inductor current was proposed to ensure zero crossing in every resonant cycle (Divan 1989). However, the initial current is a function of the inverter input current, which depends upon the load current of the inverter. In a practical circuit, the load current would fluctuate and hence the current i_0 can be bidirectional. Thus, using a fixed initial inductor current concept would not ensure zero crossing in every resonant cycle unless this current were designed on the worst-case basis. However, this approach would aggravate the voltage overshoot problem. A programmable initial current control technique for the PRDCLI was reported by Lai and Bose (1991). This scheme is somewhat complex from the implementation viewpoint. In this paper we present a novel current initialization technique for the resonant circuit which ensures reliable zero voltage switching. The proposed method is based on a state transition equation and is simple to implement.

The philosophy is to switch the device only when the voltage across it is zero. For a given set of resonant link parameters, a constant resonant oscillation period is selected. The state vector consists of link capacitor voltage (v_C) and inductor current (see figure 1). The capacitor voltage must be zero at the start and at the end of every resonant oscillation period for successful ZVS (figure 2 (*a*)). With this condition, the exact initial value of the inductor current (i_R) is determined. In order to start a resonant cycle with this value of the initial current, the time duration for which the dc bus must be shorted can be calculated. Thus, the initial inductor current is generated by shorting S_5 in figure 1 (*a*), and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. Thus the link capacitor voltage returns to zero after the pre-specified resonant oscillation period. Figure 2 (*b*) shows the state-plane trajectory where the transition along the curve (e.g. t_0 to t_1) takes the fixed pre-specified time. The transition along the vertical axis ($v_C \simeq 0$) takes a variable time (e.g. t_1 to t_2), depending on the load current.



(a)



(b)

Figure 2. (*a*) Link voltage and current waveforms with associated timings; (*b*) state-plane diagram.

2. Proposed current initialization method

The schematic diagram of a single-phase PRDCLI that runs from a dc supply (V_{dc}) is shown in figure 1 (*a*). This contains a resonant circuit generated by the dc source, an inductor (L) and a capacitor (C), as shown in this figure. The inductor coil has a resistance (R) and a finite Q-factor. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The four switches (S_1-S_4) are connected across the link and are switched when the link voltage is zero. One additional switch (S_5) is added to the circuit to short the link at the end of a resonant cycle. The resistance R_S represents the ON-resistance of this switch and stray resistance of the circuit. The duration of the shorting period is predetermined such that the link current (i_R) can be built up to a desired value to sustain the resonance.

The proposed current initialization scheme is explained with the help of the waveform of capacitor voltage v_C and link current i_R as shown in figure 2 (*a*). The resonant cycle starts at time t_0 and ends at time t_1. Similarly, the next resonant cycle starts at t_2 and ends at t_3. The interval $t_2 - t_1$ is used to build up the current $i_R(t_2)$ in the inductor L by turning on switch S_5. To ensure that no zero-crossing failure occurs at t_3, the current through the inductor L at time t_2 must be built up to the required value. The choice of the interval $t_2 - t_1$ depends on this requirement which, in turn, depends on the input current i_0 of the inverter (figure 1 (*a*)). The instant t_2 is calculated such that the current at this instant is sufficient to bring the capacitor voltage to zero again after a resonant cycle. Note that the switch S_5 is turned off at instant t_2 and the resonant cycle starts all over again.

In this paper we propose a scheme in which the duration of the resonant cycle (e.g. $t_3 - t_2$) is fixed at ΔT (μs). Note that the particular value of ΔT chosen depends on the parameters of the resonant circuit. This time is slightly smaller than the undamped period of the resonant circuit. Since a resonant cycle time is much smaller than the time constant of the load circuit, the load current is assumed to be a constant current equal to I_0 over a particular resonant cycle. This gives the equivalent circuit of figure 1 (*b*). In a practical circuit I_0 is estimated in the previous cycle, that is, any time between t_0 and t_1, and is used for predicting $i_R(t_2)$. This is acceptable as the resonant cycle time is small.

Referring to figure 1 (*b*), let us define a state vector as $x = [v_C \quad i_R]^T$ and an input vector as $u = [I_0 \quad V_{dc}]^T$. The state-space equation of the circuit with S_5 off is then given by

$$\dot{x} = Ax + Bu \tag{1}$$

where the matrices A and B are given by

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & -R/L \end{bmatrix}, \quad B = \begin{bmatrix} -1/C & 0 \\ 0 & 1/L \end{bmatrix}.$$

The solution of (1) for an initial time t_0 and final time t_f is given by

$$x(t_f) = e^{A(t_f - t_0)} x(t_0) + \int_{t_0}^{t_f} e^{A(t_f - \tau)} Bu(\tau)\, d\tau \tag{2}$$

Noting that the resonant cycle is defined as $\Delta T = t_3 - t_2$, the solution of (1) at instant t_3, based on the initial condition at instant t_2, is given from (2) as

$$x(t_3) = e^{A\Delta T} x(t_2) + \int_0^{\Delta T} e^{A(\Delta T - \tau)} B u(\tau)\, d\tau \tag{3}$$

Note that in the above equation V_{dc} is constant and I_0 is assumed to be known and constant, and therefore u is known.

The estimation of $i_R(t_2)$ can be viewed as a boundary-value problem (BVP). Refer to figure 2(*a*) in which the capacitor voltage can be seen as zero at both instants t_2 and t_3. Thus the state vector at these two instants will contain a 0 for the capacitor voltage and unknown values of the link current, i.e. $x(t_2) = [0 \quad i_R(t_2)]^T$ and $x(t_3) = [0 \quad i_R(t_3)]^T$. Let us now define the following two matrices

$$\phi = e^{A\Delta T} \quad \text{and} \quad \theta = \int_0^{\Delta T} e^{A(\Delta T - \tau)} B\, d\tau$$

Since the vector u is a constant between the interval instants t_2 and t_3, we can then modify (3) as

$$x(t_3) = \phi x(t_2) + \theta u(t_2)$$

Substituting the values of $x(t_3) = [0 \quad i_R(t_3)]^T$ and $x(t_2) = [0 \quad i_R(t_2)]^T$ and writing the matrices in full, we get

$$\begin{bmatrix} 0 \\ i_R(t_3) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \begin{bmatrix} 0 \\ i_R(t_2) \end{bmatrix} + \begin{bmatrix} \theta_{11} & \theta_{12} \\ \theta_{21} & \theta_{22} \end{bmatrix} \begin{bmatrix} I_0 \\ V_{dc} \end{bmatrix}$$

We therefore obtain the following two equations for $i_R(t_2)$ and $i_R(t_3)$

$$i_R(t_2) = -\frac{1}{\phi_{12}} [\theta_{11} I_0 + \theta_{12} V_{dc}] \tag{4}$$

$$i_R(t_3) = \phi_{22} i_R(t_2) + [\theta_{21} I_0 + \theta_{12} V_{dc}] \tag{5}$$

Since A, B and ΔT are known *a priori*, the matrices ϕ and θ can be evaluated numerically. The state plane trajectory under the BVP is shown in figure 2(*b*), where v_C is assumed to be approximately zero when the switch S_5 is closed. The value of $i_R(t_2)$ given by (4) is required to ensure the zero-crossing of v_C ΔT seconds later, at the instant t_3.

The calculation of $i_R(t_2)$ in equation (4) uses the value of the load current I_0. This current is assumed to be constant during one resonant cycle of interval ΔT. An estimate based on the previous cycle, that is, a value of I_0 at t_0, must be used if (4) is to predict the value of $i_R(t_2)$. Equations similar to (4) and (5) can be written for each resonant cycle occurring during the interval $t_0 - t_1$, $t_2 - t_3$ etc. In each case I_0 may be different as a result of changes in the load.

Once $i_R(t_2)$ is obtained, there are two ways of obtaining the time interval $t_2 - t_1$ for which the capacitor should be shorted. These are discussed below.

2.1. *Method 1*

This is based on mathematical calculation and will produce fairly accurate results. This method, however, is only suitable for simulation studies. The circuit equation for the time interval between t_1 and t_2 is given by

$$\frac{di_R}{dt} = -\frac{R}{L} i_R + \frac{1}{L} V_{dc} \tag{6}$$

In the above the switch S_5 is assumed to be ideal, that is, $R_S = 0$. The solution of the equation is given by

$$i_R(t_2) = \exp\left(-\frac{R}{L}\Delta t\right) i_R(t_1) + \frac{V_{dc}}{R}\left\{1 - \exp\left(-\frac{R}{L}\Delta t\right)\right\} \tag{7}$$

where $\Delta t = t_2 - t_1$. Equation (7) is solved to obtain an expression for Δt as

$$\Delta t = \frac{L}{R} \ln\left\{\frac{i_R(t_2) - V_{dc}/R}{i_R(t_1) - V_{dc}/R}\right\} \tag{8}$$

We can then calculate Δt from (8) using $i_R(t_2)$ calculated from (4) and measured values of $i_R(t_1)$. The value of I_0 at t_0 is used in (4).

There are a couple of problems associated with the above approach. The measurement of $i_R(t_1)$ is required for the computation of Δt and this can be available at some time after t_1. This leaves very little time for computation of Δt. Note that Δt is of the order of a few microseconds. Hence it is almost impossible to compute equation (7) in real time. Even if we assume that this time duration is computed earlier with a prior knowledge of $i_R(t_1)$, it is difficult to generate this time delay using a real-time clock. For example, in one cycle this time is computed as 4.71 μs and in the next cycle it is computed as 4.73 μs. A very high-speed and stable clock and counter circuits will be required to differentiate between these two values in real time. If the time delay is created using software, this resolution is rather difficult to achieve even with modern high-speed computers.

We can, instead, use the measurement of i_R at instant t_0 to find an estimate of $i_R(t_1)$, using equations similar to (4) and (5) for the interval $t_0 - t_1$. This does give an analytical solution for Δt. This will, however, mean that we are using an estimate of this current rather than its actual measured value. This will cause an error in computation between the actual and computed value. The accumulation of error may in turn cause sustained zero-crossing failures, forcing the link to collapse.

2.2. *Method 2*

A more workable solution is to compare, in an analogue comparator, the computed value of current $i_R(t_2)$, obtained from equation (4), with the actual value link current i_R while switch S_5 is turned on and kept closed. This switch is opened when these two values are equal. This ensures that the link current is built up to the required level of initial current such that the link voltage goes to zero at instant t_3, i.e. at the end of the resonant cycle. The value of I_0 at t_0 is used in (4). The implementation is discussed in § 3.

3. Hardware implementation details

The power circuit, shown in figure 1, is similar to that of a normal PWM inverter circuit except for the introduction of the resonant circuit between the dc supply and the inverter bridge. The inductor is made of litz wire to provide a high Q. This inductor is designed to provide the required value and Q-factor. The capacitor used is a polypropylene type that has very low ESR. This is suitable for high frequency ac operation that can take bidirectional current. The values of the inductor, capacitor and the dc side voltage are

$$\text{inductor} \quad L = 52\,\mu\text{H}, Q = 60$$
$$\text{capacitor} \quad C = 0.89\,\mu\text{F}$$
$$\text{dc voltage} \quad V_{\text{dc}} = 65\,\text{V}$$

With these values of inductor and capacitor the undamped oscillation time is about 42.75 μs. Therefore, a time duration of 37.5 μs is chosen as the resonant cycle time ΔT, taking account of the finite Q-factor of the coil.

The control circuit diagram is shown in figure 3. The heart of this circuit is a Pentium personal computer (PC) along with its associated high-speed analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC). The PC is used for the computation of the initial current from equation (4). In this equation θ_{11}, θ_{12} and ϕ_{21} are constants that are dependent on the circuit parameters and the time ΔT. These are pre-computed and stored. The load current (I_0) and the dc voltage are measured through Hall-effect sensors at the start of every resonant cycle (e.g. t_0, t_2, etc.) and are converted through the ADC. These measured values, along with the constants mentioned above, are used for the computation of the initial current for the next cycle. This process is repeated for every resonant cycle. Note that the computation here is fairly simple and can also be achieved through a hardware configuration. However, the arrangement of introducing a PC makes the control circuit much more flexible than a hardwired circuit. Furthermore, due to the presence of the PC, the circuit delays can also be taken into account for accurate zero-voltage switching.

As soon as the required initial current is computed in the PC, it is converted into analogue signal through a DAC. The computation time required is much smaller than the resonant cycle time ΔT. This signal is then available to the comparator for comparison with the actual link current. The link current is monitored continuously through a Hall-effect current sensor. When the link current becomes equal to the required initial current, the comparator output becomes zero. This output is used for clearing the J–K flip-flop. Once the flip-flop is cleared its output (Q) becomes zero and $\bar{Q}$ becomes unity. This is then used for switching off S_5 through a buffer. Simultaneously, the inverted output ($\bar{Q}$) of the J–K flip-flop is used for triggering

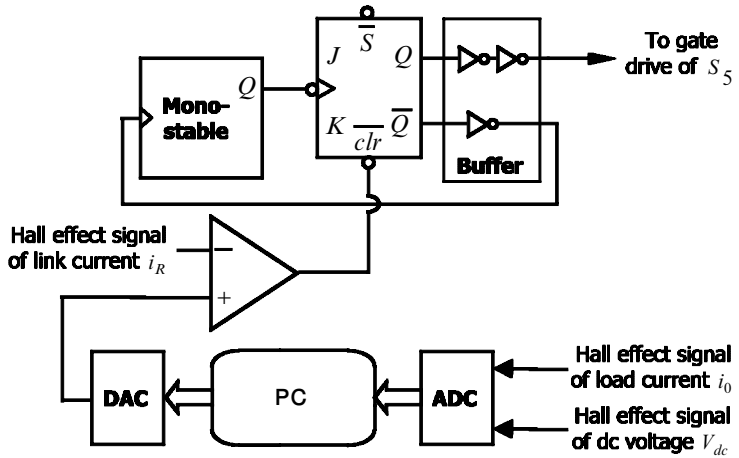


Figure 3. Schematic diagram of PRDCLI control circuit.

the monostable through an inverting buffer. The monostable is set to give a pulse width of 37.5 μs. Once this time elapses, the negative going edge of the monostable output is used for clocking the flip-flop. This forces the output of the flip-flop to one and, consequently, the shorting switch S_5 is turned on.

Through the above scheme, zero-voltage switching is obtained. Note that, during the time when S_5 is on, the switching transitions of the switches S_1-S_4 take place. To ensure that these switches are turned on or off only during this prescribed interval, the gatings of S_1-S_4 are conditioned by the output Q of the J–K flip-flop. Further note that the configuration of the switches S_1-S_4 at a particular resonant cycle is dependent on the load connected to the output of the inverter.

4. Simulation and experimental results

In this section we present the results of three different tests that have been performed. The system parameters are the same as those mentioned in the previous section. We shall present the results obtained through both digital computer simulation studies and experiment.

4.1. *No-load test*

This test is performed to show the zero-voltage switching condition. The inverter is operated with no load connected at its output ($i_0 = 0$). The link voltage goes to zero after every 37.5 μs, as is evident from the simulation results shown in figure 4. It can be seen that the link capacitor voltage has a peak of about 130 V and that the current rises linearly during Δt. The experimental results with no load are shown in figures 5–7. In figure 5, the link voltage, link current and the gating signal of switch S_5 are shown. The link current and the output of the monostable are shown in figure 6. It can be seen that the monostable goes low after every 37.5 μs and remains low in that state till the comparator is activated. This illustrates the working principle of the proposed current initialization for the PRDLCI.

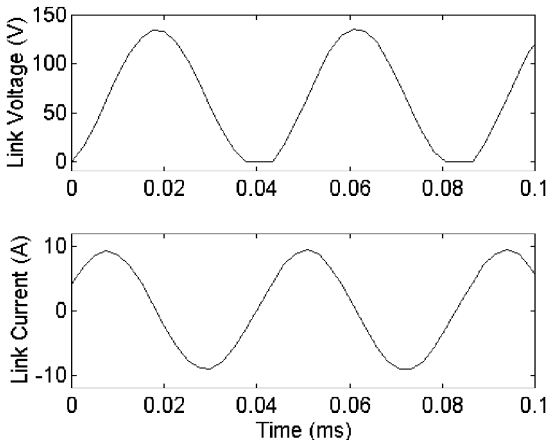


Figure 4. Simulation results for no-load test.

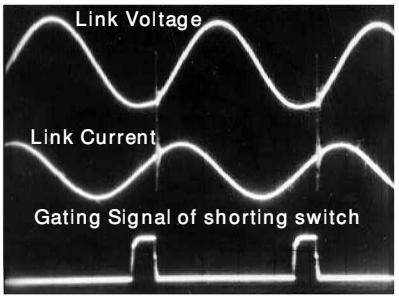


Figure 5. Link voltage, link current and gating signal of the shorting switch for no-load test.

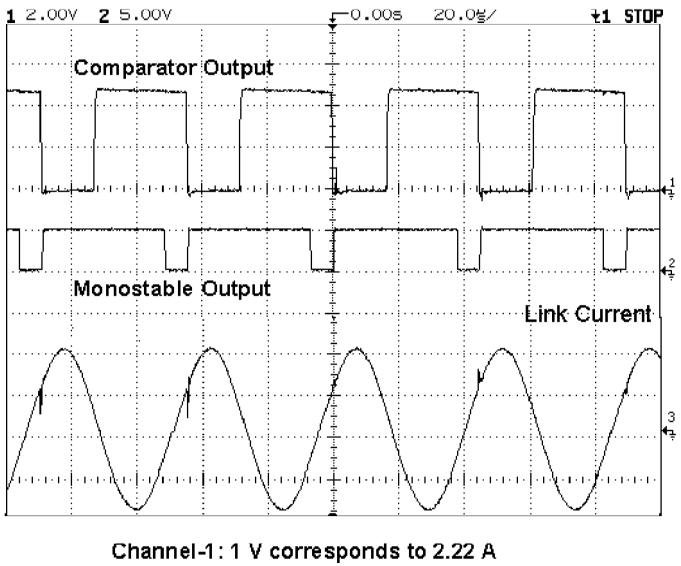


Figure 6. Link current, monostable output and comparator output for no-load test.

4.2. *Frequency response test*

A PRDCLI is normally used for motor drive applications. It can further be used for active filtering (Mahapatra *et al.* 1997), sophisticated power supplies etc. It is therefore important to show the capability of this device in tracking reference waveforms of differing nature, amplitude and frequency. The purpose of this test is to demonstrate this behaviour. In this test, a reference current is generated from a signal generator. The output current of the inverter is constrained to follow this reference current in a zero hysteresis bang-bang mode by properly gating the switches S_1–S_4. The load of figure 1 (*a*) chosen for this study has an inductance of 17 mH and a resistance of 10 Ω.

In the first instance, a reference current of amplitude 1 A and frequency 100 Hz is chosen. The simulation results are shown in figure 7 and the practical implementation results are shown in figure 8. It can be seen that the results obtained for the two

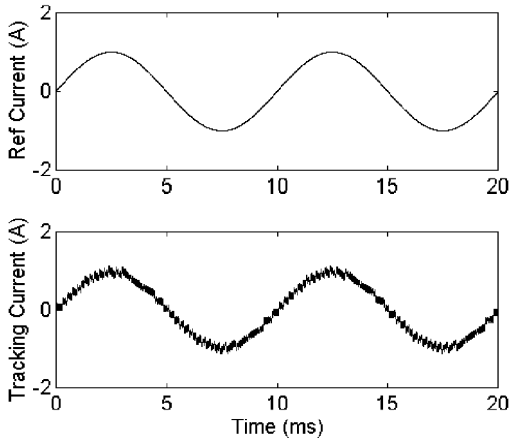


Figure 7. Simulation results for tracking a 100 Hz sinusoid.

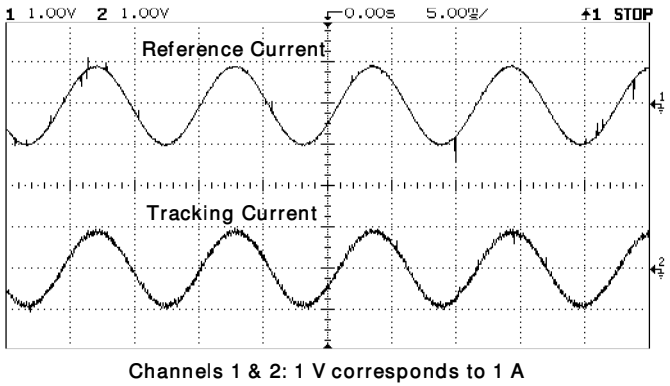


Figure 8. Experimental results for tracking a 100 Hz sinusoid.

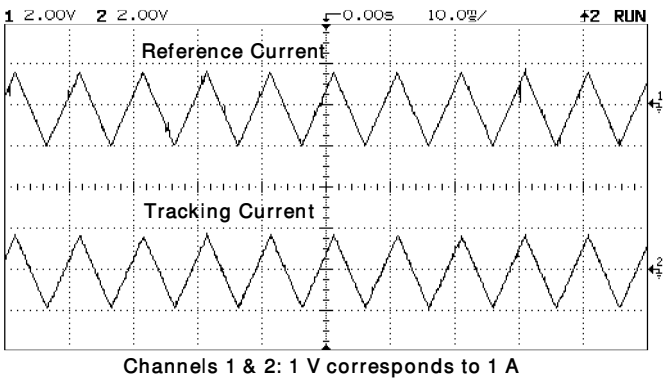


Figure 9. Experimental results for tracking a 100 Hz triangular waveform.

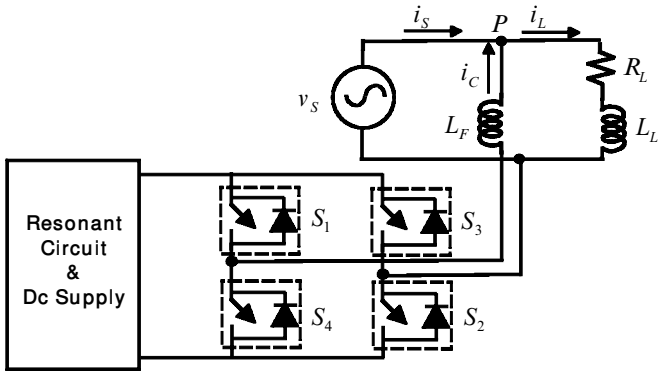


Figure 10. Schematic diagram of power factor correction arrangement.

cases are almost identical and that the reference current is properly tracked by the inverter. For this test the current i_0 (see figure 1) is a variable that takes on different positive and negative values in a continuously variable form in order to track the reference current. Successful operation of a PRDCLI implies that the zero voltage switching is maintained under this condition. Therefore the current initialization scheme is validated.

To illustrate this principle further, a triangular reference current of magnitude 2 A and frequency 100 Hz is chosen. The reference and tracking waveforms for the practical implementation are shown in figure 9. It can be seen that the reference is tracked perfectly.

4.3. *PRDCLI as load compensator*

In this test, the PRDCLI is used for power factor correction. This is illustrated in figure 10 in which an R-L load is connected to an ac supply voltage v_S. It is well known that the source current (i_S) will lag the supply voltage. We now inject a current (i_C) through the PRDCLI such, that the source current (i_S) is in phase with v_S. This is done at the point of common coupling P at which the output current (i_C) is injected into the network through an interfacing inductor (L_F). In this example we have chosen the following:

ac supply voltage v_S	$50\sin(100\pi t)$
load resistance L_L	27.57 mH
load resistance R_L	50 Ω
interface inductance L_F	17 mH

First we measure the load current when the PRDCLI is not connected at the point of common coupling. This current is found to be of magnitude 0.5 A and has a phase angle of 60°C (lagging). Therefore, the active component of this current is 0.25 A. Applying KCL at the point of common coupling P, we set a reference for the PRDCLI current (i_C) as $i_L - 0.25\sin(100\pi t)$, where i_L is measured using a Hall-effect current sensor and the second component is phase-locked with the supply voltage. Through this design example we achieve a unity power factor of the source current.

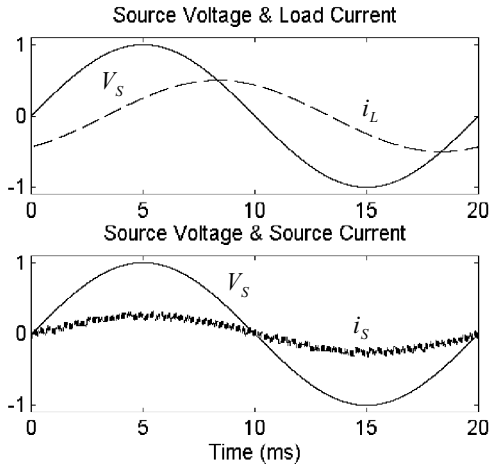


Figure 11. Simulation results for power factor correction case study.

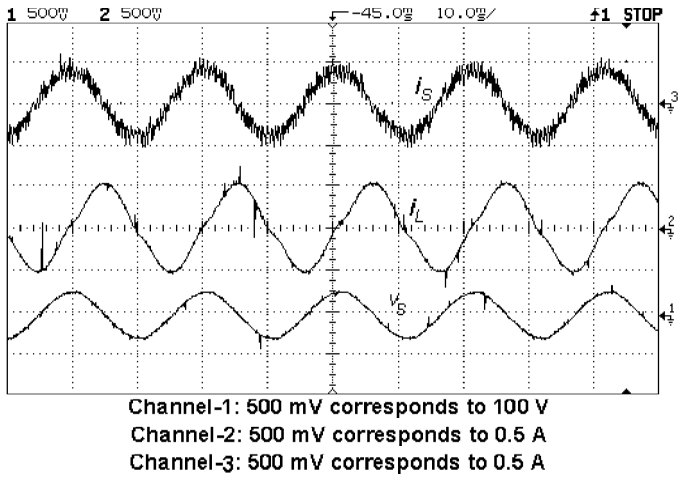


Figure 12. Source voltage, source current and load current waveforms for power factor correction case study.

The simulation results for this case are shown in figure 11 and the experimental results are shown in figure 12. Note that in figure 11 the supply voltage is scaled by a factor of 50 to bring its magnitude to the same order as that of the currents. It is evident from all these figures that the unity power factor operation is achieved by using the PRDCLI.

5. Conclusions

A new current initialization scheme for a parallel resonant dc link inverter is proposed in this paper. This initialization scheme is based on a boundary value problem. It is shown that this current can be predicted very accurately, which in turn ensures the zero-crossing of the link voltage at a prescribed time instant. The

proposed scheme is validated through simulation and experimental studies. The proposed method is elegant and quite precise, yet simple to implement.

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