Design of Single Node Upset Resilient Latch for Low Power, Low Cost and Highly Robust Applications

Anwesh Kumar Samal
Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela, India
anweshsamal@gmail.com

Sandeep Kumar
Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela, India
sandeep_kumar@nitrkl.ac.in

Atin Mukherjee
Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela, India
mukherjeea@nitrkl.ac.in

***Abstract*—This paper proposes a soft error-resilient latch (SERL), which is capable of self-recovering of all possible single event upsets (SEU). The latch mainly uses two 1-output C-elements and a 2-output C-element to create interlocked feedback loops. Simulation results from Mentor Graphics T-SPICE show that proposed SERL is complete resilient to SEU from all of its internal nodes and the output node. Compared to the existing SEU resilient latches, the proposed latch shows the least power dissipation and area overhead, and the lowest cost in terms of power delay area product (PDAP). The proposed latch saves on average approximately 24.29% power, 10.24% area, improves 12% delay and 40% PDAP in comparision to other existing resilient latches.**

***Keywords*—Single node upset, radiation hardened latch, robustness, soft errors, single event upset.**

I. Introduction

CMOS scaling technologies are rapidly advancing, enabling the creation of smaller and more power-efficient electronic devices, with modern SoC designs chipsets. However, this trend towards miniaturization comes at a cost, as smaller devices are more susceptible to execution failures and data upsets due to radiation induced soft errors, particularly in the domain of memory designs such as latches. Latches, which store one bit of data at a time, are of particular concern in atmospheric environments where high radiation particles, such as cosmic rays, are present. When these particles strike any of the transistors in the latch, a transient current is passed which causes a voltage spike, resulting in a single event upset (SEU). Essentially, high energy particles striking any node cause the release of an electron-hole pair, with the resulting charge being efficiently collected at the affected node by drift processing. These events lead to single event transients (SETs), with the glitch being latched referred to as a SEU [1]. Fig. 1 shows the SEU mechanism in the latch. Therefore, the design of radiation-resilient memory is essential for CMOS technology, particularly as we progress further into nuclear energy and space science. When exposed to ionizing radiation, devices can accumulate electrical charge, leading to bitflips, latch-ups, and other errors, particularly in memory circuits which store and retrieve critical information. High energy particles can introduce two types of error - soft errors, such as SEUs, which are transient changes in the state of a digital circuit, and hard errors which are more destructive. Without appropriate measures to mitigate these effects, such errors can result in severe malfunctioning of expected data due to voltage drops and node capacitance, making the system susceptible to induced charge from high energy radiation particle attacks [2].

Due to the possible influence of radiation-induced effects, which can cause electronic equipment to malfunction or produce mistakes, radiation-hardened memory is becoming increasingly important in CMOS (complementary metal oxide semiconductor) technology. As we learn more about technology connected to nuclear energy and space research, this need becomes even more crucial . Ionising radiation exposure from sources like nuclear or cosmic rays can cause electrical charge to build up inside the device, which can result in glitches like bitflips and latch-ups as well as other problems.

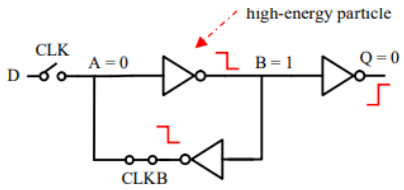


Fig. 1. Occurrence of SEU

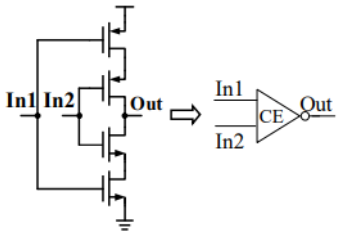
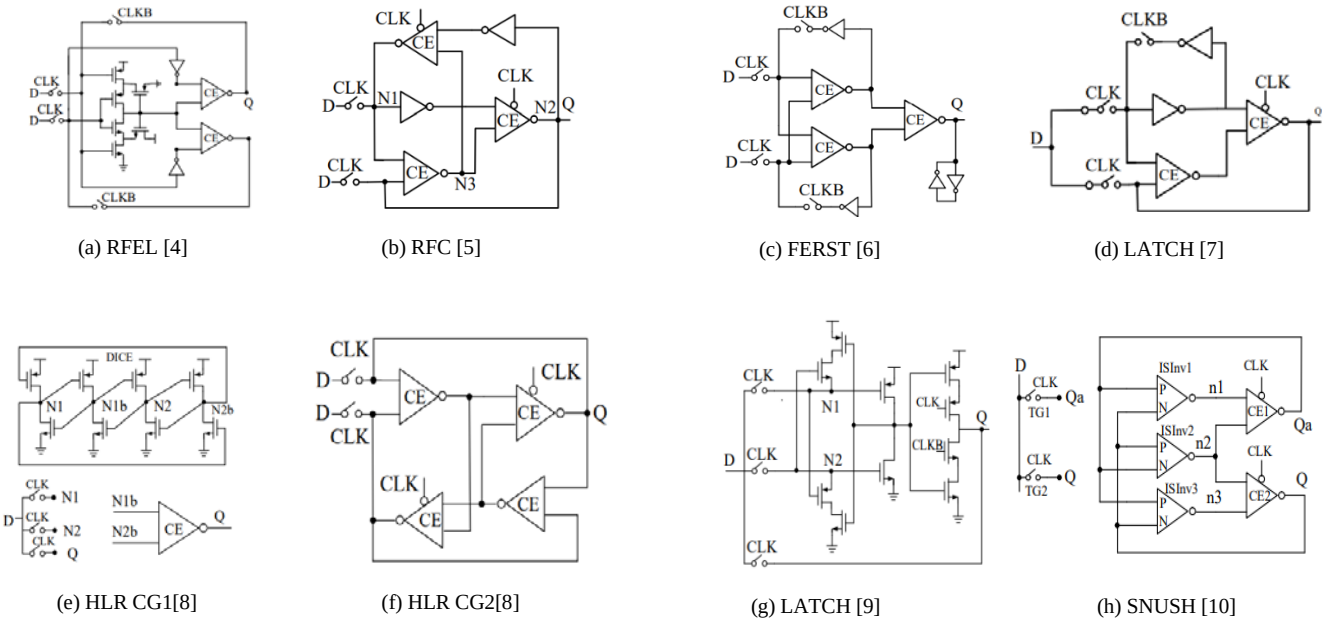


Fig. 2. Muller's C element

Since memory circuits are in charge of storing and retrieving data, these faults can be extremely troublesome. Both soft and hard mistakes can be produced by high energy particles. SEU is a mild error as it is caused by a transient change in the state of a digital circuit. Even though these errors are less severe than hard errors, ignoring them can still result in substantial data corruption and persistent circuit malfunction. Due to decreased node capacitance and voltage loss, which limits the amount of charge that can be deposited on a node, the system is more susceptible to induced charge from a high-energy radiation particle attack.

Various static hardware redundancy methods for permanent fault tolerance are also widely utilised in memory components that are built to be resilient to any sort of transient and permanent defects [3]. However, these methods incur enormous expense in terms of hardware and power overheads. To combat this, radiation-hardened-by-design (RHBD) techniques have been used at the circuit level to offer SE protection that is both affordable and effective. Radiation-hardened latches have frequently been created using C-elements (CE), as seen in Fig. 2. A CE behaves like an inverter when the inputs are the same, but it keeps the prior value when the inputs are different.

Latch hardening techniques include tolerance and self-healing or resilience. In the tolerant latches, the output node is



(a) RFEL [4] (b) RFC [5] (c) FERST [6] (d) LATCH [7]

(e) HLR CG1[8] (f) HLR CG2[8] (g) LATCH [9] (h) SNUSH [10]

Fig. 3. Existing Radiation Hardened SNU Latches

only resilient to SEU but internal nodes remain upset after radiation event. However, resilient latches are capable to self-recover from all of its affected internal and the output nodes, making the resilient latch highly robust.

In this paper, we propose a design for radiation-hardened latch that offers total defence against SEUs and has the ability to self-heal from any single node upset (SNU) that may happen while it is operating in hold mode. We have referred to SEU and SNU interchangeably throughout the text. The past has seen the development of a number of SNU-resistant latches, but each has its own shortcomings in terms of cost and/or strength. In contrast to the existing SEU hardened latches, our proposed latch has the following advantages:

1) The proposed latch is complete resilient to SEU and it offers higher robustness than the tolerant latches.

2) The proposed latch consumes the least power compared to other resilient latches.

3) The proposed latch occupies smaller area than most of the existing resilient latches.

4) The proposed latch also offers the lowest cost in terms to PDAP compared to other existing resilient latches.

The remaining sections are organised as follows: The second section examines the existing radiation hardened latch. Section III describes the latch's cell structure, behaviour, and self-healing verification using simulation results. Section IV contains a comparison and evaluation of costs.

II. Existing Hardened Latches

Previously many research has been conducted to develop radiation hardened latches and a brief review has been stated in this regard in the following section. Two 2-input CEs and an input-splitting Schmitt trigger (ST) are used to design the RFEL [4] in Fig. 3(a), which results in mutually feeding back structures that provide complete SEU self-healing and SET filterability. However, the power and delay overheads are quite high.

The RFC latch [5] shown in Fig. 3(b) using a 2-input CEs, two 2-input CG-based CEs, and two inverters to provide complete SEU resilience. However, similar to HLR-CG2 the area of the latch can be still optimized.

Two feedback interlocked loops are formed using three CEs and inverters to provide SEU-tolerant by the FERST latch in [6], which is depicted in Fig. 3(c). However, the latch is not capable of self-recovering from all possibles SNU. Moreover, to avoid high impedance state (HIS) the latch requires week keeper, which consumes more area and power overheads.

The Latch in [7], shown in Fig. 3(d), employs two cross-coupled components to build negative feedback loops, which facilitates SEU tolerance. However, the latch is not capable of recovering from SNU at its internal nodes.

The HLR-CG1 [8], depicted in Fig. 3(e), employs one dual-interlocked storage cell (DICE) and one two input CE to provide complete recovery from all possible SNUs. Indeed, the latch is complete SNU resilient but presence of active feedback loop in DICE makes it to dissipates high power. The HLR-CG2 latch [8], shown in Fig. 3(f) is designed using two inputs CEs and two CG-based CEs with the help interlocked feedback loops, the latch is capable of recovering from all possible single node upset Snus. However, the area can be still optimized.

The latch in [9], depicted in Fig. 3(g), employs an input-splitting inverter, and restorative circuits based on memory elements. The insufficient driving paths for particular internal nodes, however, reduce its resilience. Moreover if 1 to 0 SEU at node N1 makes the latch to store incorrect value.

The SNU self-healing latch SNUSH [10] shown in Fig. 3(h) provides complete resiliency to SEU by the help of inter-locked feedback loops formed by input-splitting inverters and clock gating based CEs. However, similar to HLR-CG2 and RFC the cost can be optimized. The major factor of improvement is based on reducing the PDAP value which will lead to cost effective nature of latch.

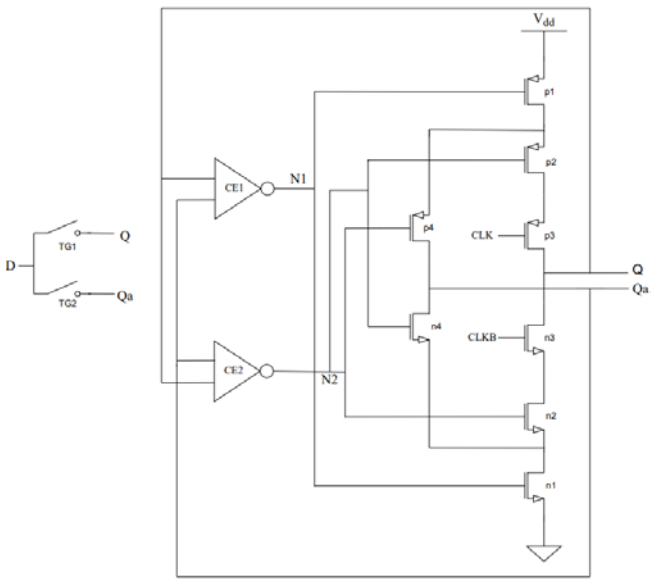


Fig 4. Proposed radiation hardened SERL latch

III. Proposed SEU Resilient Latch

A. *Latch Design and Behaviour*

The schematic of the proposed SERL latch is shown in Fig. 4. The SERL latch creates interlocked feedback loops using 2-input CEs, and a 3-input 2-output CE. The TGs (TG1 and TG2) are used to transfer the data in the latch. The latch has D as the primary input, CLK as the system clock, the internal nodes N1 and N2, and the output node Q (or Qa).

The simulation for the normal D-latch in an error-free condition is shown in Fig. 5. When the clock is high, the latch operates in transparent mode and D directly drives the output nodes Q and Qa through transmission gates (TGs). In this mode, CG based 3-input 2-output CE avoids active feedback loops and current competition at output node Q. Hence, the power dissipation and propagation delay are effectively reduced.

During the hold mode, the clock switches from high to low, turning off both TGs and preventing D from driving the output nodes Qa and Q. Assuming that D is logic '0' when in transparent mode, the logic values at the capacitive nodes Q and Qa are also '0' making the nodes N1 and N2 logic '1'. The 3-input 2-output CE receives logic 1 input from the internal nodes N1 and N2 and produces logic low at output nodes Q and Qa. Thus, in hold mode, the interlocked feedback loops maintain correct logic values at all of internal and output nodes. Thus, as illustrated in Fig. 6 in hold mode, the interlocked feedback loops maintain correct logic values at all its internal and output nodes.

As there are 4 nodes, so by considering both types of transients, i.e., 0 to 1 and 1 to 0 at each node, there will be total of 8 possibilities for SEU occurrences. In the next, we shall discuss for this 8 SNU cases (Sn) in hold mode.

When logic '0' is being stored, i.e., Q = Qa = 0 and N1 = N2 = 1. The following four SEU incidents could occur in this state:

S1: Suppose a high energy particle strikes at Q and its state changes to 1 from 0. Earlier the values of N1 and N2 were equal to 1 which needs to be preserved to restore the

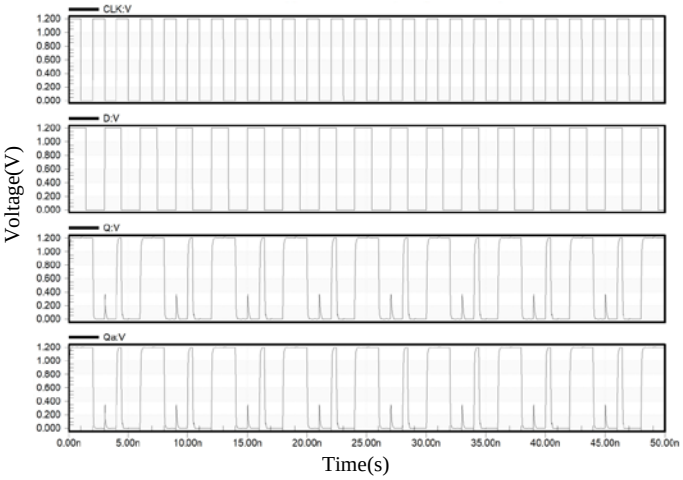


Fig 5. Simulation results for normal latching conditions

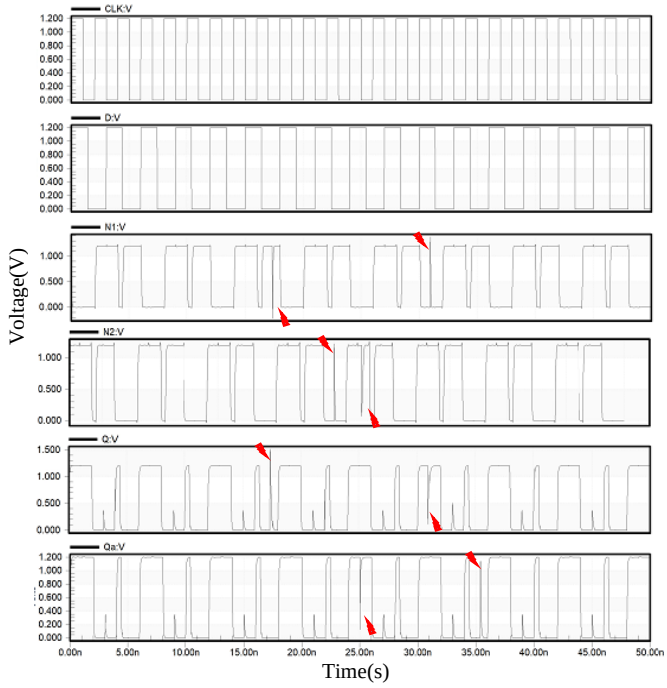


Fig 6. Simulation Results for SEU tolerance of SERL latch

original input state at the CEs and according to characteristics of C element if inputs are different the output will hold the previous values Therefore, the internal nodes N1 and N2 are at their original states, making p1, p2 off and n1, n2 on. Hence node Q regains its correct logic '0' value.

S2: If Qa changes from 0 to 1. Earlier the values of N1 and N2 were equal to 1. Now one input at CE1 and the second input at CE2 will change to 1. So, there will be a different input pair at the C elements and similar to case S1 the internal nodes N1 and N2 are unchanged. So p1, p4 are off and n1 and n4 are on which helps in recovering node Qa to its correct logic '0' state.

S3: Considering the SEU affects internal node N1 and its value changes to 0 from 1. The following combination occurs at the CMOS design part of 3-input 2-output CE: the MOSFETS p1 and n2 becomes ON whereas p2 and n1 becomes OFF. However, the error introduced at the internal node does not propagate to Q and Qa retaining its previous correct value. Hence, the logic low states of the nodes Q and

TABLE I. COST COMPARISON AND ROBUSTNESS WITH THE EXISTING SEU RESILIENT LATCHES

Latch	P (µw)	T_p (ps)	A_T (μm^2)	PDAP	Robustness
FERST[6]	18.28	102.69	0.253	474.92	Tol.[a]
Latch [7]	15.49	25.30	0.214	83.86	Tol.
Latch [9]	12.23	19.94	0.175	42.67	Tol.
HLR-CG1[8]	28.30	32.06	0.195	176.94	Res.[b]
HLR-CG2[8]	16.64	26.75	0.253	112.61	Res.
RFC[5]	16.94	26.81	0.253	114.97	Res.
RFEL[4]	25.45	172.52	0.273	1198.64	Res.
SNUSH[10]	17.26	25.36	0.234	103.26	Res.
Proposed SERL	14.27	29.09	0.214	88.81	Res.

[a] *Tol. stands for Tolerant*
[b] Res. *stands for Resilient*

Qa help in recovering of node N1 to its original logic '1' state through CE1.

S4: Considering the internal node N2 value changes to low from high. There is a similar way of mismatching events. The MOSFETS p2 and p4 become ON whereas p1, n4 and n2 becomes OFF. However, the error introduced at the internal node does not propagate to Qa and Qa retaining its previous correct value. Hence, the logic low states of the nodes Q and Qa help in recovering of node N2 to its original logic '1'.

When logic '1' is stored, the value of Q = Qa = 1 and N1 = N2 = 0. There are following four more possible cases of SEU occurrence:

S5: Suppose a high energy particle strikes at Q and its state changes to 0 from 1. Earlier the values of N1 and N2 were equal to 0 which needs to be preserved to restore the affected nodes. Now one input at CE1 and second input at CE2 will change to 0. So, there will be a different input pair at the CEs and according to characteristics of C element if inputs are different the output will hold the previous values. Therefore, the internal nodes N1 and N2 are at their original states, making p1, p2 ON and n1, n2 OFF. Hence node Q regains its correct logic '1' value.

S6: If Qa changes from 1 to 0. Earlier the values of N1 and N2 were equal to 0. Now one input at CE1 and second input at CE2 will change to 0. So, there will be a different input pair at the C elements and similar to case S1 the internal nodes N1 and N2 are unchanged. So p1, p4 are ON and n1 and n4 are OFF which helps in recovering node Qa to its correct logic '1' state.

S7: Considering the SEU affects internal node N1 and its value changes to 1 from 0. The following combination occurs at the CMOS design part of 3-input 2-output CE: the MOSFETS p1 and n2 becomes OFF whereas p2 and n1 becomes ON. However, the error introduced at the internal node does not propagate to Q and Qa retaining its previous correct value. Hence, the logic high states of the nodes Q and Qa help in recovering of node N1 to its original logic '0' state through CE1.

S8: Considering the internal node N2 value changes to high from low. There is similar way of mismatch events. The MOSFETS p2 and p4 become OFF whereas p1, n4 and n2 becomes ON. However, the error introduced at the internal node does not propagate to Qa and Qa retaining its previous correct value. Hence, the logic high states of the nodes Q and Qa help in recovering of node N2 to its original logic '0' state through CE2.

From the above discussion, it is clear that the proposed latch is capable of self-recovering from all of its affected internal and the output nodes, making the latch complete resilient to SEUs.

TABLE II. RELATIVE OVERHEADS OF SEU-RESILIENT LATCHES IN COMPARISON WITH PROPOSED LATCH

Design Name	ΔPower (%)	ΔDelay (%)	ΔArea (%)	ΔPDAP (%)
HLR-CG1[8]	49.57	9.26	– 9.74	49.82
HLR-CG2[8]	14.24	– 8.74	15.41	21.13
RFC [5]	15.76	– 8.51	15.41	22.75
RFEL [4]	43.93	83.13	21.62	92.59
SNUSH [10]	17.33	–14.71	8.54	13.33
Average	24.29	12.09	10.25	39.92

B. SEU Resilience Verification

The simulation of the proposed SERL latch for SEU-resilience verification has been carried out by Mentor Graphics Tanner Tool using 65 nm CMOS technology. The supply voltage is held at 1.2 V, and the working temperature is kept at 27°C. The simulation has been performed at 0.5 GHz operating frequency. The faults are injected using a double-exponential current source model with rise and fall time constants of 0.1 ps and 3 ps, respectively.

The NMOS and PMOS transistor widths are held constant at 100 nm and 200 nm, respectively, to produce the SERL and the transistor length is kept constant at 65 nm.

In error free case, the proposed latch performs similar to the conventional D latch. The Fig. 5 shows the simulation for the latch in error free case.

The Fig. 6 shows the SEU self-recovery verification of the proposed latch. The faults have been injected in node N1 at times 17.5 ns and 32 ns, in node N2 at times 25 ns and 28 ns, in node Q at 17 ns and 33 ns, in node Qa at 25 ns and 37 ns respectively. The fault injection simulation results from Fig. 6 shows that all these injected errors are restored to their original states. For instance, if we consider the case when N1 holds the logic '1' state and an error is injected at 17.5 ns the voltage value changes to logic '0' state but due to the self-healing capacity of the SERL, the latch is rectified to its previous logic '1' state within a small instance of time.

IV. LATCH ASSESMENT AND COMPARISON

For the purpose of comparison, the proposed SERL latch and the latches existing in the literature as discussed in Section II— RFEL [4], RFC [5], FERST [6], Latch [7], HLR-CG1 [8], HLR-CG2 [8], Latch [9] and SNUSH [10] were designed using the same simulation conditions that were used for the proposed SERL latch.

In Table I, the proposed latch is compared with other existing SEU hardened latches in terms of cost and robustness. The term "Power (P)" in this context refers to the

average of dynamic and static power consumptions. Power dissipation is a crucial component in the design of nanoscale CMOS circuits. The expression "Delay (Tp)" represents the average rise and fall propagation delay of D to Q transmissions.

The total relative silicon area as determined by the following equation (1):

$$A_T = \sum_{i=1}^{n} L_n(i) \times W_n(i) + \sum_{i=1}^{p} L_p(i) \times W_p(i) \quad (1)$$

In the above equation, 'n' refers to the number of NMOS transistors, 'p' refers to the number of PMOS transistors, 'Ln' and 'W_n' are the length and width of the NMOS transistors used whereas 'L_p' and 'W_p' are the length and width of the PMOS transistors used. The term "PDAP" represents the product of "power , delay, and area." The term "Robustness" represents the tolerance (Tol.) and resilience (Res.) capability of the latches. Res. latches are more robust than Tol. latches since they can self-recover from SEUs.

The Latch [9] and Latch [7] have respectively the lowest and second lowest cost in terms of PDAP, since these latches consume low power, area and delay. However, both the aches are not enough robust because they cannot provide complete resilience to SEU. Among the SEU resilient latches, the HLR CG-1 consumes the highest power which is due to the presence of active feedback loop and current competitions during the transparent mode of operations. However, resilient latches HLR-CG2, RFC, SNUSH and proposed SERL consumes low power since they avoid active feedback loops and current competitions. Meanwhile, the proposed SERL latch consumes the least power which is 14.27 µW to be specific. Moreover, the area of SERL latch is less than HLR-CG1, RFC and SNUSH since it has only 22 transistors.

Among all the SEU hardened latches, the RFEL and FERST exhibit the highest and second highest propagation delay, respectively, since both the latches have no direct D to Q propagation paths. However, remaining latches there is a direct D to Q propagation path exist, hence these latches are showing low transmission delay.

Due to its low power, delay and area overheads, the proposed SERL latch has the lowest PDAP among all SEU-resilient latches. Hence, the proposed latch is the most cost-effective robust latch among all the existing latches.

Furthermore, in Table II, the relative overheads of the SEU resilient latches are quantitatively compared for Power, Delay, Area, and PDAP [11], where is defined as in (2):

$$\Delta = \frac{Compared - Proposed}{Compared} \times 100\ \% \quad (2)$$

Table II shows that the proposed SERL latch typically saves 24.29% power, 12.09% time, 10.25% of area and 39.92% PDAP. Consequently, when compared to existing SEU resilient latches, the SERL latch is the lowest cost design.

V. Conclusion

Technology scaling makes semiconductor devices more prone to radiation induced soft errors such as SEUs. The existing hardened latches have the limitations in terms of robustness or cost. The simulation results verifies that proposed latch is complete resilient to SEUs. Hence it is more robust than the tolerant latches. Compared to the existing resilient latches the proposed latch has the least power and least cost in terms of PDAP value.

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