Indirect Sliding Mode Control of Proposed Non-Isolated Zeta-based Dual output converter

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***Abstract*— This article presents topology synthesis and control of a non-isolated dual output converter. The new integrated dual output converter is derived from a conventional Zeta converter. In a Dual output converter, the cross-coupling effect is unavoidable due to the presence of interacting dependable output voltage. Therefore, this article proposed an indirect sliding mode control (ISMC) to regulate both the output voltages. The Proposed ISMC employs a sliding surface function based on the inductor current error only and output voltage control can be achieved indirectly by inductor current. The inductor current reference is generated by PI controller and Voltage error. The performance of the proposed ISMC is verified in Matlab/ Simulink environment with the newly proposed Zeta-based dual output converter in terms of output voltage regulation ability under sudden changes in load resistance, input voltage and the output reference voltage.**

***Index Terms*— DC-DC converter, Dual output converter, Sliding mode control (SMC), small-signal analysis, Zeta converter.**

I. INTRODUCTION

Now-a days, multiport dc-dc converters are more popular in various applications like portable devices [1], electric vehicles chargers [2], LED drives [3], etc. In general, multiple output dc-dc converters are used to supply different loads with different voltage level. For obtaining N- output voltage N number of dc-dc converter required, which is increased component count by N times and increased losses of the system. The former unit has a higher cost, lesser efficiency and achieving centralized control is difficult due to multiple stages of conversion.

The above-mentioned problem can be solved by using a (Single input multiple output) SIMO/ (single input dual output) SIDO converter shown in Fig. 1, which is an increasing research area. In comparison to multiple single-output DC-DC converters in the renewable energy system, multi-output converters have the advantages of reduced conversion stages, increased system efficiency, higher power density, centralized power management, and no communication system. [5]-[10]. The general topologies of multi-output converters are classified into two categories: isolated topologies [4][5] and non-isolated topologies [6]–[9]. Consequently, considerable research has been done on the synthesis and derivation of topologies for non-isolated multioutput converters. Because there are so many devices, the former topologies are not compact and have a low power density. With a non-isolated multi-output converter [6]-[9], a wide operating range, high efficiency, and high step-up ratio are achieved.

Several control methods have been adopted in the literature with operating conditions and load variations [10]. The objective of a well-designed controller includes being able to respond quickly to changes in input parameters, being robust to parameter changes, assuring stability, and determining tracking performance from the input voltage and load fluctuations. There have been several different nonlinear control approaches proposed to achieve these objectives for the Cuk converters, including backstepping, passivity-based control [1], fuzzy logic [11], and sliding mode control (SMC) [12], [13].

SIDO converter is a highly effective method to satisfy the aforementioned control objectives owing to its excellent performance. However, the existing SMC approaches are hindered by a lack of a control design methodology and complexity, regardless of their significant advantages. As presented in [14], the sliding surface function is formed by linearly combining input current and output voltage errors with suitable constants and integrating these errors. A calculation of input current reference and four constants are eventually required by this method. However, no information is available to determine how these constants should be selected or how they should be computed for multi-output converter.

The article proposes an indirect SMC method for dc-dc Zeta based SIDO converters. Unlike traditional SMC methods, the sliding surface functions are derived from inductor current errors only without a sliding constant. As a result, sliding constants are not necessary for the sliding surface function. Furthermore, the output voltage control can be indirectly controlled by the sliding surface function.

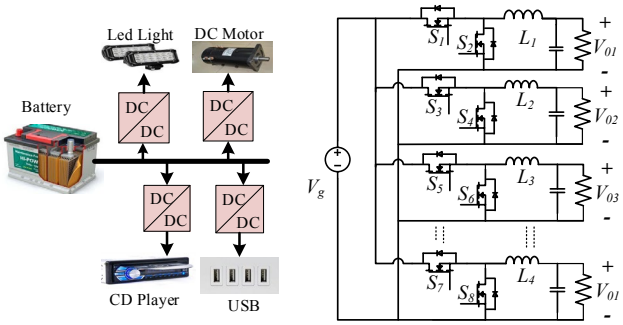


Fig. 1. (a) Block diagram of DC microgrids with two separate DC-DC Cuk converters. (b) Proposed NI-TPCC.

This paper is synthesis Zeta based SIDO converter topology and indirect sliding mode control with two output voltages. The key contributions of this paper are as follows.

- The proposed Zeta based dual output topology includes two switches. Hence, the converter incurred reduced switching losses with increased power density.
- An indirect SMC with simplified sliding surface based on the input current error is used for Zeta based Dual output converter.

II. PROPOSED CONVERTER STRUCTURE

In this section, the proposed converter has been synthesized from a Zeta converter, which can be explained as follows,

Step 1: The diodes D_1 are replaced by a switch S_2, as shown in fig 2 (b). In this figure, it can be seen that it is similar to a

synchronous Zeta converter, where all the switches are operated by separate gate pulses.

Step 2: An extra diode D_3 is added in series with the switch S_2 as shown in fig 2(c). So that the operating principle is the same as a Zeta converter.

Step 3: As shown in Fig. 2(d), the extra load is connected along with a capacitor and an inductor across the diode D_3. Then the circuit can produce a single-stage SIDO converter. Similarly, an n-port Zeta-based single-input multi-output (SIMO) converter can be synthesized from a conventional Zeta converter.

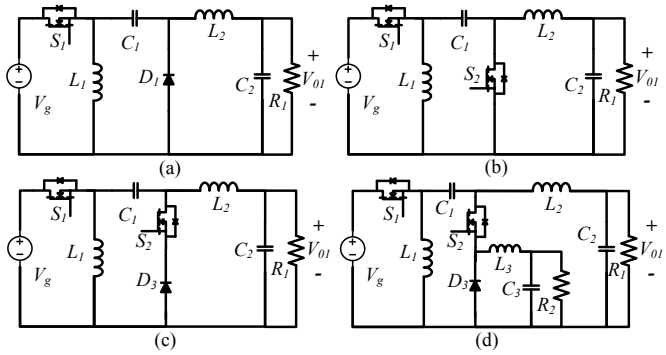


Fig. 2. Synthesis of Zeta based SIDO converter

The circuit configuration of the Zeta based SIDO converter is presented in Fig. 2(d). The converter has two output ports connected with different loads and different voltage levels. The output port voltages V_{01} and V_{02} are controlled by controlling the duty of switches S_1, and S_2. The output port is incorporated with low pass filters $L_2 - C_2$ and $L_3 - C_3$ to improve output voltage quality. The capacitor C_1 is a coupled capacitor between input and output port. In this paper, the duty cycle of switches S_1, and S_2 are D_{S1},and D_{S2} respectively.

III. Operation of the Zeta based SIDO Converter

This section detail demonstrates the power electronics circuitry and operation of the Zeta based SIDO Converter. The switches S_1 and S_2 are operated with the gate pulse G_{S1} and G_{S2} respectively. The equivalent circuit of different sub-intervals is shown in Fig.3. Fig 4 shows the steady-state waveforms of gate pulses and inductor currents i_{L1}, i_{L2} and i_{L3}. T_S is the switching period of the converter. Depending upon the switching condition, the total switching period T_S is divided into three sub-intervals.

Sub-interval-1 ($0 < t < (1 - D_{S2})T_S$) :

During this mode, the switch S_1 is On, and the switch S_2 is Off. The Diode D_1 gets forward biased. The inductors L_1 and L_2, and the capacitor C_1 get charged by the input voltage and store energy. The inductor L_3 and the capacitors C_2 and C_3 supply energy to the load and discharge. The voltage across the inductors are given by

$$V_{L1} = V_g, V_{L2} = V_g - V_{C1} - V_{01} \text{ and } V_{L3} = -V_{02}. \quad (1)$$

Sub-interval-2 ($(1 - D_{S2})T_S < t < D_{S1}T_S$) :

The switch S_1 is off and S_2 is On during this period. The diode D_1 remains in forward biased. The inductors L_1 and L_2, and the capacitor C_1 release the energy stored during the previous sub-interval and charges the capacitor C_2 as well as supplies energy to the load R_{01}.The inductor L_3 discharges the stored energy, and this energy is transferred to both load R_{02} and the capacitor C_3. The voltage across the Inductors are given by

$$V_{L1} = V_g \text{ , } V_{L2} = V_g - V_{C1} - V_{01} \text{ and } V_{L3} = V_g - V_{C1} - V_{02}. \quad (2)$$

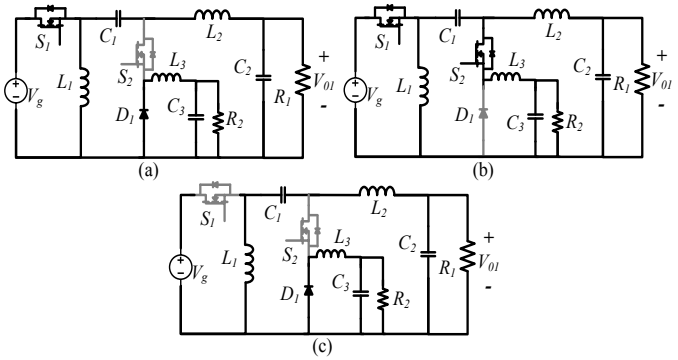


Fig. 3. Equivalent circuit of the converter during (a) Sub-interval-1 (b) Sub-interval-2 and (c) Sub-interval-3

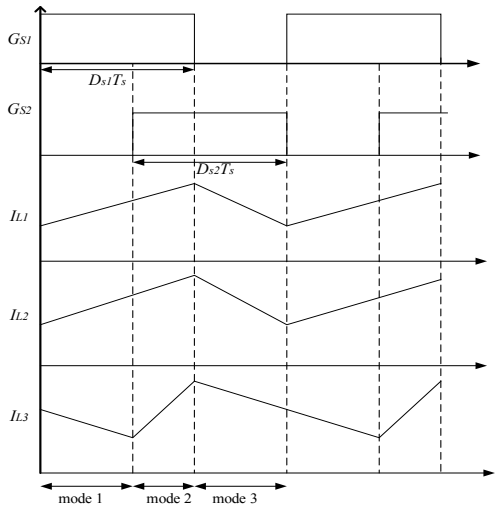


Fig. 4. Steady-State waveform of G_{S1}, G_{S2}, I_{L1}, I_{L2} and I_{L3}

Sub-interval-3 ($(1 - D_{S1})T_S < t < T_S$) :

During this sub interval, All the energy storing element except C_3 get charged by the input voltage. The capacitor C_3 supplies the stored energy to the load and discharges. The voltage across the Inductors is given by

$$V_{L1} = V_{C1} \text{ , } V_{L2} = -V_{01} \text{ and } V_{L3} = -V_{02}. \quad (3)$$

By applying volt-sec balance in inductors L_1, L_2 and L_3. The steady-state output voltage of the converter in SIDO mode is given by:

$$V_{01} = \left(\frac{D_{S1}}{1-D_{S1}}\right)V_g \quad (4)$$

$$V_{02} = \left(\frac{D_{S1}+D_{S2}-1}{1-D_{S1}}\right)V_g \quad (5)$$

IV. Small-Signal Modeling of the Converter

In this section, small-signal, AC modeling of the proposed Non-isolated three-port converter is done by State-space averaging technique Considering the following Ideal conditions. (i) Switches are ideal (ii) Series resistance of inductors is neglected (iii) Paracitics in capacitance are also neglected. Modeling is done for the SIDO converter using the state-space averaging technique for different sub-intervals.

a. *State-space equations for different sub-intervals:*

While operating the converter in SIDO mode, Inductor currents (I_{L1} , I_{L2} , I_{L3}) and capacitor voltages (V_{C1},V_{C2},V_{C3}) are considered as state variables. Input voltage (V_g) is considered as input variables. The vector representation of 'x' and 'u' are given by

$x = [I_{L1}\ I_{L2}\ I_{L3}\ V_{C1}\ V_{C2}\ V_{C3}]^T$ and $u = [V_g]$

The state-space equation for different sub-intervals are given by,

$$\dot{x} = \begin{cases} A_1 \mathrm{x} + B_1 \mathrm{u}, & 0 < \mathrm{t} < (1 - D_{S2})T_S \\ A_2 \mathrm{x} + B_2 \mathrm{u}, & (1 - D_{S2})T_S < \mathrm{t} < (1 - D_{S1} + D_{S2})T_S \\ A_3 \mathrm{x} + B_3 \mathrm{u}, & (1 - D_{S1} + D_{S2})T_S < \mathrm{t} < T_S \end{cases} \quad (6)$$

Time intervals of sub-intervals-1, 2 and 3 are $(1 - D_{S2})T_S$, $(D_{S1} + D_{S2} - 1)T_S$ and $(1 - D_{S1})T_S$ respectively where T_S is the switching period.

b. *Averaged state-space model:*

Depending upon the switching combination, the converter operates in three sub-intervals. The averaged state equation can be derived by averaging the set of equations each by the weighted time interval associated with it. The average state equation is given by,

$$\dot{x} = A_{av}x + B_{av}u \quad (7)$$

Where,

$$\begin{cases} A_{av} = A_1(1 - D_{S2}) + A_2(D_{S1} + D_{S2} - 1) + A_3(1 - D_{S1}) \\ B_{av} = B_1(1 - D_{S2}) + B_2(D_{S1} + D_{S2} - 1) + B_3(1 - D_{S1}) \end{cases}$$

Now equation (7) can be written as

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{1-D_{S1}}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-D_{S1}}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{-(D_{S1}+D_{S2}-1)}{L_3} & 0 & \frac{-1}{L_3} \\ \frac{D_{S1}-1}{C_1} & \frac{D_{S1}}{C_1} & \frac{D_{S1}+D_{S2}-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_{01}C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_{02}C_3} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} + \begin{bmatrix} \frac{D_{S1}}{L_1} \\ \frac{D_{S1}}{L_2} \\ \frac{1-D_{S1}-D_{S2}}{L_3} \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_g] \quad (8)$$

c. *Small signal perturbation and linearization:*

Linearization is required to make the matrixes linear and time-invariant. The linearized model helps in deriving different transfer functions. The small-signal perturbations are applied to the variables that appear in the averaged state-space equation. Using perturbation, the state space equation can be written as:

$$\dot{X} + \dot{\hat{x}} = [A_1(1 - D_{S2} - \widehat{d_{S2}}) + A_2(D_{S1}+D_{S2} - 1 + \widehat{d_{S2}} + \widehat{d_{S1}}) + (1 - D_{S1} - \widehat{d_{S1}})](X + \hat{x}) + [B_1(1 - D_{S2} - \widehat{d_{S2}}) + B_2(D_{S1}+D_{S2} - 1 + \widehat{d_{S2}} + \widehat{d_{S1}}) + B_3(-D_{S1} - \widehat{d_{S1}})](U + \hat{u}) \quad (9)$$

In the above equation, the DC and second-order terms can be neglected. Collecting first-order linear terms, we get,

$$\dot{\hat{x}} = A_{av}\hat{x} + B_{av}\hat{u} + \big[(A_1 - A_2)X + (B_1 - B_2)U\big]\widehat{d_{S2}} + [(A_2 - A_3)X + (B_2 - B_3)U]\widehat{d_{S1}} \quad (10)$$

Which can also be represented as

$$\dot{\hat{x}} = A_{av}\hat{x} + B_{av}\hat{u} + E_1\widehat{d_{S2}} + E_2\,\widehat{d_{S1}} \quad (11)$$

Where,

$E_1 = [(A_1 - A_2)X + (B_1 - B_2)U]$

$E_2 = [(A_2 - A_3)X + (B_2 - B_3)U]$

V. Indirect Voltage Control ZETA-Based SIDO Converter

In indirect voltage control, the output voltage is controlled indirectly by comparing the inductor current. In order to control the output voltage indirectly, we control the input current i_{l1}. We define the sliding surface functions and their derivatives as follows.

$$S_1 = i_{L1} - i_{L1}^* \quad (12)$$

$$S_2 = i_{L3} - i_{L3}^* \quad (13)$$

$$\frac{dS_1}{dt} = \frac{di_{L1}}{dt} - \frac{di_{L1}^*}{dt} \quad (14)$$

$$\frac{dS_2}{dt} = \frac{di_{L3}}{dt} - \frac{di_{L3}^*}{dt} \quad (15)$$

Where i_{L1}^* and i_{L3}^* are the reference or the required values of the input inductor currents i_{L1} and i_{L3} respectively. Which can be generated by using a proportional-Integral (PI) controller as the equation (16) and (17) [15]. The proportional and integral gain of the converter to generate the reference inductor current i_{L1}^* is k_{p1} and k_{i1} respectively. Similarly to generate reference inductor current i_{L3}^*, proportional and integral gain are k_{p3} and k_{i3} respectively.

$$i_{L1}^* = -k_{p1}x_1 - k_{i1}\int x_1 dt \quad (16)$$

$$i_{L3}^* = -k_{p3}x_3 - k_{i3}\int x_3 dt \quad (17)$$

Derivative of (16) and (17) can be written as

$$\frac{di_{L1}^*}{dt} = -k_{p1}x_2 - k_{i1}x_1 \quad (18)$$

$$\frac{di_{L3}^*}{dt} = -k_{p3}x_4 - k_{i3}x_3 \quad (19)$$

Now substituting (8) and (18) in (14)

$$\frac{dS_1}{dt} = \frac{D_{s1}v_g}{L_1} + \frac{v_{c1}(1-D_{s1})}{L_1} + k_{p1}x_2 + k_{i1}x_1 \quad (20)$$

similarly, substituting (8) and (19) in (15)

$$\frac{dS_3}{dt} = \frac{(v_g - v_{c1})(D_{S1}+D_{S2}-1)}{L_3} - \frac{v_{c3}}{L_3} + k_{p3}x_4 + k_{i3}x_3 \quad (21)$$

At the time when the system enters into the sliding mode, The system is subjected to some dynamics, and it can be obtained by equating dS/dt to 0. From (20) and (21), it can be written as

$$0 = \frac{D_{s1}v_g}{L_1} + \frac{v_{c1}(1-D_{s1})}{L_1} + k_{p1}x_2 + k_{i1}x_1 \quad (22)$$

$$0 = \frac{(v_g - v_{c1})(D_{s1}+D_{s2}-1)}{L_3} - \frac{v_{c3}}{L_3} + k_{p3}x_4 + k_{i3}x_3 \quad (23)$$

Which implies

$$\dot{x}_1 + \frac{k_{i1}}{k_{p1}}x_1 = \frac{D_{s1}(v_{c1} - v_g) - v_{c1}}{k_{p1}L_1} \quad (24)$$

$$\dot{x}_3 + \left(\frac{1 + k_{i3}L_3}{k_{p3}L_3}\right)x_3 = -\frac{(v_g - v_{c1})(D_{s1}+D_{s2}-1) + v_{out}^*}{k_{p3}L_3} \quad (25)$$

Since these are first-order differential equations, their solution can be obtained as

$$x_1(t) = \frac{1}{k_{i1}L_1}\big[D_{s1}(v_{c1} - v_g) - v_{c1}\big] + K_1 e^{-\frac{k_{i1}}{k_{p1}}t} \quad (26)$$

$$x_3(t) = \frac{1}{1+k_{i3}L_3}\big[(v_g - v_{c1})(D_{s1} + D_{s2} - 1) + v_{02}^*\big] + K_2 e^{-(\frac{1+L_3k_{i3}}{L_3k_{p3}})t} \quad (27)$$

Before the operation of the converter, the output voltages (V_{01} *and* V_{02}) is zero. Which indicates

$$x_1(0) = -v_{01}^*$$

$$x_3(0) = -v_{02}^*$$

By substituting the value of $x_1(0)$ and $x_3(0)$ in (26) and (27) respectively, the values of constants $K_1$and K_2 can be obtained as follows

$$K_1 = -v_{01}^* - \frac{1}{k_{i1}L_1}\big[D_{s1}(v_{c1} - v_g) - v_{c1}\big] \quad (28)$$

$$K_2 = -v_{02}^* - \frac{1}{1+k_{i3}L_3}\big[(v_g - v_{c1})(D_{s1} + D_{s2} - 1) + v_{02}^*\big] \quad (29)$$

The steady-state value of the first term in (26) and (27) becomes zero by substituting the steady-state value of capacitor voltages (V_{c1} *and* V_{c3}), input voltage (V_g), and Duty cycles (D_{s1} *and* D_{s2}). In order to make the closed-loop system stable, the steady-state value of $x_1(t)$ and $x_3(t)$ should be zero. This means on steady-state, the actual output voltage and the reference output voltages are equal. To make this condition satisfied, the value of the exponential term should

be zero as t→ ∞. The value of $x_1(\infty)$ and $x_3(\infty)$ will be zero if the following condition is satisfied. $\frac{k_{i1}}{k_{p1}} > 0$ and $\frac{1+L_3 k_{i3}}{L_3 k_{p3}} > 0$

The above condition can be satisfied by choosing appropriate values of the controller gains. Such as k_{i1}, k_{i3}>0, $k_{p1}k_{p3}$>0 and k_{i1}, k_{i3}<0, k_{p1}, k_{p3}<0.

Now let's define the control input as follows:

$$D_{S1} = 0.5(1 - sgn(S_1)) = \begin{cases} 1 & if\ S_1<0 \\ 0 & if\ S_1>0 \end{cases} \quad (30)$$

and

$$D_{S2} = 0.5(1 - sgn(S_2)) = \begin{cases} 1 & if\ S_2<0 \\ 0 & if\ S_2>0 \end{cases} \quad (31)$$

Where $sgn(\,)$ is the signum function whose value is either 1 or -1 depending upon the sign of S_1 or S_2. The following condition ensures that the sliding mode control is stable[13],

$$S\frac{dS}{dt} < 0 \quad (32)$$

Then using (20), (30) and (32), we can obtain the region in which the closed-loop control is stable on x_1, x_2 plane.

Case − I:

When $S_1 < 0$, $D_{S1} = 1$ so that $\frac{dS_1}{dt}$ should be greater than 0

$$l_1 = \frac{V_g}{L_1} + k_{p1}x_2 + k_{i1}x_1 > 0 \quad (33)$$

Case − II

When $S_1 > 0$,$D_{S1} = 0$ so that $\frac{dS_1}{dt}$ should be less than 0

$$l_2 = \frac{V_{c1}}{L_1} + k_{p1}x_2 + k_{i1}x_1 < 0 \quad (34)$$

(33) and (34) represent the equations of two straight lines l_1 and l_2, the boundary for the stability region of the system. The slope of both the lines is the same and equal to $-k_{i1}/k_{p1}$, Which means the lines are parallel to each other.

similarly, Using (21), (31), and (32), we can obtain the region in which the closed-loop control is stable on the x_3, x_4 plane.

$$l_3 = \frac{-v_{c3}}{L_3} + k_{p3}x_4 + k_{i3}x_3 > 0 \quad (35)$$

$$l_4 = \frac{V_{c1}-V_g-V_{c3}}{L_3} + k_{p3}x_4 + k_{i3}x_3 > 0 \quad (36)$$

According to Fig. 5, each proportional and integral gain pairs have two different stability regions. It is important to note that inductors $L_1 and\ L_3$ is involved in determining the size of the stability region. Increasing the value of inductors causes decrease in ripple current as well as reduces the stability region. y-state and transient. Conversely, if the transversality, reachability, and equivalent control conditions are also satisfied, they constitute an essential condition for a sliding motion to exist on the sliding surface [16].

$$\frac{\partial}{\partial u}\left(\frac{dS_1}{dt}\right) \neq 0 \quad (37)$$

$$\frac{\partial}{\partial u}\left(\frac{dS_2}{dt}\right) \neq 0 \quad (38)$$

Using Equations (35) and (36), we can ensure that the sliding mode dynamics of the system are governed by control input D_{S1} in $\frac{dS_1}{dt}$ and control input D_{S2} in $\frac{dS_2}{dt}$

By substituting (20) into (37) it can be easily verified the transversality condition.

$$\frac{\partial}{\partial u}\left(\frac{dS_1}{dt}\right) = \frac{-V_{c1}}{L_1} \neq 0 \quad (39)$$

similarly,

$$\frac{\partial}{\partial u}\left(\frac{dS_2}{dt}\right) = \frac{V_g - V_{c1}}{L_3} \neq 0 \quad (40)$$

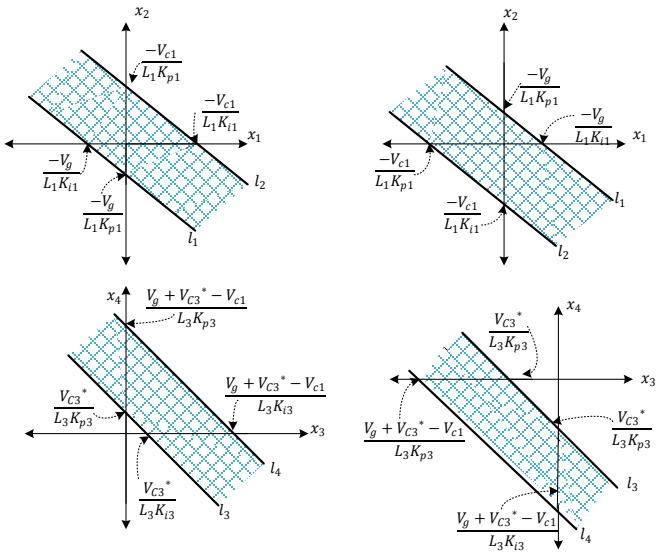


Fig. 5. Stability regions of the system with the proposed SMC method. (a) kp > 0 and ki > 0. (b) kp < 0 and ki < 0

The above condition always follows since the capacitor voltage V_{c1} is a non-zero quantity and $V_g \leq V_{c1}$.The last thing that needs to be checked to ensure the stable indirect control of the converter is to confirm that the continuous signal equivalent control input D_{S1eq} and D_{S2eq} are bounded between the minimum and maximum values of the discontinuous signal $D_{S1}$and D_{S2} respectively. For dc converters D is bounded between 0 and 1. So, proving the condition $0 < D < 1$ ensures that the control method is stable.

Proof 1:

The expression for D_{s1eq} can be obtained from (20) by substituting $\frac{dS_1}{dt} = 0$ and $x_1 = x_2 = 0$. Which results in

$$D_{s1eq} = \frac{V_{c1}-V_{in}}{V_{c1}} \quad (41)$$

Now substituting (8) and (14) in (23) we get,

$$S\left(\frac{v_g D_{S1}}{L_1} + \frac{v_{c1}(1-D_{S1})}{L_1} - \frac{di_{l_1}^*}{dt}\right) < 0$$

Substituting (30) and $S = |S|sgn(S)$ into the above expression,

$$\frac{|S|sgn(S)}{2L_1}\left[(v_{c1} + v_g) - (v_g - v_{c1})sgn(S) - 2L_1\frac{di_{l_1}^*}{dt}\right] < 0$$

Simplifying further,

$$\frac{|S|}{2L_1}\left[sgn(S)\left\{v_g + v_{c1} - 2L_1\frac{di_{l_1}^*}{dt}\right\} - (v_g - v_{c1})\right] < 0$$

The above inequality holds if the following condition is satisfied

$$\left|v_g + v_{c1} - 2L_1\frac{di_{l_1}^*}{dt}\right| < v_g - v_{c1} \quad (42)$$

During steady-state, since $i_{l_1}^*$ is constant, $\frac{di_{l_1}^*}{dt} = 0$. Hence (42) can be written as

$$v_{c1} - v_g < v_g + v_{c1} < v_g - v_{c1} \quad (43)$$

Adding, $(v_{c1} - v_g)$ to the inequality and then dividing the resulting equation by 2. We get,

$$(v_{c1} - v_g) < v_{c1} < 0 \quad (44)$$

Dividing (44) by $v_{c1} - v_g$ and rearranging the above expression. We get,

$$1 > \frac{V_{c1}}{V_{c1}-V_g} > 0 \qquad [\because (v_{c1} - v_g) < 0] \quad (45)$$

Substituting (40) in (45) and rearranging we get,

$$0 < D_{eq1} < 1$$

This completes the proof that D_{eq1} is bounded between 0 and 1.

Proof 2:

The expression for D_{s2eq} can be obtained from (21) by substituting $\frac{ds_2}{dt} = 0$ and $x_3 = x_4 = 0$. Which results in

$$D_{s2eq} = \frac{V_g + V_{C3}}{V_g - V_{C3}} \quad (46)$$

Now substituting (8) and (14) in (23) we get,

$$S_2\left(\frac{(v_g - v_{c1})(D_{S1} + D_{S2} - 1)}{L_3} + \frac{v_{c3}}{L_3} - \frac{di_{l3}^*}{dt}\right) < 0$$

Substituting (31) and $S_2 = |S_2|sgn(S_2)$ into the above expression,

$$\frac{|S_2|sgn(S_2)}{2L_3}\left[(-v_g - v_{c1} - 2v_{c3}) - (v_g - v_{c1})sgn(S_2) - 2L_3\frac{di_{l3}^*}{dt}\right] < 0$$

Simplifying further,

$$\frac{|S|}{2L_3}\left[sgn(S)\left\{(-v_g - v_{c1} - 2v_{c3}) - 2L_3\frac{di_{l3}^*}{dt}\right\} - (v_g - v_{c1})\right] < 0 \quad (47)$$

The above inequality holds if the following condition is satisfied

$$\left|-v_g - v_{c1} - 2v_{c3} - 2L_3\frac{di_{l3}^*}{dt}\right| < v_g - v_{c1} \quad (48)$$

During steady-state, since i_{l1}^* is constant, $\frac{di_{l3}^*}{dt} = 0$. Hence (48) can be written as

$$v_{c1} - v_g < -v_g - v_{c1} - 2v_{c3} < v_g - v_{c1} \quad (49)$$

Adding, $(v_{c1} - v_g)$ to the inequality and then dividing the resulting equation by 2. We get,

$$2(v_{c1} - v_g) < -2v_g - 2v_{c3} < 0 \quad (50)$$

Dividing (32) by $-2(v_g - v_{c1})$ and rearranging the above expression. We get,

$$1 > \frac{v_g + v_{c3}}{v_g - v_{c1}} > 0 \quad (51)$$

Substituting (28) in (34) and rearranging we get,

$$0 < D_{s2eq} < 1$$

This completes the proof that D_{s2eq} is bounded between 0 and 1.

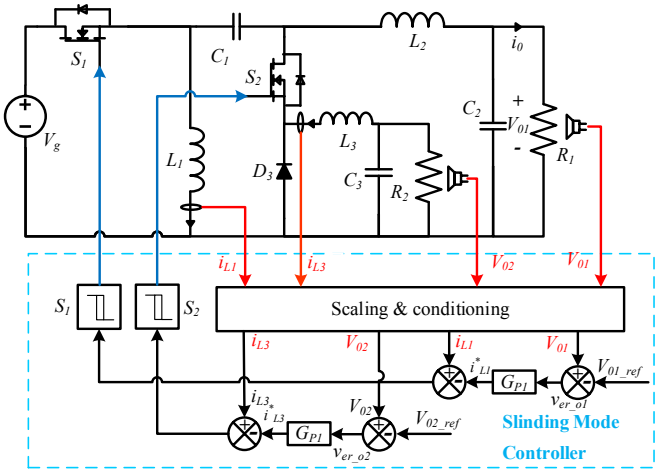


Fig.6. Block diagram of control architecture of ISMC

VI. Simulation Results

The numerical simulation verifies the theoretical considerations of the zeta-based SIDO converter in the MATLAB/Simulink environment. The converter has been simulated with a purely resistive load (25 Ω and 15 Ω) and a 30 V input voltage. The simulation control parameters used are summarised in Table I. The performance of the proposed ISMC for dual output converter is tested in terms of voltage regulation under variable input voltage, and the effect on output voltage when another load changes.

TABLE I

Control Parameters

Description	Value
Hysteresis band (h)	-0.12/+0.12
Sampling time (T_S)	10µs
Switching frequency (f_S)	10 kHz
$K_{P1}, K_{I1}, K_{P3}, K_{I3}$	0.2,60,0.35,40

1) *Steady-State Performance:*

The steady-state performance of the converter is presented in Fig. 7. The figure presents the steady-state performance of Zeta based SIDO converter of input voltage(V_g), output voltage (V_{01}, V_{02}) and output current (i_{01}, i_{02}). The two output voltages follow their set reference voltages efficiently. The corresponding switch voltages and currents in steady-state conditions are also illustrated in Fig. 7.

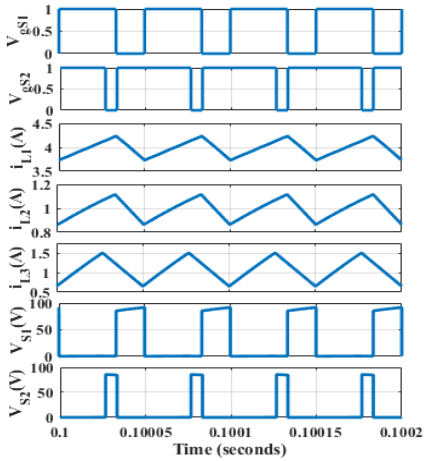


Fig. 7 Verification of steady-state voltage and current waveform of SIDO-CC

2) *Performance under input voltage variations*

In this case, the robustness of the proposed ISMC over dual output converter is depicted in Fig.8. Fig.8 shows the transient response of both the output voltages (V_{01}, V_{02}) and currents (i_{01}, i_{02}), when input voltage V_g changes from 30 V to 24 V at 0.1 s. Initially, the converter is operating under a steady-state condition with V_g = 30 V. when input voltage changes, the output voltages regulate their respective reference voltages with negligible overshoot and settle in mili second. The overshoot in V_{01} and V_{02} is found to be 0.6 V, 0.5 V, respectively.

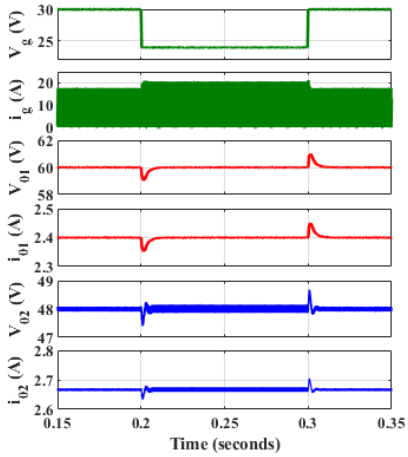
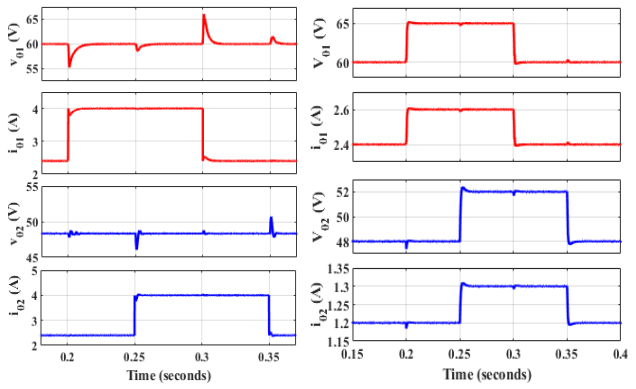


Fig. 8. Transient response of the converter during input voltage V_g change from 30V to 24V at 0.1 s.



(a) (b)

Fig.9. Transient response of converter **(a)** during Load-1(R_1) changed from 25 Ω to 15 Ω at 0.2 s and Load-2 (R_2) changed from 20 Ω to 12 Ω at 0.25s. **(b)** during voltage reference change. V_{ref1} changed from 60V to 65 V at 0.2 s and from 65 V to 60V at 0.3 s. V_{ref2} changed from 48 V to 52 V at 0.25 s and from 52 V to 48 V at 0.35s.

3) *Performance under load variations*

In this case, the effect of the proposed ISMC is verified by changing the output load. Fig.9(a) shows the transient responses of the output voltages and currents for an abrupt change in the load resistance of port-1 and port-2. The port-1 load is changed from 25 Ω to 15 Ω at 0.2 s and port-2 is changed from 20 Ω to 12 Ω at 0.25 s. The port-1 and port-2 output current i_{01} and i_{02} change accordingly with the change in load. Due to port-1 load change, the output voltage V_{01} dipped 4 V and settled in 20 ms. However, negligible effect on the port-2 voltage and current, as shown in Fig 9(a). Similarly, when Port-2 load changes, the output voltage V_{02} suffers a dip of 2 V due to port-2 load change and settles in 30 ms. However, a minor effect on port-1 voltage and current.

4) *Performance under reference voltage variations*

To verify the effect on reference voltage change of the output port of the converter output port with ISMC, a test with a step-change in reference voltage is done, and simulation results of output voltage and current are shown in Fig. 9(b). The load resistance at port-1 and 2 remains the same as before. The output voltage reference V_{ref1} is changed from 60 V to 65 V at 0.2 s and from 65 V to 60 V at 0.3 s. The output voltage V_{01} follows the reference voltage and settles in 30 ms. The change in V_{ref1} resulted in a negligible change in output voltage V_{02}. In this case, V_{02} has an overshoot of 0.6 V as shown in Fig. 9(b). Similarly, the change in V_{ref2} is changed from 48 V to 55 V at 0.25 s and from 55 V to 48V at 0.35 s. The output voltage V_{02} follows the reference voltage and settle in 20 ms. Similarly, the change in V_{ref2} has a negligible impact on V_{01} with an overshoot of 0.3 V, as depicted in Fig. 9(b). This means that the proposed ISMC algorithm is much faster and settles the output voltage with their respective reference voltage effectively.

VII. Conclusion

A novel Non-Isolated Zeta-based dual output converter has been synthesized, modelled and presented in this article. Comparing the proposed topology to the existing one, the proposed topology is observed to have a lower device count and a better efficiency. A more flexible multi-output converter is achieved as a number of output-port with different voltage levels can be obtained from a single input. In addition, the single-stage power conversion topology offers a better solution for connecting with the utility grid. The sliding surface functions are derived from inductor current errors only without a sliding constant. As a result, sliding constants are not necessary for the sliding surface function, which simplifies the controller design of the converter. The simulation results validate the functionality of the proposed controller under different load demands and different input voltage levels.

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