# Comparative Evaluation and Analysis of Different Switching Schemes for a Three-Phase Symmetrical Multilevel Inverter with Reduced Switch Count

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***Abstract*—Nowadays, multilevel inverters (MLIs) are receiving profound attention to cater the power requirements of industry 4.0. In this context, newer MLI topologies are being explored as well as proposed with reduced component counts to attain higher levels of output voltage. In this context, this article illustrates the comparative analysis of sinusoidal pulse width modulation (SPWM) with two different carrier wave and low frequency modulation (LFM) for a 3-phase symmetrical modular multilevel inverter (M-MLI) with reduced component counts. Since, this topography is uncomplicated and modular, it could be extended to several levels by rising the number of cells. The M-MLI topology having 3-levels in each pole with a single fundamental cell in each phase is simulated in MATLAB/Simulink. The %THD of M-MLI using LFM scheme is found less compared to other two techniques which are demonstrated through FFT analysis.**

***Index Terms*—Low frequency modulation, Modular Multilevel Inverter, Sinusoidal pulse width modulation, Symmetrical topology.**

## I. Introduction

The concept of multilevel inverters (MLIs) is first introduced in early 1980s. Due to fast evolution of power electronics, the development of MLIs as an lucrative and efficient solution for higher power/medium voltage DC-AC conversion has garnered more attention [1], [2]. MLIs offer several advantages in comparison to a two-level traditional inverters [3] such as (a) it exhibits staircase/stepped waveform which offers better power quality and harmonic profile minimizing the filter size and even eliminated in some cases, (b) the problems related with electromagnetic compatibility and dv/dt stress is lowered as the no. of steps or levels are increased, (c) the common mode voltage obtained is lesser, (d) modulation in MLIs can be done with both fundamental frequency as well as high frequency switching schemes, (e) It also provides more degrees of freedom to the controller. Several MLI architectures are illustrated in the literature [4], [5], [6]. The % THD of output voltage of these converters are minimized by increasing the no. of levels. Nevertheless, the drawback is increase in switching devices and associated gate drivers count, consequently making the control framework complex and the overall system more expensive [7]. Hence, a significant issue in MLI is reduction of the component counts to achieve a cost-effective system. Many topologies have been proposed in the last decade and still continuing with the goal of reducing the aforementioned shortcomings of MLIs [8]. The reduced switch count topologies of MLIs are getting more popularity as the number of switch requirements are reduced drastically. These topologies are producing same number of levels in output waveforms with lesser number of switches and also with better efficiency. For comparing the performance of different reduced switch MLI topologies some terminologies are defined. One such term is components count per level factor. It is defined as total number of components per pole that are utilized for generating the required levels in the output voltage waveform. This is utilized in determining the elements needed to provide 1 voltage level/pole. As a result, it serves as a benchmark for illustrating how the various MLI topologies optimize their components. So, the main focus is on decreasing the value of this factor. It is critical to note that, the choice of a distinct topology is comprehensively governed by the application requirement(s) [9].

This paper illustrates comparative evaluation and analysis of different switching schemes for a 3-phase symmetrical M-MLI with minimized component count. The phase and line output voltage/current waveforms of each modulation technique are presented. The corresponding % THD of output voltage and current waveforms are also compared. Following the introduction of MLI in section I, the rest of the article is described in a sequential manner for better understanding of the readers. The system architecture along with its operation is delineated in section II. Section III explains in detail about various PWM schemes taken into account. The simulation results and comparative analysis are presented in section IV and conclusion in section V.

## II. Architecture of Symmetrical Three-Phase Multilevel Inverter

The circuit diagram delineating the generalized architecture of a symmetrical 3-phase M-MLI is shown in Fig. 1 [10]. It can be seen that each arm is made up of fundamental cells

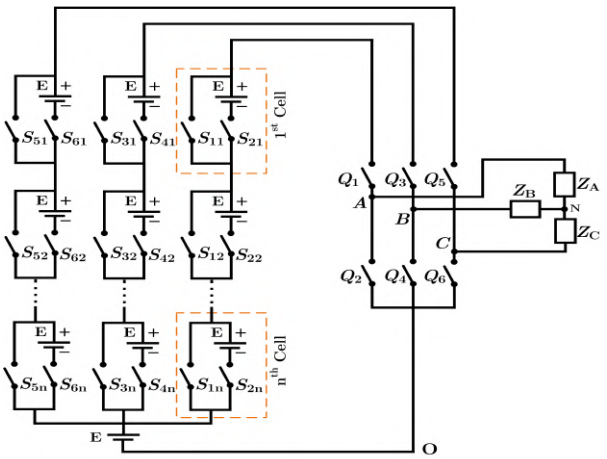


Fig. 1: Generic circuit diagram of modular MLI [10]

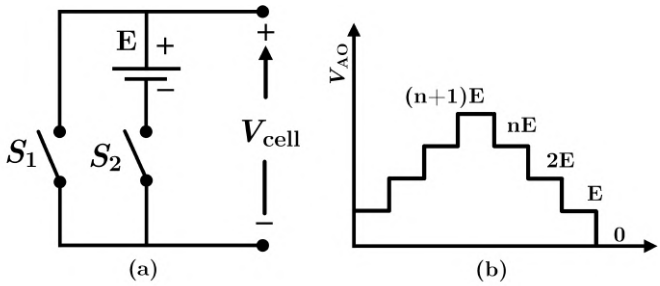


Fig. 2: (a) Basic unit of 3-phase modular MLI (b) Pole voltage corresponding to n-cell MLI

connected in series with a switch. For instance, leg $A$ is made up of a single unit/cell connected in series with switch ($Q_1$). The pole voltages ($V_{AO}, V_{BO}, V_{CO}$) are created by connecting the common DC supply ($E$) to each arm. The switch $Q_2$ is being added to obtain a zero voltage across pole $A$, in the same way $Q_4$ and $Q_6$ for other pole $B$ and $C$. The fundamental unit/cell represented in Fig. 2(a) is made up of two identical switches (namely $S_1$ and $S_2$) and a DC supply ($E$). Both switches work in tandem but the switching takes place in complementary manner. As a result, each cell generates two voltage levels i.e. zero voltage across the cell terminal when the switch $S_1$ is in ON-state, and voltage $E$ across the cell terminal when switch $S_2$ is in ON-state. Furthermore, by applying appropriate switching signals to the switches $S_1$, $S_2$, $Q_1$ and $Q_2$, 3 voltage levels in each pole (i.e., 0, $E$ and $2E$ ) are obtained by using only one cell per phase. The output for '$n$' no. of cells connected in series in terms of pole voltage is delineated in Fig. 2(b). Various switching states along with the cell voltage and pole voltage ($V_{AO}$) of M-MLI architecture is given in Table. I. This architecture can be further increased to any other required level. Various relationships of the MLI topology are shown in equations (1) – (4).

$$N_P = N_{cell} + 2 \quad (1) \qquad M_L = 2 * N_{cell} + 3 \quad (2)$$

$$N_{dc} = 3 * N_{cell} + 1 \quad (3) \qquad N_S = 3 * (2N_{cell} + 2) \quad (4)$$

where, $N_P$ is the pole voltage level, $M_L$ is the line-to-line output voltage level, $N_{dc}$ is the count of DC power supply, $N_S$ is the count of switching devices and $N_{cell}$ is the number of cells . For instance, let $N_{cell}$ = 1, then $N_P$ = 3, $M_L$ = 5, $N_{dc}$ = 4 and $N_S$ = 12.

TABLE I: Distinct switching states and their respective output voltages

| Switching States | Switch | | | | Basic Cell Voltage | Pole Voltage ($V_{AO}$) |
|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $Q_1$ | $Q_2$ | | |
| 1 | ON | OFF | ON | OFF | 0 | $E$ |
| 2 | OFF | ON | OFF | ON | $E$ | $2E$ |
| 3 | OFF | OFF | OFF | ON | $NA$ | 0 |

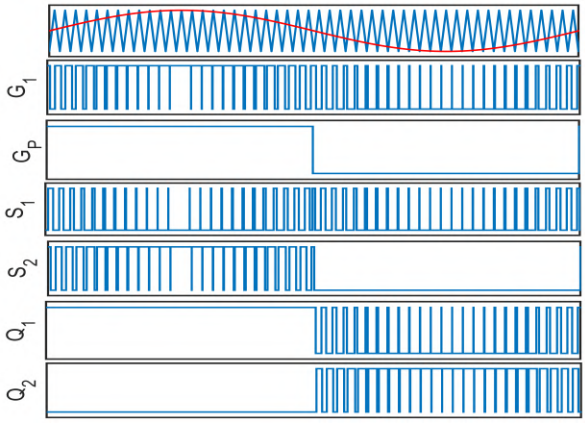


Fig. 3: Switching patterns for the simulated modular MLI using SPWM (one carrier wave)

## III. Multilevel Inverter Modulation Techniques

The M-MLI topology having 3-levels per pole in each phase with $N_{cell}$ = 1 (Fig. 1) is cosidered and the performance is analyzed. As per the switching frequency utilized to run the inverter switches, modulation approaches are basically categorized into two major groups:

- Pulse Width Modulation (PWM) techniques
- Low-Frequency Modulation (LFM) techniques

This paper examines two modulation approaches (i.e SPWM with single as well as double carrier and LFM) to generate sinusoidal output voltage waveforms, which are outlined in detail in the next subsections.

### A. SPWM Technique with One Carrier Wave

The Boolean signals necessary to synthesise the control pulses are generated by the direct comparison of a sinusoidal with a triangular signal (i.e. carrier wave). This method uses only one carrier wave having amplitude equal to modulation/reference signal's peak-to-peak value. Moreover, the carrier signal must be centered properly with reference signal for generation of switching pulses. Further, the modulation/reference signal should be DC level shifted by half the magnitude of the carrier signal as depicted in Fig. 3. The comparison of modulation signal with carrier signal gives main pulse $G_1$ and with DC level of zero value, generates $G_P$. The different switching pulses $S_1$, $S_2$, $Q_1$ and $Q_2$ usually generated

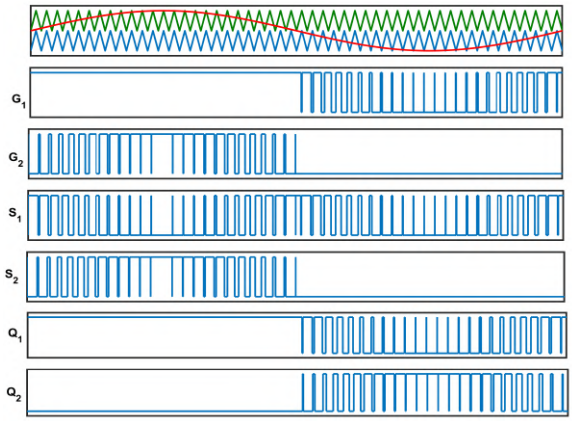


Fig. 4: Switching patterns for the simulated modular MLI using SPWM (two carrier wave)

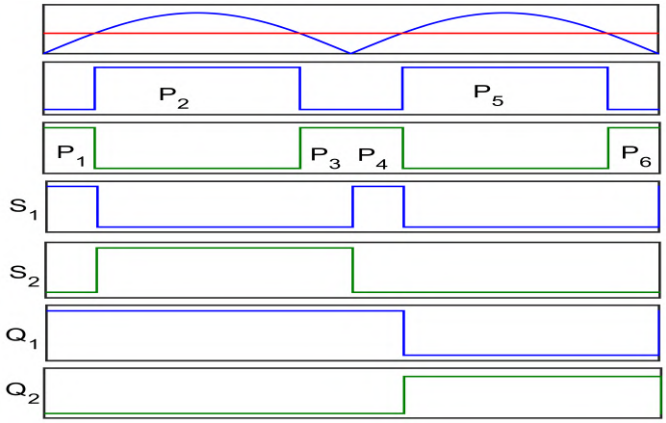


Fig. 5: LFM switching technique

by logical processing of these two obtained signals $G_1$ and $G_P$. The logical processing done to obtain switching pulses is mentioned below:

$$S_1 = (G_1 \wedge \overline{G_P}) \vee (\overline{G_1} \wedge G_P) \tag{5}$$

$$S_2 = (G_1 \wedge G_P) \tag{6}$$

$$Q_1 = G_P \vee \{(G_1 \wedge \overline{G_P}) \vee (\overline{G_1} \wedge G_P)\} \tag{7}$$

$$Q_2 = \overline{\{G_P \wedge \overline{(G_1 \wedge \overline{G_P})}\}} \tag{8}$$

where, $\wedge$, $\vee$ denotes logical AND and OR operation. To avoid the possibility of shoot through fault, a dead-period of $2\mu$s is provided in between the switching pulses of $(S_1, S_2)$ and $(Q_1, Q_2)$ repectively.

### B. SPWM Technique with Double Carrier Wave

In this method, to generate SPWM signal two identical carrier signals level shifted with respect to each other is used. The amplitude of these carrier signals are equal to peak of sinusoidal reference signal as shown in Fig. 4. It should be noted that since there are two carrier waves, so on comparing modulating signal with both these carrier signals separately generates two Boolean signals namely $G_1$ and $G_2$. The logical processing done to obtain switching pulses is mentioned below:

$$S_1 = (G_1 \wedge \overline{G_2}) \tag{9}$$

$$S_2 = G_2 \tag{10}$$

$$Q_1 = \overline{\overline{G_2} \wedge \overline{(G_1 \wedge \overline{G_2})}} \tag{11}$$

$$Q_2 = \overline{G_2} \wedge \overline{(G_1 \wedge \overline{G_2})} \tag{12}$$

### C. Low Frequency Modulation Technique

LFM technique has switching frequency usually lesser than the other modulation methods, hence also known as the fundamental modulation technique. The main advantage offered by LFM is minimization of switching losses. To generate switching pulses, a DC voltage signal is compared with a rectified sinusoidal signal with a frequency of 50 Hz and amplitude is considered as half of the peak value of the sinusoidal signal. Six different periods ($P_1$ to $P_6$) are identified at the junctions of these signals. Four switching signals ($S_1$, $S_2$, $Q_1$ and $Q_2$) are constructed based upon the combinations of these six periods ($P_1$ to $P_6$) as shown in Fig. 5.

$$S_1 = P_1 \vee P_4 \tag{13}$$

$$S_2 = P_2 \vee P_3 \tag{14}$$

$$Q_1 = P_1 \vee P_2 \vee P_3 \vee P_4 \tag{15}$$

$$Q_2 = P_5 \vee P_6 \tag{16}$$

The same logic is being used to obtain other pole voltages i.e., $V_{BO}$ and $V_{CO}$ by just giving phase shift of -120° and +120° respectively to the sinusoidal voltage.

## IV. Simulation Results and Discussion

The simulation study of modular MLI topology is carried out in MATLAB/Simulink. Here, a single cell i.e., $N_{cell}$ = 1 is selected to generate five levels of line voltage. A three-phase resistive load with LC filter is interfaced at the output side of the M-MLI. For execution of SPWM, the switching frequency ($f_s$) is selected as 10 kHz. The system parameters are: $E$ = 100 V, filter inductor ($L$) = 2 mH, filter capacitor ($C$) = 20 $\mu F$, per phase load resistance ($R_L$) = 100 Ω.The corresponding result analysis are illustrated below.

### A. SPWM using one carrier wave

The switching signals generated for $S_1$ and $S_2$ as well as $Q_1$ and $Q_2$ are complementary to each other. The concept of hybrid switching is used to generate the required pulses which also reduce the switching losses. The 3-level pole voltage of the MLI topology with SPWM with one carrier is depicted in Fig. 6(a). constitutes of total three levels. The phase voltage having 9-level and line-to-line voltage waveforms with 5-level are shown in Fig. 6(b) and (c) respectively.

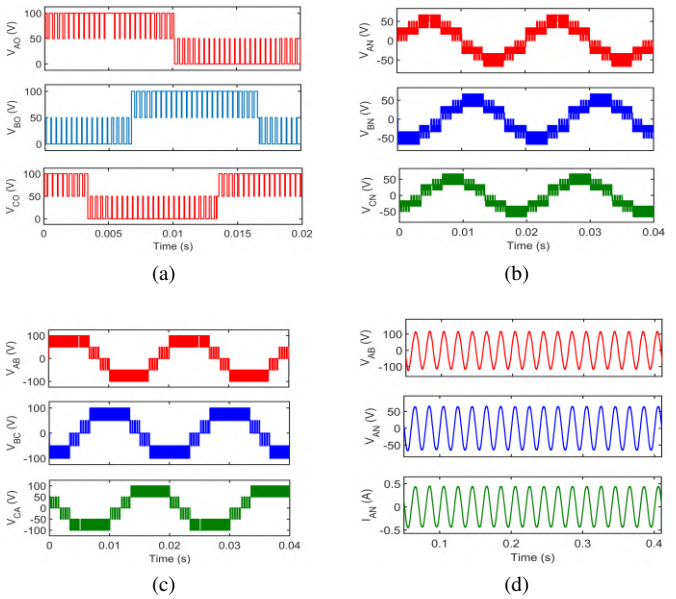


Fig. 6: Simulation results of MLI with SPWM (single carrier) (a) $V_{AO}$, $V_{BO}$ and $V_{CO}$ (b) $V_{AN}$, $V_{BN}$ and $V_{CN}$ (c) $V_{AB}$, $V_{BC}$ and $V_{CA}$ (d) output waveforms of $V_{AB}$, $V_{AN}$ and phase current ($I_{AN}$) with R load after using LC filter

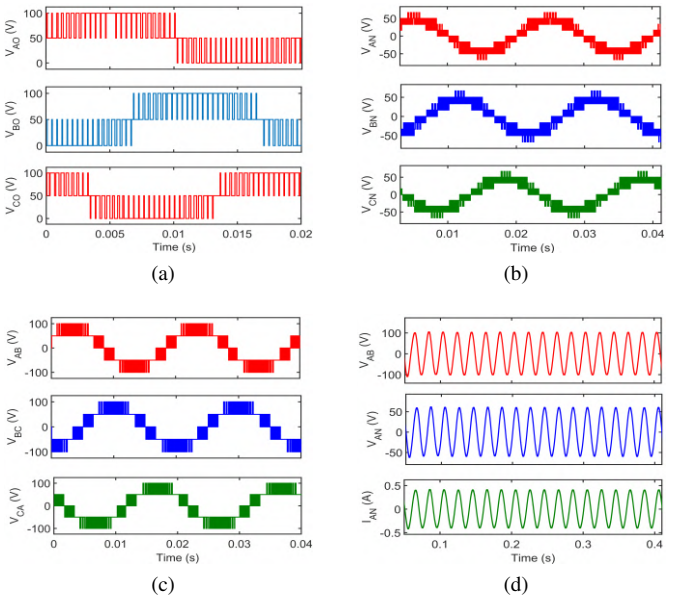


Fig. 7: Simulation results of MLI with SPWM (double carrier) (a) $V_{AO}$, $V_{BO}$ and $V_{CO}$ (b) $V_{AN}$, $V_{BN}$ and $V_{CN}$ (c) $V_{AB}$, $V_{BC}$ and $V_{CA}$ (d) output waveforms of $V_{AB}$, $V_{AN}$ and phase current ($I_{AN}$) with R load after using LC filter

### *B. SPWM using two carrier waves*

Here two carrier waves are used, so modulation index plays a crucial role in determining how many number of levels are available in output waveform of line voltages and also phase voltages [10]. For this method, the pole voltage waveform is depicted in Fig. 7(a). When modulation index is greater than 0.5 then five level are obtained in line voltages and nine level are obtained in phase voltages as depicted in Fig. 7(b) and Fig. 7(c) respectively. On the other hand, if modulation index is less than 0.5 then number of level obtained in line voltages is three and five in case of phase voltages.

### *C. Low Frequency Modulation Technique*

In this case, the most important part in generation of output voltage is the pole voltage i.e., $V_{AO}$, $V_{BO}$, $V_{CO}$. Each pole voltage has a phase shift of 120° to obtain a balanced 3-phase sinusoidal output voltage as depicted in Fig. 8(a). It can be seen that, the pole voltage waveforms have three level (i.e. $E, 0, -E$). The phase voltages having 7-level (i.e.$E, (-4/3)E, (-2/3)E, -E, 0, E, (2/3)E, (4/3)E$) are shown in Fig. 8(b). The line voltages are obtained by subtracting each pole voltage with adjoining pole voltage (i.e., $V_{AB}$= $V_{AO}$-$V_{BO}$). The line-to-line voltage waveforms have five level (i.e.$-2E, -E, 0, E, 2E$ ) (Fig. 8(c)).

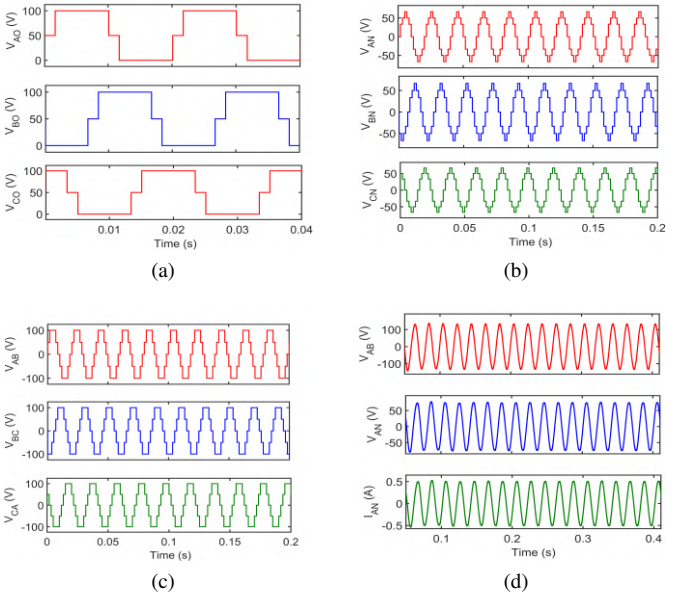


Fig. 8: Simulation results of MLI with LFM (a) $V_{AO}$, $V_{BO}$ and $V_{CO}$ (b) $V_{AN}$, $V_{BN}$ and $V_{CN}$ (c) $V_{AB}$, $V_{BC}$ and $V_{CA}$ (d) output waveforms of $V_{AB}$, $V_{AN}$ and phase current ($I_{AN}$) with R load after using LC filter

All the output waveforms after L-C filter $V_{AB}$, $V_{AN}$ and phase current ($I_{AN}$) with R load are shown in Fig. 6, 7 and 8 (d) respectively. The FFT analysis for the line voltage waveforms of both the SPWM and LFM modulation techniques are carried out before and after LC filter to determine the %THD. The FFT window along with the %THD with respect to the fundamental frequency is provided in Fig. 9 - Fig. 14 respectively for all the modulation schemes. The corresponding comparative %THD evaluation is presented in Table. II.

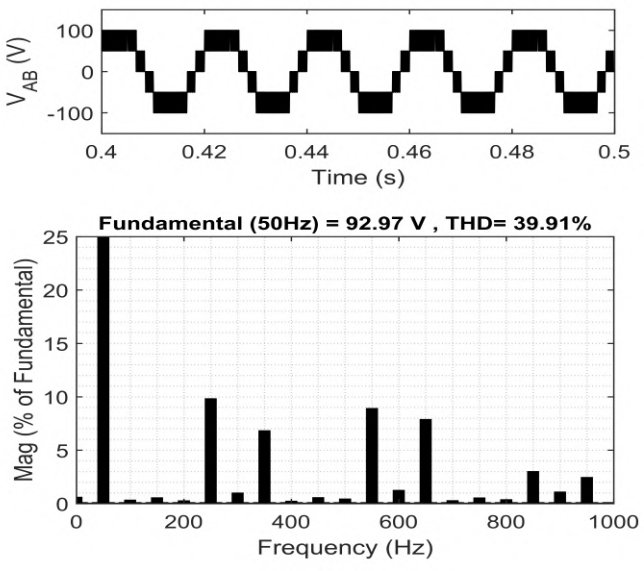


Fig. 9: FFT window of output voltage before LC filter and its %THD content for SPWM with one carrier wave

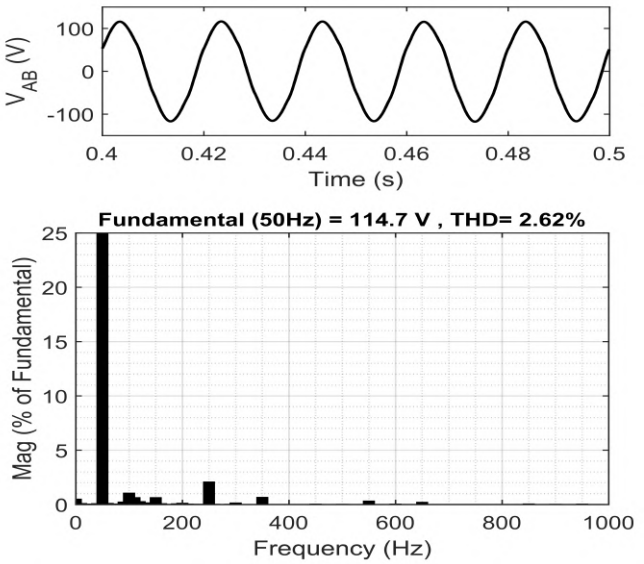


Fig. 10: FFT window of output voltage after LC filter and its %THD content for SPWM with one carrier wave

TABLE II: % THD comparison of output voltage and current waveforms of M-MLI with different PWM schemes

| Sl. No. | % THD content | SPWM with one carrier wave | SPWM with two carrier wave | Low frequency modulation |
|---|---|---|---|---|
| 1 | Output voltage (before LC filter) | 39.91 % | 36.27 % | 16.86 % |
| 2 | Output voltage (after LC filter) | 2.62 % | 1.81 % | 1.58 % |
| 3 | Output current | 2.56 % | 2.16 % | 1.82 % |

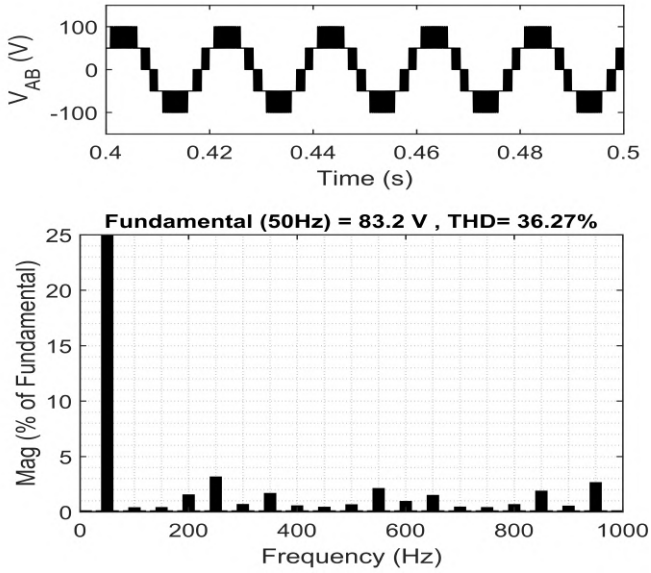


Fig. 11: FFT window of output voltage before LC filter and its %THD content for SPWM with two carrier wave

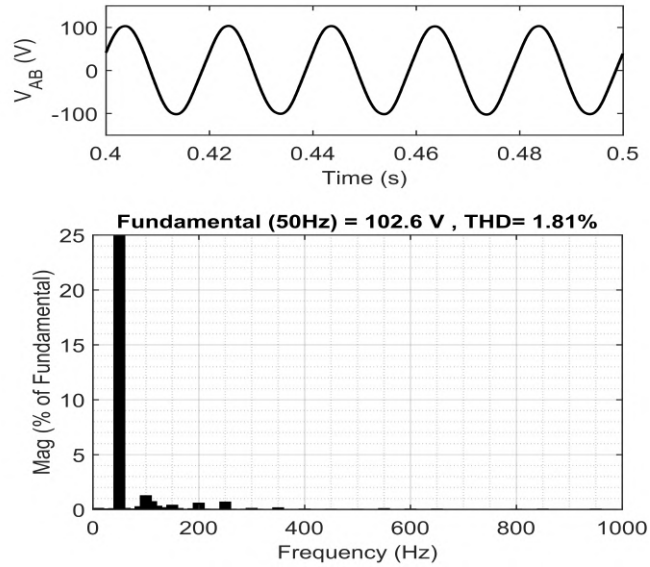


Fig. 12: FFT window of output voltage after LC filter and its %THD content for SPWM with two carrier wave

## V. Conclusion

In this article, a time-domain MATLAB simulation of reduced switch count three-phase symmetrical modular MLI topology is presented. The simulated M-MLI has several advantages such as isolated dc-power supplies, reduced number of switches. As a result, it has a simplified control algorithm, smaller inverter footprint, reduced cost, improved overall system efficiency and reliability. Apart from LFM, two SPWM approaches for controlling the MLI topology have been effectively simulated. The open loop result comparison confirms that the LFM performs better in terms of %THD reduction of

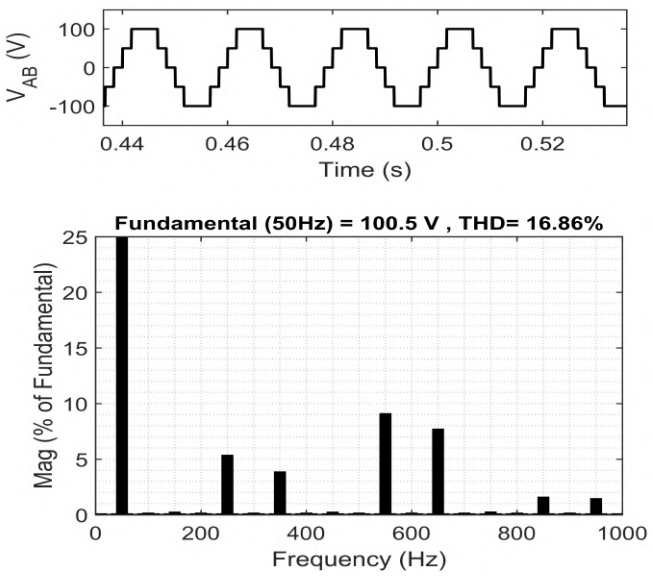


Fig. 13: FFT window of output voltage before LC filter and its %THD content for LFM technique

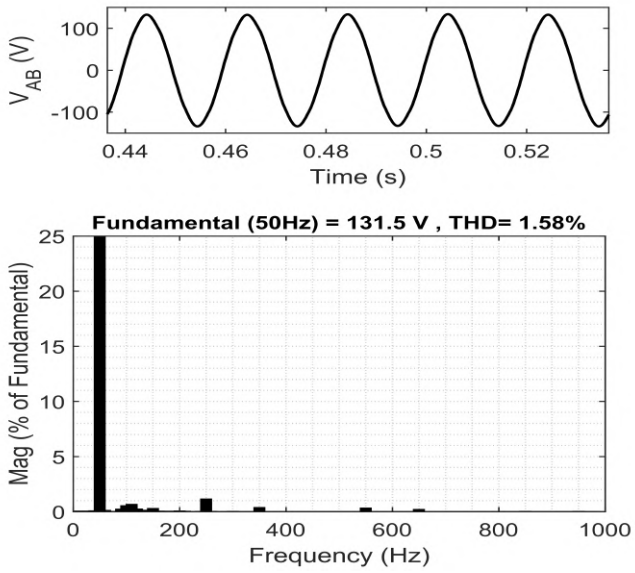


Fig. 14: FFT window of output voltage after LC filter and its %THD content for LFM technique

the MLI output voltage than other SPWM techniques. Because of the flexibility of the described topology, it can be scaled up to larger stages, resulting in improved performance issues such as low dv/dt, low EMI, and low THD, as well as the elimination of the output filter in some cases. The operation of the M-MLI with low frequency modulation scheme is found satisfactory and can be integrated in various applications such as HVDC systems, renewable power generating units and medium voltage motor drives.

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