Defect Tolerant Majority Voter Design Using Triple Transistor Redundancy

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Abstract—**In this paper, we propose a new defect tolerant majority voter based on transistor level redundancy. Majority voter chooses the winner signal with most votes and is used to select the corrected final signal in cases for fault-tolerant methods like N-tuple modular redundancy (NMR) and N-tuple interwoven redundancy (NIR). Generally the voters are assumed to be robust in nature and do not affect the design. But in practice, a fault in the voter may affect the final output of the circuit resulting in complete failure of the system. We have used new triple transistor redundancy method combined with gate level redundancy to design fault tolerant majority voter that offers very high reliability while used in conjunction with triple modular redundancy (TMR) or triple interwoven redundancy (TIR) in designing failure tolerant safety critical systems. Theoretical, as well as simulation results have been provided to prove the superiority of our design.**

Keywords- defect tolerance; majority voter; reliability; triple modular redundancy (TMR); triple transistor (TT) redundancy

I. INTRODUCTION

Fault tolerance has become essential for critical applications to increase their longevity and prohibit their sudden failures. Modern trend of device miniaturization by transistor sizing eventually lead to the increase in current density at interconnects and dielectric breakdown at gates causing in rising of the leakage current as well as the cell temperature. These phenomena makes the circuits more failure prone increasing the importance of fault tolerance. For critical applications like satellites, defence applications, nuclear reactors etc., proper functioning is of utmost necessary and hence they must be designed fault tolerant before installing.

Fault tolerance can be achieved in many ways which are broadly classified as static and dynamic. Dynamic reconfiguration [1] is mainly used in resource constrained applications having systems with structural regularity. But this method cannot tolerate intermittent or transient errors and hence is not suitable for the above mentioned applications where any temporary fault can also may lead to severe damages or even may be fatal. Hence we must opt for static methods as it is fast and robust in nature masking all sort of errors instantly.

The most popular static redundancy method is triple modular redundancy or TMR, where three identical modules are active at a time and an output majority voter determine the final result comparing the outputs from the trio. TMR is used in many critical applications till date. Now the robustness of TMR is dependent on the majority voter at the output and if it fails, TMR arrangement also fails. Works available in literature [2-4] that deal with fault tolerant voter designs having their own limitations and hence limited applicability.

In this paper, we have proposed a new fail-safe design for majority voters based on mixing of redundancy at gate level with redundancy at transistor level. We have used the triple transistor (TT) [5,6] redundancy method with triplicated gates to design the fault tolerant majority voter and call it as triple transistor voter (T2V) that offers higher reliability over the existing fault tolerant voter approaches at acceptable hardware and delay costs. The claims have been supported by theoretical analysis as well as simulation results. Use of the proposed fault tolerant majority voter in conjunction with the TMR would increase the overall reliability of the system.

In Section II of the paper, we explore the existing fault tolerant majority voter circuits and analyse their limitations that prohibit to use them in designing resource constrained reliable systems. The proposed fault tolerant majority voter based on TT is explained in Section III. In Section IV, we perform the reliability analysis of our design. In Section V, we provide the simulation results proving the efficiency of our design. Section VI concludes the paper.

II. FAULT TOLERANT MAJORITY VOTERS

Majority voters are essential whenever one have to choose single output from multiple signals generated by identical modules. It is an essential block in case of TMR and TIR (triple interwoven redundancy) for fault tolerant designs. Hence the final reliability of TMR and TIR is precisely dependent on the reliability of the output majority voter. But in most cases, the final output voter is assumed to be robust and hence the reliability of the fault tolerant design is affected. In critical applications like satellite, avionics etc., TMR is still used as primary fault tolerant method because of its simplicity and robustness and in such cases failure of output majority voters limits the reliability of the systems which is not at all favourable.

Reliability analysis of fault tolerant majority voters using compensating faults was first studied by Charles E. Stroud [2]. In [3], Kshirsagar and Patrikar have proposed a novel fault-tolerant voter circuit (NFTVC) that can tolerate any single defect affecting either at the inputs or outputs of the voter circuit. A modification of the method is simple fault tolerant digital voter circuit (SFTDVC) [4] that offers higher

reliability with simpler hardware at higher speed compared to NFTVC. Major drawback of both the methods is their limited capability of tolerating single fault occurring in the whole fault tolerant system. A Fault Tolerance Improved Majority Voter (FTIMV) has been proposed by Balasubramanian et al. [7], which helps to pave the way for improved resilience to potential internal and/or external fault(s) and has been claimed to be superior to SFTDVC. Fault tolerant voter design using TIR-QT was hinted in [8] where the voters after TIR logic were designed using quadded transistors (QT). QT offers defect tolerance by replacing each transistor of a circuit by a special arrangement of four transistors having inbuilt fault absorbent capability. Similarly one can use QT after TMR (TMR-MQT) to increase the system reliability. But these methods suffers from large delay overhead because of the use of QT logic, where four inputs are fed separately from each of the triplicated outputs of TIR/TMR. In [9], a new feedback-based complementary dual-modular redundancy (CDMR) scheme using two-stage voter circuits has been proposed. CDMR cannot mitigate the effect of hard errors arising due to manufacturing defects, ageing and other technical faults in the system. Our proposed T2V method can tolerate all sorts of defects: hard and soft, providing high reliability to the whole system. A fault tolerant voter for approximate triple modular redundancy has been proposed in [10], which requires considerably large area and delay overheads due to the quadded transistor counterpart.

III. Proposed Fault Tolerant Majority Voter

A. Fault Models

In this paper, we primarily consider different types of stuck-at faults at inputs and outputs of digital gates and transistor defects. Stuck-at faults at gate signals of a MOS can also be mapped to transistor defects and vice versa which simplify our analysis for mixing of redundancy at different levels. For example, input stuck-at-0 (s-a-0) to gate terminal of an n-MOS transistor causes in permanent open in the path between drain and source of it, which corresponds to the transistor stuck-open or stuck-off fault. Alternatively, input stuck-at-1 (s-a-1) can be mapped to transistor stuck-close (stuck-on) fault for which the drain and source of the n-MOS is shorted. In a similar fashion, input s-a-0 and s-a-1 faults at the gate terminal of a p-MOS transistor can be modelled as transistor stuck-close and stuck-open faults respectively. Our proposed structure has the capability to tolerate all sort of single as well as multiple defects depending on the target logic gates and transistors in the design.

B. The TT Logic

We have used TT logic for our fault tolerant design of the majority voter. In case of TT, each transistor of a circuit is replaced by three transistor placed in a special way as shown in Fig. 1, either like 1b or 1c [5]. Arrangement shown in Fig. 1b is preferred where probability of transistor stuck-open defect is higher and structure as in Fig 1c is used in applications with higher probability of transistor stuck-close defects.

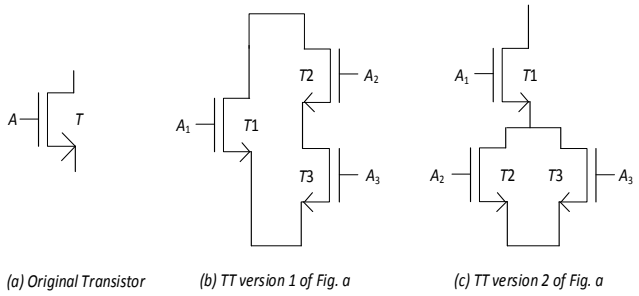

Fig. 1. Triple transistor (TT) logic

In our discussion and analysis, we consider the structure 1b assuming that probability of transistor stuck-open or input s-a-0 fault is higher. Similar derivation follows for the alternate case. In case of structure shown in Fig. 1b, if either of $A2$ or $A3$ is affected by s-a-1 or the corresponding transistor is shorted, the whole arrangement works flawlessly because of the remaining non-faulty transistors are working fine.

Alternatively, if $A1$ is at s-a-0, transistor $T1$ would be cut-off leading to stuck-open fault; but correct output is now produced by working $T2$ and $T3$. Similarly, if either of $A2$ and $A3$ is at s-a-0, T1 produces the correct output ignoring effects of the affected transistor. This arrangement produces faulty result, only when input $A1$ is at s-a-1 or $T1$ is at stuck-close defect. Now this arrangement also has the capability of tolerating two faults simultaneously. For example, if $T2$ and $T3$ both suffers stuck-open fault or $T1$ is open and either of $T2$ and $T3$ is close, the arrangement works fine producing the correct result at the final output. Similar derivations follow for Structure 1c.

C. Description of the Proposed Method

The 3:1 majority voters used at the output stage of TMR and TIR are conventionally made of two levels of NAND gates as shown in Fig. 2. In our T2V, the first level NAND gates of the majority voter are triplicated and fed from the outputs of the previous triplicated logic like TMR or TIR. The 3-i/p NAND (NAND3) gate at the second level is designed using TT logic, whose inputs are taken from the triplicated outputs of the gates at the previous level. The TT NAND3 gate at the final level of the majority voter can absorb any fault generated and propagated from the previous stage of the voter consisting of NAND2 gates.

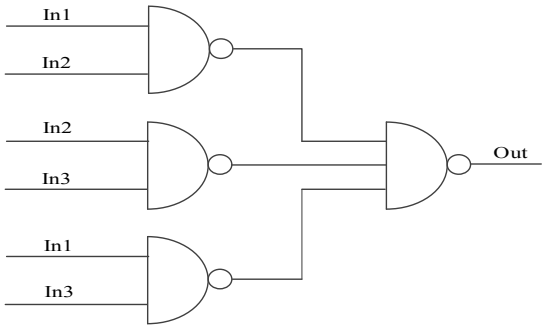

Fig. 2. NAND implementation of majority voter circuit

It also has the capability to tolerate and absorb any fault generated within itself. The multi fault tolerant capability of the TT logic [6] helps to achieve in high reliability while designing the majority voter using TT. The inputs to the last stage TT NAND3 gate are fed from three separate NAND2 gates in the previous stage, thus mitigating the problem of feeding of three separate inputs of TT from single output at previous level. This reduces the delay overhead of the circuit compared to that for the full TT structure.

The complete structure of the fault tolerant majority voter using TT logic, i.e. T2V is shown in Fig. 3. T2V is used as the last stage voter generating the final output for TMR/TIR as well as they have inbuilt fault tolerant capability, thus increasing the overall reliability.

Area of the voter circuit is triplicated in T2V and hence area overhead is increased, but the complete structure produces high reliable design compared to the normal TMR as well as other fault tolerant voter methods. For further discussion and analysis, we have considered ISCAS 85 benchmark circuit C17 [11] whose logic diagram is shown in Fig. 4. Complete TMR implementation of C17 with majority voters designed using our proposed T2V is shown in Fig. 5.

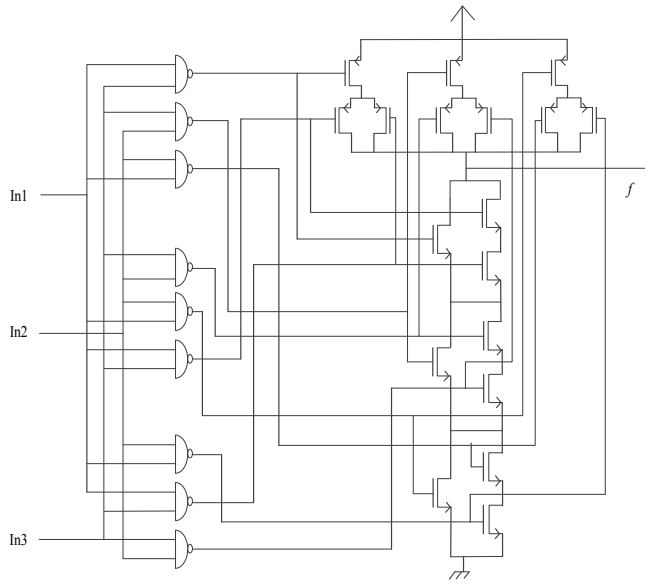

Fig. 3. Proposed triple transistor voter (T2V)

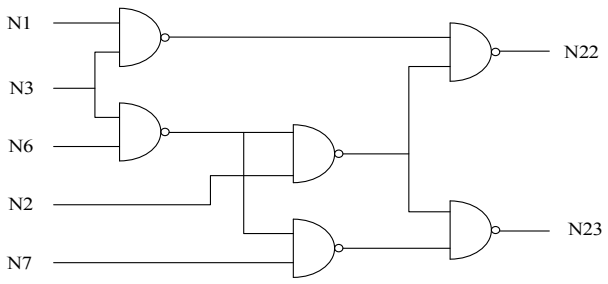

Fig. 4. Logic diagram of C17

IV. Reliability Analysis

In this section, we provide the reliability analysis of the proposed design and compare the same with that of mostly popular TMR method with traditional non-redundant voter circuit. The first stage of TMR consists of the triplicated modules, where at least two out of three identical modules must be non-faulty and the output majority voter takes care of any faulty module and provides the corrected result.

Due to the series connection of the triplicated module and the voter, reliability of the TMR structure is calculated as

$$R_{TMR} = R_{TM} \times R_{Voter} \quad (1)$$

R_{TM} and R_{Voter} represent reliabilities of three modules of TMR and that of the output majority voter respectively.

A. Reliability of T2V

At the first level of the fault tolerant T2V, each 2-i/p NAND gate is triplicated and for the fault-free operation, at least two out of three of them at each set must be non-faulty. Hence reliability of the first level of gates of the fault tolerant voter is given by

$$R_{T2V\_L1} = R^3_{NAND2\_Triple} = (3r^2_{NAND2} - 2r^3_{NAND2})^3 \quad (2)$$

, where $r_{NANDi} = r_f^{2i}$ is reliability of single i-input NAND gate and r_f is reliability of single transistor. In case of the second level of T2V, each transistor of the 3-i/p is replaced

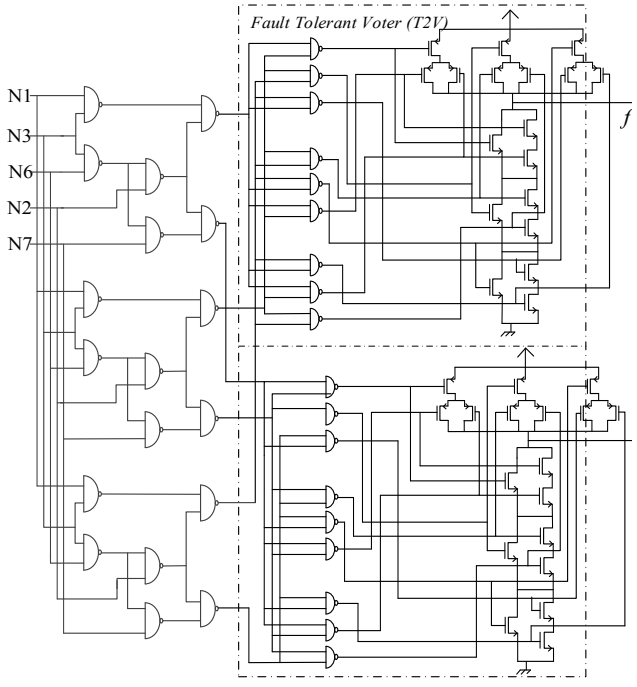

Fig. 5. TMR implementation of C17 with fault tolerant T2V

by corresponding TT structure. Hence reliability of the TT NAND3 gate at the second level of the voter is given by

$$R_{T2V\_L2}=R_{NAND3,TT}=R_{q,TT}^{6} \quad (3)$$

, where $R_{q,TT}$ is the reliability for single TT structure and has been derived in [5] as

$$R_{q,TT}=\frac{5}{4}r_f-\frac{1}{4}r_f^3 \quad (4)$$

Hence reliability of complete T2V is calculated as

$$R_{T2V}=R_{T2V\_L1}\times R_{T2V\_L2}=(3r_f^8-2r_f^{12})^3(\frac{5}{4}r_f-\frac{1}{4}r_f^3)^6 \quad (5)$$

B. Reliability of TMR with Normal Voter

The first stage of TMR consists of the triplicated modules, where at least two out of three identical modules must be non-faulty and its reliability is given by

$$R_{TM}=\{\sum_{i=2}^{3}{}^3C_i R_{module}^i(1-R_{module})^{3-i}\}=3R_{module}^2-2R_{module}^3 \quad (6)$$

, where R_{module} represents the reliability of each module in the first stage of TMR before voter. Reliability of the normal 3:1 majority voter implemented using NAND gates is given by

$$R_{voter(3:1)}=r_{NAND2}^3\times r_{NAND3} \quad (7)$$

Hence reliability of the TMR is given by

$$R_{TMR}=R_{TM}\times R_{Voter(3:1)}=(3R_{module}^2-2R_{module}^3)\times(r_f^{12}\times r_f^6) \quad (8)$$

C. Reliability of TMR with T2V

Similarly reliability of TMR with fault tolerant majority voter T2V is given by

$$R_{TMR,T2V}=(3R_{module}^2-2R_{module}^3)(3r_f^8-2r_f^{12})^3(\frac{5}{4}r_f-\frac{1}{4}r_f^3)^6 \quad (9)$$

D. Comparison for C17

C17 consists of six NAND2 gates and its reliability is

$$R_{C17}=r_{NAND2}^6=r_f^{24} \quad (10)$$

C17 has two final outputs and hence its TMR implementation has two majority voters. Hence reliability for TMR implementation of C17 is given by (using (8))

$$R_{TMR,C17}=R_{TM,C17}\times R_{Voter(3:1)}^2=r_f^{84}(3-2r_f^{24}) \quad (11)$$

Similarly from (9), reliability for TMR implementation of C17 with fault tolerant T2V is calculated as

$$\begin{aligned}R_{TMR,T2V,C17}&=R_{TM,C17}\times R_{T2V}^2\\&=r_f^{108}(3-2r_f^{24})(3-2r_f^4)^6(\frac{5-r_f^2}{4})^{12}\end{aligned} \quad (12)$$

Reliabilities for TMR implementation of C17 with and without T2V is plotted in Fig. 6. Increase in reliability in TMR with fault tolerant T2V compared to traditional unreliable voter ($R_{TMR,T2V,C17}-R_{TMR,C17}$) is also depicted in the figure. The figure shows that at $p_f = 0.015$ (approximate), the increase in reliability for the T2V voter is highest which can also be proved by differentiating (12) with respect to r_f.

V. Simulation Results

We have simulated fault tolerant designs of ISCAS 85 benchmark circuits [11] including C17 applying TMR with various fault tolerant voters in Synopsys Design Compiler using 180 nm technology. Our T2V shows highest improvement in reliability amongst them.

A. Area and Delay Overheads

We have simulated the circuit C17 applying TMR with various fault tolerant voter methods using UMC 180 nm standard cell library in Synopsys Design Compiler. The area and delay overhead results are summarized in Table I. The table shows that the proposed method has comparable area and delay overheads with NFTVC and SFTDVC and requires lesser hardware and delay compared to TMR-MQT. Newly proposed CDMR is much better in terms of cost overhead with respect to proposed T2V technique, but CDMR can tolerate only soft errors and provides low reliability in case of hard errors.

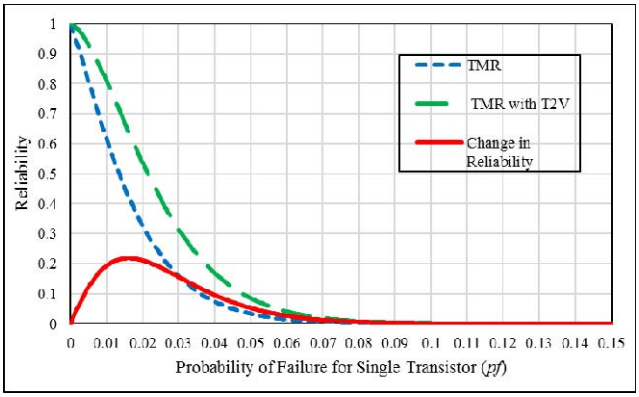

Fig. 6. Comparison of reliabilities with and without T2V for TMR implementation of C17

Table I. AREA AND DELAY COMPARISON FOR C17 *

TMR of C17 with voter	Area (in μm^2)	% Increase in Area	Critical path (in ns)	% Increase in Critical Path
without FT	265.21	350.42	0.35	75
TMR-MQT	499.23	747.88	0.72	260
NFTVC	399.9	579.18	0.55	175
SFTDVC	381.7	548.26	0.51	120
CDMR	177.25	201.04	0.34	70
Proposed T2V	**400.4**	**580.03**	**0.55**	**175**

** in UMC 180 nm technology*

To support the observations in Table I, we have considered some more ISCAS 85 benchmark circuits [11] with various complexities and the results of area and critical paths are plotted in Figs. 7 and 8 respectively. Fig. 7 shows that T2V, in general, requires more area overhead compared to other techniques except TMR-MQT. For most of the cases, its area overhead is also comparable with that for NFTVC. Fig. 8 shows that with few exceptions, T2V method requires least critical path among the others. With the increase in circuit size and less number of output voters our T2V method outperforms. Thus our proposed method may not be best in terms of hardware cost, but provides maximum reliability in high speed applications as depicted in the next sub-section.

B. Reliability

We have used the stochastic computational model (SCM) at transistor level [12] as well as gate level [13] wherever applicable and inject random faults to the circuits under consideration to compare the probability of failures for different fault tolerant voter designs. We have simulated the TMR structure for C17 circuit considering various fault tolerant voters using UMC 180 nm standard cell library in Synopsys Design Compiler and the failure rates are summarized in Table II. The table depicts that in case of C17, the proposed T2V offers highest reliability compared to the other fault tolerant voter methods. Failure probabilities for the same set of ISCAS 85 benchmark circuits implemented using TMR with various fault tolerant voters for fixed gate error rate p_g =0.01 are plotted in Fig. 9, which shows substantial improvement for our T2V over the other methods. TMR-MQT has less probability of failures for some circuits, but it requires very area and delay overheads making it unsuitable for practical applications. The figure also depicts that the cost efficient CDMR method has the highest probability of failures for all the circuits under consideration because of its inability to tolerate hard errors.

Table II. FAILURE RATE FOR C17 WITH FAULT TOLERANT VOTERS*

Gate Error Rate (p_g)	10^{-04}	10^{-03}	5×10^{-03}	0.01	0.1
without FT	4.5×10^{-04}	3.44×10^{-03}	0.031	0.03851	0.551
TMR-MQT	4.12×10^{-04}	4.42×10^{-03}	0.011	0.0397	0.395
NFTVC	4.12×10^{-04}	0.00457	0.02054	0.04417	0.4999
SFTDVC	4.09×10^{-04}	0.00429	0.02009	0.04415	0.4903
CDMR	4.7×10^{-04}	4.1×10^{-03}	0.044	0.052	0.601
Proposed T2V	**4.05×10^{-04}**	**0.00411**	**0.0191**	**0.0402**	**0.4327**

** in UMC 180 nm technology*

VI. CONCLUSION

This paper presents the design of a new fault tolerant majority voter T2V based on triple transistor redundancy, which increases the reliability of a majority voter at nominal increase in area and delay overheads. Our fault tolerant voter shows a good improvement in reliability while used with TMR and can be a good replacement for the non-redundant as well as other fault tolerant voters in all safety critical applications.

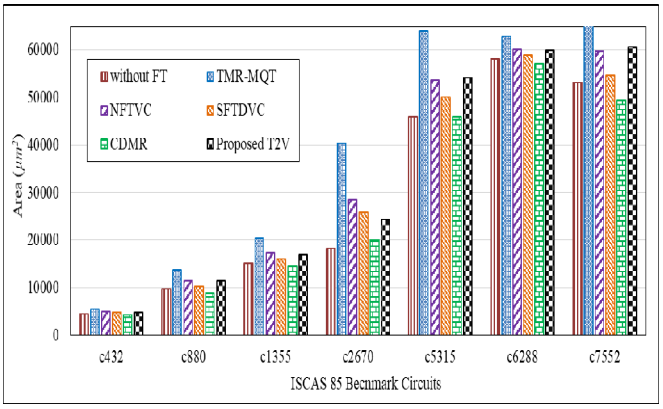

Fig. 7. Area overheads for various defect tolerant voters while used with TMR in designing reliable ISCAS 85 benchmark circuits

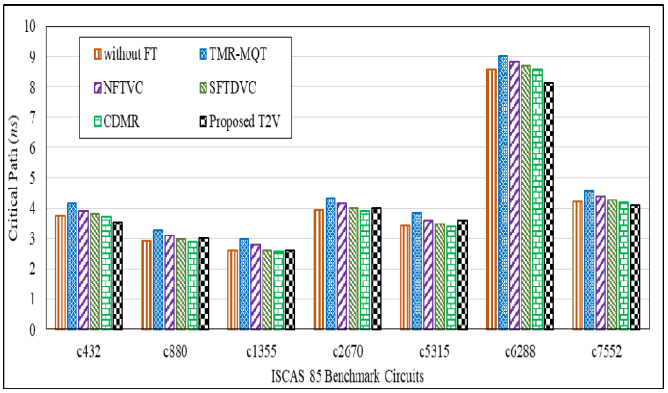

Fig. 8. Critical paths for various defect tolerant voters while used with TMR in designing reliable ISCAS 85 benchmark circuits

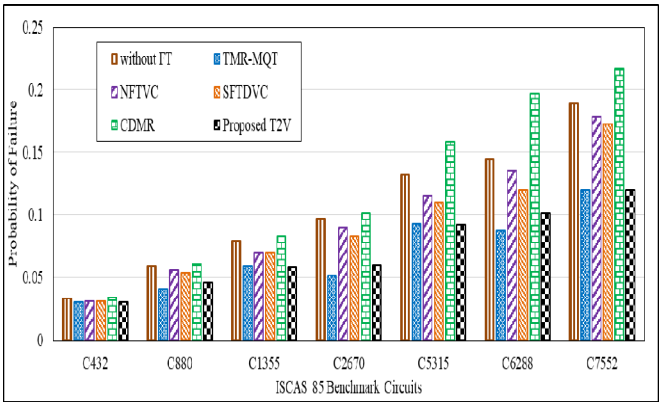

Fig. 9. Probability of failures for various defect tolerant voters while used with TMR in designing reliable ISCAS 85 benchmark circuits (p_g=0.01)

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