Modeling of Drain current and analog characteristics of dual-metal quadruple gate (DMQG) MOSFETs

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***Abstract*— This paper presents analytical modeling and simulation of output current-voltage characteristics, output conductance, and transconductance of dual metal quadruple gate (DMQG) MOSFET. With the help of above said characteristics, this work analyzes the drain current and analog characteristics dependence on device parameters such as gate length ratio and work function ratios. The results of the modeling are compared with those obtained by a 3D ATLAS device simulator to verify the accuracy of the proposed model. Finally, it is observed that the optimum performance of a fixed channel length device is possible with higher control gate length than the screen gate length.**

***Index Terms*—Quadruple Gate (QG), Dual Metal (DM), transconductance (g_m), drain conductance (g_d), control gate, screen gate**

I. INTRODUCTION

The semiconductor industry has been growing at an enormous pace over the past six decades. In the digital era, IC industry is in demand for better performance and higher device density. To meet these demands, semiconductor industries and researchers have been introduced CMOS technology boosters like hybrid orientation technology (HOT) [1], strained silicon (s-Si) technology [2,3], high-k dielectric MOSFETs [4], and gate engineering technologies [5.6], etc. However, the continuous scaling down of transistors has made the dimensions of conventional MOSFETs to nearly reach their practical limit [7]. The scaling of the conventional MOSFETs to the nano-meter regime will result in severe short-channel effects (SCEs) beyond the tolerable limit and increases standby power dissipation and deteriorate the switching characteristics of the MOSFETs and causing lower I_{on}/I_{off} ratio [7]. Therefore, the suppression of the SCEs and improvement of drain current is of vital importance to continue the MOSFET scaling and it is necessary to carry out research for the development of some alternative non-conventional MOSFET devices such as ultra-thin body silicon-on-insulator (SOI) MOSFETs [8], multiple-gate (MuG) MOSFETs [9.10], finFETs [11] and gate-all-around (GAA) MOSFETs [12] etc. Among all these non-conventional MOSFET devices, GAA MOSFET is considered to be the most promising MOS devices for future high density of IC's and these GAA MOSFETs are scaled down to deca-nanometre regime with considerable SCE's [12,13].

Multi-gate (MuG) MOSFETs offer to reduce leakage currents and high drain current due to multiple gates that suppress SCE's [14,15] and allow for further downscaling of device channel length and supply voltage. MuG MOS structures have the flexibility to control the channel by a single gate electrode. Among all the multi-gate MOSFETs, gate-all-around (GAA) MOSFET promised to be a strong contender for future low power and high-frequency application devices for its excellent electrostatic control in the channel region. In GAA MOSFETs, the gate material surrounds the channel region among all sides. GAA MOSFETs can be of quadruple and cylindrical gates. Both square/quadruple and cylindrical GAA MOSFETs are currently under research from the simulation and modeling viewpoints. The quadruple gate MOSFET has a higher current drive capability compared to cylindrical GAA MOSFETs [16]. Quadruple gate MOSFET [12-15] offers better scalability, better switching characteristics, and higher transconductance. Moreover, in cylindrical GAA MOSFETs, the performance is strongly influenced by surface roughness and interface defects due to the high surface-to-volume ratio.

In view of the above merits, quadruple gate MOSFET with dual metal gate is considered in this work and its analog characteristics are modeled and analyzed along with drain current in linear and saturation regions.

II. DEVICE STRUCTURE

Figure 1 shows the 3D device structure of the DMQG MOSFETs in x-y-z space. The channel length (L), channel width (W), and channel height (H) are represented along the z-axis, x-axis, and y-axis, respectively, as shown in Figure 1. The lightly doped Si channel is surrounded by SiO_2 of thickness t_{ox}. Over this oxide layer, two different metals with work functions $\emptyset_{m1}$ and $\emptyset_{m2}$ (where $\emptyset_{m1}$>$\emptyset_{m2}$), act as control gate and screen gate are placed side by side.

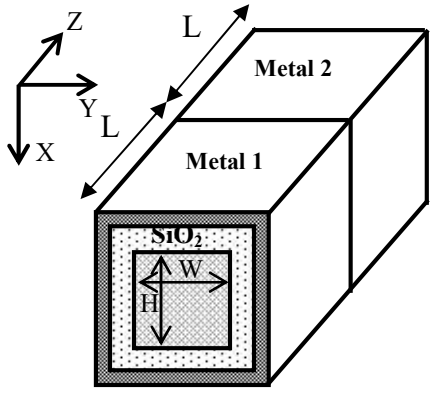

Fig.1 Schematic of a DMQG MOSFET structure in x-y-z space

III. MODELING OF DRAIN CURRENT AND ANALOG PARAMETERS

In the above threshold regime of device operation, the current-voltage characteristic is mainly dominated by drift phenomenon. The drain current in the linear region is given by [18].

$$I_D = W_{ch}\mu_{eff}Q_{inv}(z)\frac{dV(z)}{dz} \quad (1)$$

where W_{ch} is the channel width, $V(z)$ represents the channel potential along the z direction, $Q_{inv}(z)$ is the surface charge density at a point z in the strong inversion region, μ_{eff} is the effective field dependent mobility.

The inversion charges at above-threshold condition locate near the Si/SiO_2 interfaces and proportional to the total gated perimeter of the channel body. Therefore, the channel width, W_{ch} in Eq. (1) is modified to perimeter of the channel cross-section given by

$$W_{ch} = 2(W + H) \quad (2)$$

The effective field-dependent mobility μ_{eff} is given by [18]

$$\mu_{eff} = \frac{L}{(L_1/\mu_1)+(L_2/\mu_2)} \quad (3)$$

where μ_1 and μ_2 are the mobility of the charge carriers under the control gate of length L_1 and screen gate of length L_2 respectively, and is given as [18]

$$\mu_{1,2} = \frac{\mu_0}{1+\theta_{1,2}(V_{gs}-V_{th1,2})} \quad (4)$$

where $\theta_{1,2}$ are the fitting parameters, $V_{th1,2}$ are the threshold voltages for two different quadruple gate (QG) MOSFETs with gate metal work functions equal to work functions of control gate and screen gate of DMQG MOSFETs respectively. The threshold voltages V_{th1} and V_{th2} can be calculated from our previous work [17] by considering zero screen gate length ($L_2 = 0$) for V_{th1} and zero control gate length ($L_1 = 0$) for V_{th2}, μ_0 is impurity density dependence of mobility and is given as [19]

$$\mu_0 = \frac{\mu_{no}}{\sqrt{1+\left[N_a/\left(N_{ref}+(N_a/S)\right)\right]}} \quad (5)$$

where μ_{no} is the electron mobility and its value is taken to be $\mu_{no} = 677\ \mathrm{cm^2/Vs}$. The parameters N_{ref} and S involve tradeoffs between phonon and impurity scattering respectively.

The surface charge density, $Q_{inv}(z)$ is given by

$$Q_{inv}(z) = C_{ox}.\left(V_{gs} - V_{th} - V(z)\right) \quad (6)$$

where V_{th} is the threshold voltage of DMQG MOSFET [17] Substituting Eqs. (2) to (7) in Eq. (1) and integrating along the channel length, results in the following expression for the drain current in the linear region

$$I_D = \frac{2(W+H)\mu_{eff}C_{ox}\left(V_{gs}-V_{th}-(V_{ds}/2)\right)V_{ds}}{L\left(1+(V_{ds}/LE_{eff})\right)} \quad (7)$$

Now, the saturation current (I_{Dsat}) is given as

$$I_{Dsat} = W_{ch}v_{sat}Q_{invsat} \quad (8)$$

where $Q_{invsat} = C_{ox}\left(V_{gs} - V_{th} - V_{dsat}\right)$ (9)

Using Eqs. (2) and (9) in Eq. (8), the drain current at saturation region is given as

$$I_{Dsat} = 2(W + H)v_{sat}C_{ox}\left(V_{gs} - V_{th} - V_{dsat}\right) \quad (10)$$

where V_{dsat} is drain saturation voltage and it is determined by equating and solving the Eqs. (7) and (10) at $V_{ds} = V_{dsat}$ and is given as [18]

$$V_{dsat} = \frac{V_{gs}-V_{th}}{1+((V_{gs}-V_{th})/LE_{eff})} \quad (11)$$

Transconductance (g_m) is the ratio of the change in drain current (I_D) to the change in gate voltage (V_{gs}) at constant drain voltage (V_{ds}). It is given as

$$g_m = \left.\frac{\partial I_D}{\partial V_{gs}}\right|_{V_{ds}=\text{constan}} \quad (12)$$

Solving Eq. (12) using the Eq. (7), the expression for g_m in linear region is obtained as

$$g_{m,lin} = [2(W + H)C_{ox}V_{ds}]\frac{\left[\begin{array}{c}((L_1/\mu_1)+(L_2/\mu_2)+(V_{ds}/2v_{sat}))\\ -\left(V_{gs}-V_{th}-(V_{ds}/2)\right)((L_1\theta_1+L_2\theta_2)/\mu_0)\end{array}\right]}{\left((L_1/\mu_1)+(L_2/\mu_2)+(V_{ds}/2v_{sat})\right)^2} \quad (13)$$

Similarly, g_m in saturation region can be obtained by differentiating Eq. (10) with V_{gs} at constant V_{ds} and is given by

$$g_{m,sat} = 2(W + H)C_{ox}v_{sat}\left[1 - \frac{1+\left[\frac{\left((V_{gs}-V_{th})\mu_{eff}\right)^2(L_1\theta_1+L_2\theta_2)}{2\mu_0L^2v_{sat}}\right]}{\left(1+((V_{gs}-V_{th})\mu_{eff}/2Lv_{sat})\right)^2}\right] \quad (14)$$

On the other hand, drain conductance (g_d) is an important device parameter for analog circuit simulation and is defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_{ds}}\right|_{V_{gs}=\text{constan}} \quad (15)$$

Solving Eq. (15) using the Eq. (5.7), the expression for g_d in linear region is obtained as

$$g_{d,lin} = \frac{2(W+H)C_{ox}\mu_{eff}}{L}\frac{E_{eff}L(V_{gs}-V_{th}-V_{ds})}{E_{eff}L+V_{ds}} - \frac{I_D}{E_{eff}L+V_{ds}} \quad (16)$$

Similarly, g_d in saturation region can be obtained by differentiating Eq. (10) with V_{ds} at constant V_{gs} and is given by

$$g_{d,sat} = 2(W + H)v_{sat}C_{ox}\left(V_{gs} - V_{th} - 1\right) \quad (17)$$

IV. RESULTS AND DISCUSSION

In this section, I_D, g_m and g_d of DMQG MOSFET are demonstrated using developed models. These model results are compared with the numerical simulation results in linear and saturation regions for validation. Fig.2 shows the $I_D - V_{ds}$ characteristics with variation in gate voltage from 0.6 V to 1V. It is apparent from Fig. 2 that the model results are in good agreement with the simulation results in both linear and saturation regions. Fig. 3 compares the drain current of DMQG MOSFET at varying gate length ratios ($L_1{:}L_2 = 1{:}1, 1{:}2, 2{:}1$). Work functions of gates were adjusted to maintain constant threshold voltage for faithful comparison. It is evident that smaller control gate to screen gate length ratio (L_1:L_2) offers less drain current due to poor gate voltage control over channel. Moreover, weaker drain current dependence on drain voltage is observed in this case. This is due to the fact that, virtual cathode is away from the drain terminal because of small control gate length. This in turn causes very small DIBL.

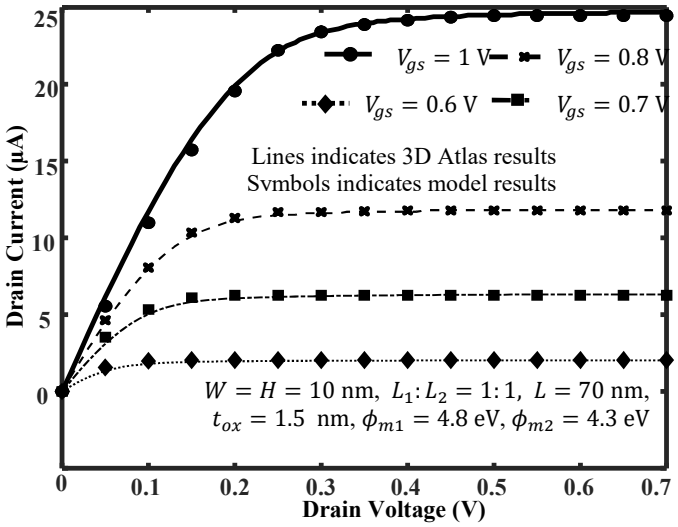

Fig. 2 $I_D - V_{DS}$ characteristics with varying gate-to-source voltages (V_{gs})

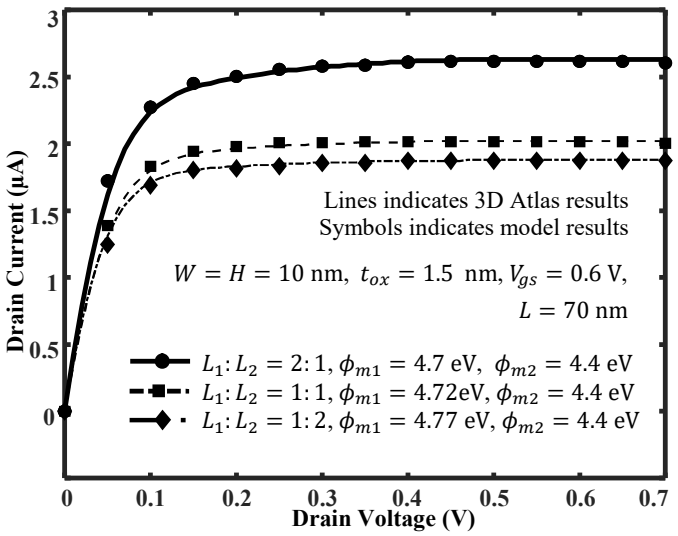

Fig.3 Variation of drain current with gate length ratio

Drain current variation with change in work function difference of control and screen gates was observed in Fig. 4. Control gate work function has been kept at a constant value ($\phi_{m1} = 4.8$ eV) and the screen gate work function (ϕ_{m2}) has been varied from 4.3 eV to 4.8 eV. It is found that saturation current increases when workfunction difference ($\phi_{m1} - \phi_{m2}$) increases from 0 eV to 0.5 eV. Drain current of single metal gate is lesser than dual metal gate. It is worth noting that, it is not possible to kept constant threshold voltage here. Fig. 5 presents the transconductance characteristic of the device with change in gate length ratios. In a device, transconductance is an efficiency of converting input small signal to output current. Highest gate length ratio (2:1) offered better trans conductance with more drain current caused by higher gate voltage control. Fig. 6 depicts the output conductance variation at different gate length ratio. It is clear from the figure that, lower gate length ratio offers less drain conductance due to poor influence of drain voltage on drain current.

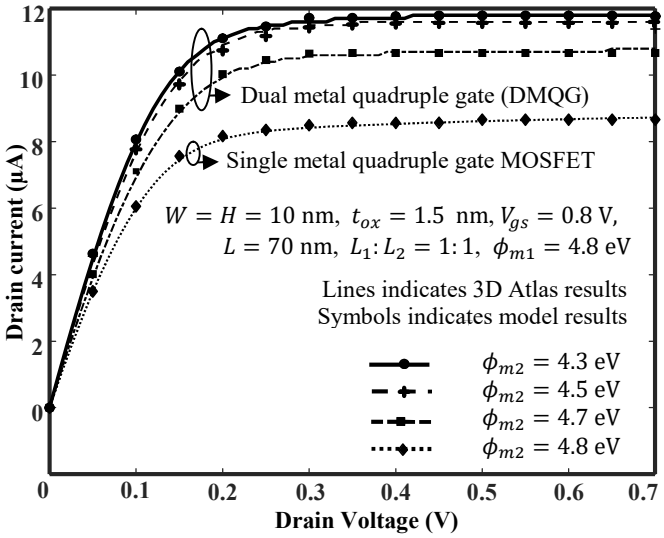

Fig.4 Drain current dependence on work function difference

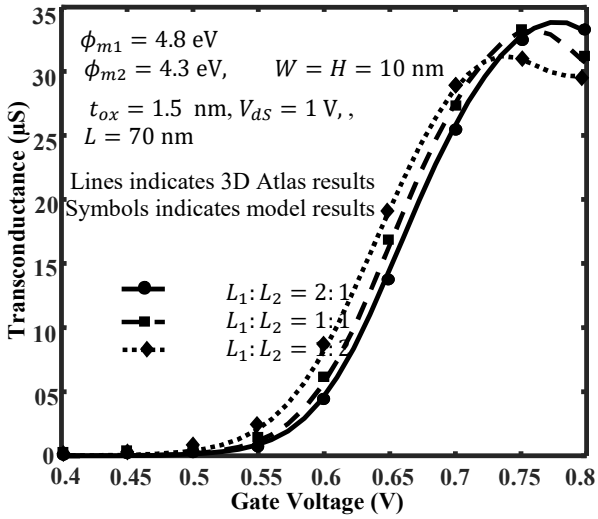

Fig.5 Transconductance behavior at different gate length ratios

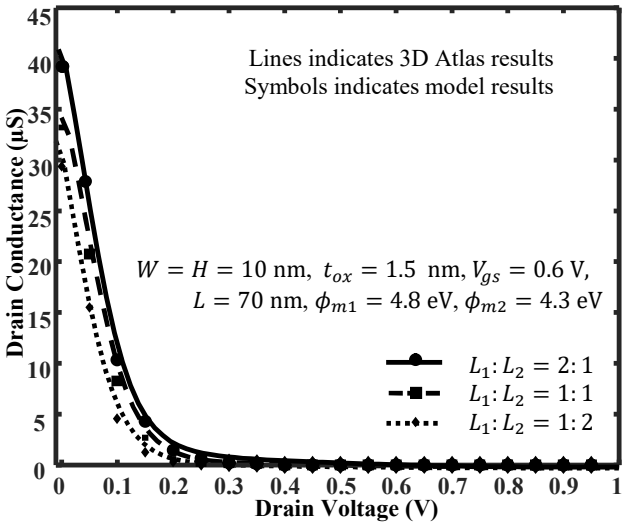

Fig. 6 Output conductance characteristics at different gate length ratios

Dependence of analog performance (I_D, g_m and g_d) on channel cross-section thickness ($W = H$), oxide thickness

(t_{ox}), and total gate length (L) is shown in table 1. Drain current is found to be increasing, when channel cross-section thickness ($W = H$) increases. A larger source-channel contact area facilitates more chargers to cross the source channel barrier resulting increased drain currents. Further, a thicker oxide resists the gate electric field entering in the channel region and thereby reduces the source channel barrier height allow to flow more charge carriers into channel region. Whereas, drain current decreases with increasing channel length as the drain electric field density reduces with increasing channel length. The transconductance (g_m) and drain conductance (g_d) also follow the similiar trend as both the analog parameters are directly proportional to the drain current. Hence, to improve the analog performance of DMQG MOSFETs, thin channel, thin gate oxide and short channel lengths are preferred; these minimum dimensions are limited by classical physics.

Table I: Impact of L , t_{ox}, and $W \times H$ on I_D, g_m and g_d for $V_{gs} = 0.8\ \text{V}/0.6\ \text{V}$

	$L = 70$ nm, $t_{ox} = 1.5$ nm	$L = 70$ nm, $W = H = 10$ nm	$W = H = 10$ nm $t_{ox} = 1.5$ nm
	$\boldsymbol{W = H}$ **(nm)** 10 12 15	$\boldsymbol{t_{ox}}$ **(nm)** 1 1.5 2	$\boldsymbol{L}$ **(nm)** 30 70 100
$\boldsymbol{I_D}$ **(μA)** $V_{gs} = 0.8$ V $V_{ds} = 1$ V	12 14.5 19.8	15 12 10.1	15.9 12 10.3
$\boldsymbol{g_m}$ **(μS)** $V_{gs} \cong 0.8$ V $V_{ds} = 1$ V	32.8 45 54	39.6 32.8 27.3	58 32.8 15
$\boldsymbol{g_d}$**(μS)** $V_{gs} = 0.6$ V $V_{ds} \cong 0$ V	34.2 48.2 61.3	38.4 34.2 30.1	44.6 34.2 29

V. CONCLUSION

A simple and efficient model is developed to understand the drain current and analog characteristics of DMQG MOSFETs. It has been demonstrated that dual metal DMQG MOSFETs shows excellent performance for analog application MOSFET devices with high control to screen gate length ratio. The drain current and analog characteristics was obtained for varying different parameters like gate length ratio, metal work function difference, channel cross-sectional area, oxide thickness and channel length. High drain current has been observed at high gate length ratio, high metal work function difference, large cross-sectional thickness with thin oxide thickness. Drain current obtained by DMQG MOSFETs is fifty percent more when compared to QG MOSFETs. The transconductance and drain conductance has shown improvement along with the drain current. The electric field at the drain can be reduced if the work function difference of the two gate metals is large and in turn it reduces the probability of hot electron injection at the drain end. The ratio of the length of the two metal gates is optimized for future generation MOS devices with sub100 nm gate lengths.

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