# Novel Threshold Voltage Model incorporating Band-To-Band Tunneling in Heterostructure p-MOSFET

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**Abstract-Threshold voltage (with and without body bias) for heterostructure pMOSFET is analytically explored as a function of applied bias for Si-$Si_xGe_{1-x}$ material system in presence of band-to-band tunneling. Threshold voltage for given device structure is calculated in the light of body effect for different structural parameters, and mole fraction of Ge is chosen as 0.28 for that operating point where 2DEG is yet to be formed, and thus making it apposite for estimating subthreshold conduction. Using this optimum structure, BTBT effect is incorporated to quantity the variation of threshold voltage over a range of source-to-gate voltages ($V_{SG}$). The results accord with available experimental data for very low and higher values of source-to-drain voltage ($V_{SD}$). Result is also computed in absence of tunneling effect, and drastic variation is observed which speaks in favor of our proposed model of subthreshold conduction which can be further extended for modeling of sub-threshold drain current characteristics of HFETs..**

***Keywords- Tunneling window, Heterostructure FET, Threshold Voltage, Structural parameters, High-K dielectric.***

## I. INTRODUCTION

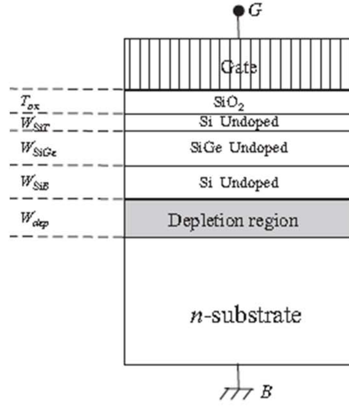
Structurally complex geometrical MOSFETs are increasingly popular these days owing to novel electronic behavior exhibited in nano-metric dimensions [1-3], despite the presence of severe short-channel effects, comparatively large power dissipation and improved subthreshold swing[4]. Several structural modifications and gate control mechanisms are reported in the literature in recent times [5-8], which not only reduce the short-channel problems, but also significantly improves the electrical performance in terms of lower leakage current, ~60 mV/decade subthreshold slope, good DIBL. The theoretical findings are well-supported by state-of-the-art fabrication technologies and processes [9-11] for experimental realization. Novel materials for substrates as well as high-K dielectrics are proposed for that purpose [12-14], and alternative material combinations are being investigated which can be used to avoid the conventional scaling techniques coupled with the advantage of higher carrier mobility. In this context, strained silicon based heterostructure devices are found to be an effective candidate for achieving the desired goal [15].

Reduction of dielectric thickness beneath the gate layer becomes extremely difficult beyond a threshold limit [16] as it enhances the probability of vertical tunneling current [17]. The same effect is observed when substrate doping is increased [18]. Henceforth, substitute materials are looked into with simultaneous satisfaction of both the requirements: higher drain current and lower threshold voltage. Strained Si based heterostructures, more precisely, Si-Ge based devices exhibit promising features [19-20] over conventional MOSFETs [21-22] with the inherent strain owing to lattice mismatch. Several research activities are being carried out on strained Si-Ge heterostructure-based MOS devices over the last decade, with the pivot being the investigation of drain current performance, precisely after pinch-off condition for application of the device in digital circuits [23].

Findings on the electrical characteristics of heterostructure MOSFETs started a decade ago when Balestra and his co-workers [24] computed subthreshold swing for ultrathin structure, followed by the study of another group calculating current in the same region [25]. Byun*et. al.*, first introduced the quantum correction model [25] for estimating the amount of charge at insulator-semiconductor interface both above and below the threshold region, whereas Balestra[24] has only taken into account the inversion conditions for drain current and threshold voltage without the 2-Dimensional Electron Gas (2-DEG) consideration. This paper focuses on that aspect of HFET, and computation is performed for threshold voltage in presence and absence of tunneling effect. Structural parameters and applied biases are tailored for highest possible leakage current, and corresponding subthreshold slope is calculated. Simulated findings are compared with published literatures, and significant novelty is observed for the proposed model, which is reflected in estimation of subthreshold slope.

## II. MATHEMATICAL MODELING

For analysis of the device, we have considered the well-known structure of pMOSFET.



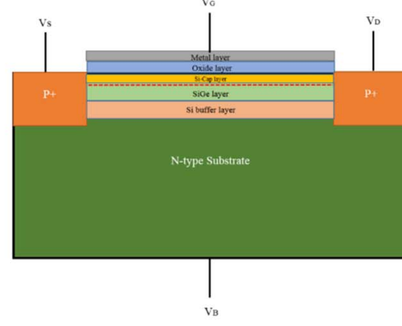




Fig 1. (a): Schematic structure of hetero-structure pMOS, Fig 1(b): Schematic of hetero-structure pMOSFET

Hole mobility for the structure is calculated using the equation

$$\mu_0 = \frac{\mu_{eff}}{1+\left(\frac{\mu_{eff} v_{sd}}{2 v_{sat} L}\right)} \quad (1)$$

where, the parameter '$\mu_{eff}$' defines the effective mobility of hole due to ionic impurity scattering, surface roughness and phonon scattering, given by

$$\mu_{eff} = \left(\frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_c}\right) \quad (2)$$

In presence of band-to-band tunneling, threshold voltage of the device is given by

$$V_{tw} = U \exp\left(\frac{V_{tho}+V_{sg}}{U}\right) \quad (3)$$

where, '$U$' is nomenclature as Urbach factor [25], $V_{tho}$ is the threshold voltage in presence of body effect and in absence of band-to-band tunneling. Threshold voltage in absence of body effect [26], given by

$$V_{t0} = -\varphi_{s2} - qN_D W_d \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{W_{SiT}}{\varepsilon_{Si}}\right) \quad (4)$$

The Urbach factor plays a critical role in tuning the subthreshold conduction as it incorporates both tunneling window opening rate and cut-off voltage, defined as [25]

$$U = \gamma_0 U_0 + (1-\gamma_0) U_0 \left(\frac{V_{sg}-V_{off}}{V_{tho}-V_{off}}\right) \quad (5)$$

where, $V_{off}$ is the cutoff voltage, $\gamma_0$ is the rate of opening of tunneling window, $U_0 = \frac{\eta k_B T}{q}$. The cutoff voltage has the significance of the minimum vertical bias for which tunneling condition remains valid. We have proposed the opening rate of tunneling window as given by

$$\gamma_0 = \operatorname{asin}(V_{sg} - \pi) + b(V_{sg} - 10)^2 + c \quad (6)$$

where, the fitting parameters '$a$', '$b$', '$c$' controls the window operating rate.

Threshold voltage is calculated incorporating the body effect coefficient, as revealed form Eq. (4), can be put into the form

$$V_{tho} = -\varphi_{SB} - \varphi_{s2} - qN_D W_d \left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{W_{SiT}}{\varepsilon_{Si}}\right) \quad (7)$$

where, depletion width is obtained from[36]

$$W_d = -W_{SiB} - \frac{\varepsilon_{Si}}{\varepsilon_{SiGe}} + \sqrt{\frac{2\varepsilon_{Si}}{qN_D}(-\varphi_{s2}) + \left(W_{SiB} + \frac{\varepsilon_{Si}}{\varepsilon_{SiGe}} W_{SiGe}\right)^2} \quad (8)$$

Eq.(7) and Eq.(8) can be together used for subthreshold current computation, whereas Eq.(4) to Eq.(8), is used to obtain threshold voltage and Eq.(8) gives the depletion region width.

## III. Results and Discussions

Simulation starts with threshold voltage computation as a function of Si composition in $Si_xGe_{1-x}$ material within the practical limit so that variation can be taken within the range from $Si_{0.1}Ge_{0.9}$ to $Si_{0.4}Ge_{0.6}$. Simulated findings are compared with the existing result[26], and much lower threshold voltage is obtained, as shown in Fig 2.

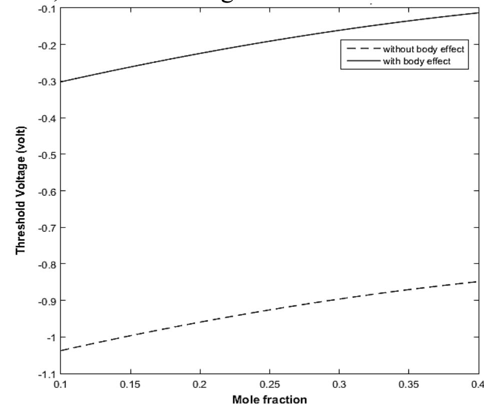



Fig 2. Threshold voltage variation in presence and absence of body effect with material composition for fixed body bias; threshold voltage in absence of body effect is taken from Ref [26]

The application of substrate bias reduces the overall threshold voltage of hetero-structure MOS device, by pushing the minority carriers i.e. holes from the substrate towards channel. Furthermore, increasing the mole fraction of Ge in $Si_xGe_{1-x}$, threshold voltage reduces almost monotonically owing to the increased band bending near the Si-$Si_xGe_{1-x}$ interface. This, in turn, boosts the probability of tunneling. As tunneling factor escalates, more numbers of minority carriers (holes) cross the potential barrier and arrive at the surface, thereby increasing the carrier concentration in channel, which eventually reduces the threshold voltage.

Fig 3 exhibits variation of threshold voltage as a function of source-to-body bias for different material systems. From the plot, it is seen that with an increase in body voltage the threshold voltage reduces and reaches at a minimum value. Further increase in voltage shows an opposite trend in the plot. It happens due to the fact that an increase in body voltage causes the minority carriers to move towards the channel which in turn will reduce the overall threshold voltage. But after a limen the drift velocity of the majority carriers will be more than the minority carriers as their number starts to ascend and scattering commenses. Moreover, due to that congregation of majority carriers, lesser number of minority carriers will reach near the channel. This will eventually cause increase the threshold voltage.

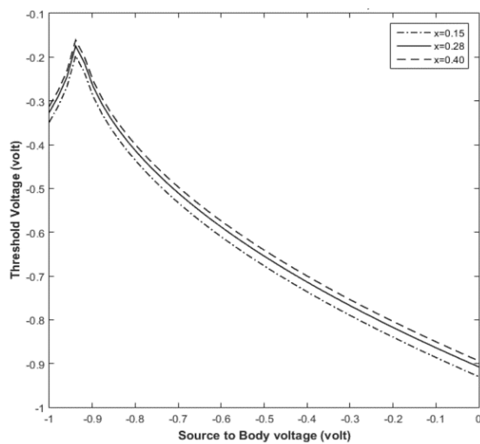



Fig 3. Threshold voltage variation in presence of body effect with source-to-body voltage for different material compositions

Corresponding to Fig 2, depletion width is subsequently computed and plotted, as shown in Fig 4. The result shows a monotonically decreasing nature with increase in Si concentration. Increasing the mole fraction of Silicon enhances band bending and thus reduces the width of the depletion region. It is therefore obvious that as mole fraction of Si increases, the probability of tunneling increases. Consequently, threshold voltage decreases. At a particular material composition, 2DHG (2D- Hole Gas) is formed inside the channel which increases the conductivity of the channel due to enhancement of carrier mobility.

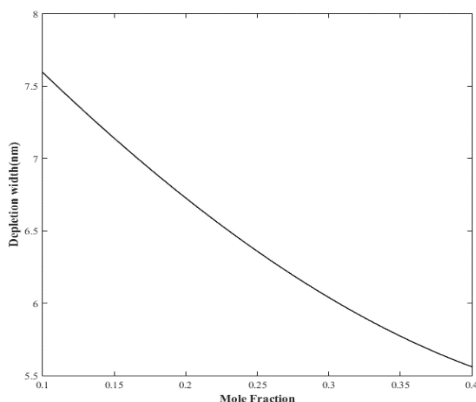



Fig 4. Depletion width with material composition in presence of body effect

Next we calculate the tunneling widow potential and its opening rate as a function of source-to-gate voltage, and the results are in Fig 5 and Fig 6 respectively.

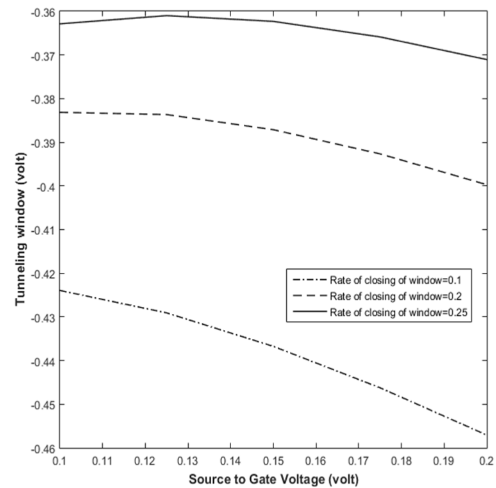



Fig 5. Tunneling window potential as a function of source-to-gate voltage for different closing rates

In Fig 5, it is observed that the tunneling window potential decreases as we increase the source-to-gate voltage($V_{SG}$), resulting in more number of carriers crossing the potential barrier and reaching the channel. As $V_{SG}$ approaches the threshold voltage, the magnitude of tunneling increases and it is also greatly influenced by the rate of closing of the tunneling window. Increment of the tunneling rate reduces the window size (negative axis). Thus, there is an overall increment in the carrier concentration in the channel, which stems in ameliorating the probability of leakage current. In Fig6, we find that for small source-to-gate voltage($V_{SG}$), rate of opening of the tunneling window increases almost linearly. After a limiting value, the rate decreases slightly, even when $V_{SG}$ is increased.

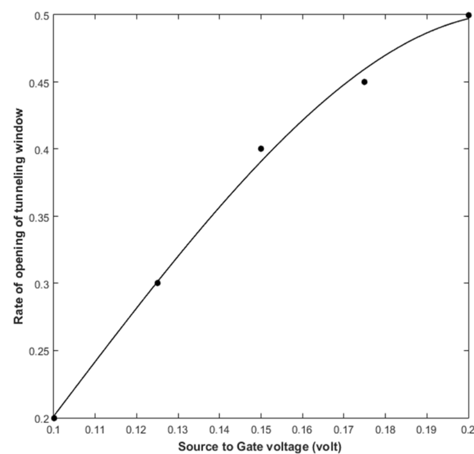



Fig 6: Rate of opening of tunneling window as a function of source-to-gate voltage

This is due to the onset of band to band tunneling, which enhances the carrier density in the channel. Under weak inversion condition, tunneling window opens to almost 50% whereas, under strong inversion

the window opens completely, i.e. 100%. Therefore, in subthreshold regime, the rate of opening of the tunneling window is less than 50% and is primarily dependent on the gate voltage. A detailed analysis reveals the dependency on doping concentration in the substrate, dielectric thickness, and lattice structure near the channel, source-to-drain voltage and effective electric field near the channel.

## IV. Conclusion

Thus in this paper we have proposed a novel threshold voltage model which also incorporates the band-to-band tunneling mechanism in HFET devices. The concept of tunneling window has also been accounted for in our study and detailed analysis for the same has been provided. The variation of threshold voltage, depletion depth and window rate with respect to various values of the date and substrate bias has been observed and the results have been explained using necessary physical phenomena. The future direction of research will be estimation of drain current and subthreshold swing in the presence and absence of tunneling mechanism and characterization of the device to make it suitable for sub nanometer digital applications.

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