Design of Fractional-Order PI controller for DC-DC Power Converters

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***Abstract*— This paper comprises the design of fractional-order proportional–integral (FOPI) controller for dc-dc power converters. Dominant-pole based control technique is used for tuning the parameter values of FOPI controller. To achieve the desired time-domain performances, two equations are derived and solved to obtain values of proportional and integral coefficients of FOPI controller in terms of dominant poles. The control scheme is implemented on second-order power converters, namely dc-dc buck converter and dc-dc boost converter. The simulation results of FOPI controller are compared with integer-order PI (IOPI) controller and it is found that FOPI controller performs comparatively better.**

Keywords- Buck converter, Controller design, Dominant poles, Fractional-order controllers, PI controller.

I. INTRODUCTION

In the past decades, the design of a controller for different power electronic converters in the industry has increased massively. The dc-dc converters find many applications in modern electronic systems such personal computers, medical instruments, portable electronic devices, communication equipment, *etc*. The development of dc-dc converters are enriched with many challenges such as compactness, reliability and excellent robust quality [1]–[3]. Conventional controllers for power converters used in industries are integer-order PI/PID because of its simplicity and acceptable performance [4]–[8]. However, to further improve the performance of dc-dc converters, researchers are looking towards new methods for designing these controllers. Thus designing robust and highly reliable controllers with the better dynamic response, lesser overshoots and undershoots, less settling time, reduced steady-state error are great challenges for the researchers.

Numerous algorithms have been developed for tuning and designing of PID controllers depending upon the applications in industry [9], [10]. Several tuning methods are present, but they have some restrictions. These methods either do not give desired tuning parameterizations or do not fulfill desired performance criterion for the control system. On the other hand, research on fractional-order PI (FOPI) controllers is progressing. The researchers have suggested different methods for tuning of the parameters of these FOPI controllers [11]–[13]. Fractional-order PI controller (FOPI) is a generalization of the conventional integer-order PI controller. It is usually denoted by PI^{λ}, where λ is a fractional coefficient to the integral term of the conventional PI controller, thus further increasing the complexity of tuning these parameters.

A simple approach is presented in this paper to tune the parameters of FOPI controller for dc-dc buck converter and boost converter. The controller's objective is to fulfill the desired time-domain performances of compensated dc-dc converters. The parameters of FOPI controller are tuned based on the dominant pole placement method [14], [15].

In the dominant pole placement method, a pair of desired poles is obtained in terms of specified time-domain performance specifications of dc-dc converters. These poles are termed as dominant poles. As the transient performance of any control system is mainly exhibited by dominant poles, so they can be used for control system analysis and design. Therefore, the control problem is formulated to find out the parameters for the FOPI controller corresponding to the dominant roots of the closed-loop characteristic equation. The values of FOPI parameters are derived in terms of these dominant poles. The performances of tuned FOPI controllers for dc-dc buck and boost are analyzed and compared with integer-order PI controllers.

The remaining contents of the paper are arranged as follows. The mathematical models for dc-dc buck and boost power converter are derived in section II. In section III, the control strategy is mentioned where dominant poles calculation and FOPI controllers have been designed for both the converters. Section IV depicts the FOPI controller design example for buck and boost converters and its simulation results. The conclusion is presented in section V followed by references.

II. MODELLING OF DC-DC BUCK AND BOOST CONVERTER

A. Buck converter

The power configuration of an ideal dc–dc buck converter is shown in Fig. 1. It has a switching device (MOSFET) *S*, inductor *L*, diode *D*, capacitor *C* and load resistor *R*. For simplicity, the parasitic resistances of different elements, *i.e*. equivalent series resistances (ESRs) of inductor and capacitor, diode forward resistance, switch on-resistance have been neglected. The converter has switching frequency *f*, duty cycle *D*. The switch (MOSFET) is ON for a *DT* duration and OFF for a duration of *(1-D)T*, where *T* is time period of one switching cycle ($T=1/f$). In continuous conduction mode (CCM), the converter operates in two modes, which are discussed below [16]:

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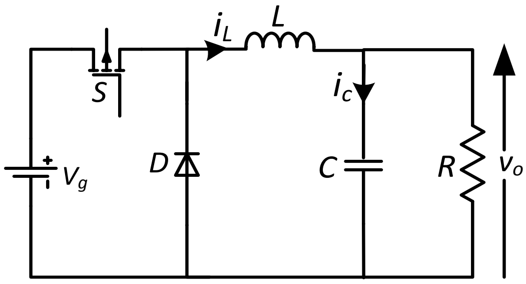

Fig. 1 DC-DC buck converter

(1) Mode-1: when MOSFET is ON ($0<t\leq DT$)

In this mode, the diode is open circuited as it is in reverse biased condition, during this state, the inductor charges through input voltage V_g and the inductor current (i_L) increases.
The state equations for this mode are:

$$L\frac{di_L}{dt}=V_g-v_0 \tag{1}$$

$$C\frac{dv_0}{dt}=i_L-\frac{v_0}{R} \tag{2}$$

In matrix form,

$$A_1=\begin{pmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & \frac{-1}{RC}\end{pmatrix}, B_1=\begin{pmatrix}\frac{1}{L}\\ 0\end{pmatrix}, C_1=\begin{pmatrix}0 & 1\end{pmatrix} \tag{3}$$

(2) Mode-2: when MOSFET is OFF ($DT<t\leq T$)

In this mode, MOSFET switch is OFF and the diode is in forward biased condition. The inductor now discharges through the diode, capacitor C and load resistance R.
The state equations for this mode are:

$$L\frac{di_L}{dt}=-v_o \tag{4}$$

$$C\frac{dv_o}{dt}=i_L-\frac{v_o}{R} \tag{5}$$

In matrix form,

$$A_2=\begin{pmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & \frac{-1}{RC}\end{pmatrix}, B_2=\begin{pmatrix}0\\ 0\end{pmatrix}, C_2=\begin{pmatrix}0 & 1\end{pmatrix} \tag{6}$$

The duty-cycle to output-voltage transfer function is given as [4]:

$$\frac{v_0}{d}=C(sI-A)^{-1}B \tag{7}$$

where,

$$A=A_1D+A_2\left(1-D\right), C=C_1D+C_2\left(1-D\right)$$
$$B=\left(A_1-A_2\right)\begin{pmatrix}I_L\\ V_o\end{pmatrix}-\left(B_1-B_2\right)V_g \tag{8}$$

In (8), D, V_o and I_L are the steady-state values of the duty cycle, output voltage and inductor current respectively.

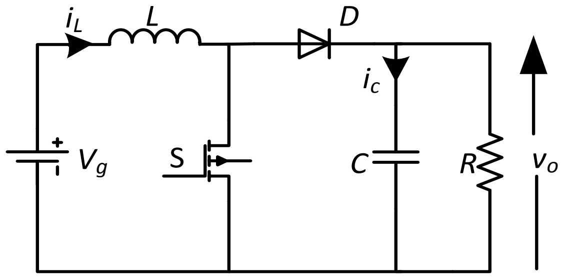

Fig. 2 DC-DC boost converter

Substituting the matrices A, B, C in (7), the duty-cycle to output-voltage transfer for buck converter is obtained as:

$$G_{buck}\left(s\right)=\frac{V_g}{s^2LC+s\frac{L}{R}+1} \tag{9}$$

B. Boost Converter

The circuit configuration of an ideal dc-dc boost converter is shown in Fig. 2 [16]. It is assumed to be operated in CCM. The description of circuit elements is same as in buck converter.

(1) Mode-1: when MOSFET is ON ($0<t\leq DT$)

In this mode, diode will be reverse biased. During this state, the inductor charges through input voltage V_g and the inductor current increases. The load is supplied by discharging of the capacitor.
The state equations for these mode are:

$$L\frac{di_L}{dt}=V_g \tag{10}$$

$$C\frac{dv_o}{dt}=-\frac{v_o}{R} \tag{11}$$

In matrix from,

$$A_1=\begin{pmatrix}0 & 0\\ 0 & \frac{-1}{RC}\end{pmatrix}, B_1=\begin{pmatrix}\frac{1}{L}\\ 0\end{pmatrix}, C_1=\begin{pmatrix}0 & 1\end{pmatrix} \tag{12}$$

(2) Mode -2: when MOSFET is OFF ($DT<t\leq T$)

In this mode, the diode will be forward biased. The inductor now discharges through the diode and RC combination.
The state equations for this mode are:

$$L\frac{di_L}{dt}=V_g-V_0 \tag{13}$$

$$C\frac{dv_o}{dt}=i_L-\frac{v_o}{R} \tag{14}$$

In matrix form,

$$A_2=\begin{pmatrix}0 & -\frac{1}{L}\\ \frac{1}{C} & \frac{-1}{RC}\end{pmatrix}, B_2=\begin{pmatrix}\frac{1}{L}\\ 0\end{pmatrix}, C_2=\begin{pmatrix}0 & 1\end{pmatrix} \tag{15}$$

Substituting the matrices in (8) and then (7), the duty-cycle to output-voltage transfer function of the boost converter is

$$G_{boost}(s)=\frac{V_o\left(1-s\frac{L_e}{R}\right)}{D'L_eC\left(s^2+s\frac{1}{RC}+\frac{1}{L_eC}\right)} \quad (16)$$

where, $D'=1-D, L_e=L/D'^2$

III. CONTROL STRATEGY

In this section, a control strategy is discussed to calculate the dominant poles of the closed-loop system to achieve desired performance specification. This control design procedure is used for dc-dc buck and boost power converters. For calculating the dominant poles in this paper, settling time (T_s) and overshoot (M_p) are considered as a performance parameter. Therefore, the dominant poles are calculated in terms of T_s and M_p.

A. Dominant poles calculation

Consider that the compensated system is represented by its dominant poles and the corresponding closed-loop system is a second-order system having following transfer function.

$$G_p(s)=\frac{\omega_n{}^2}{s^2+2\xi\omega_n+\omega_n{}^2} \quad (17)$$

For the unit response of this closed-loop system, its settling time and overshoot are found as [17].

Settling time (T_s) = $\frac{4}{\xi\omega_n}$ (18)

Overshoot (M_p) = $e^{-\frac{\xi\pi}{\sqrt{1-\xi^2}}}$ (19)

The poles of the closed-loop system *i.e.* s_1 and s_2 in (17) are given as

$$s_1, s_2=-\zeta\omega_n\pm\omega_n\sqrt{\zeta^2-1} \quad (20)$$

Equation (20) can be written as

$$s_1, s_2=\zeta\omega_n\left(-1\pm j\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \quad (21)$$

Similarly, (18) and (19) are rewritten as

$$\xi\omega_n=\frac{4}{T_s} \quad (22)$$

$$\frac{\sqrt{1-\xi^2}}{\xi}=\frac{-\pi}{\ln M_P} \quad (23)$$

Now substituting values from (22) and (23) into (21), the dominant poles of closed-loop system represented by (17) are obtained in terms of its performance parameters (T_s and M_p). Thus, the dominant poles are

$$s_1, s_2=\frac{4}{T_s}\left(-1\pm j\frac{\pi}{\ln M_P}\right) \quad (24)$$

B. Fractional-order PI (FOPI) design

Let transfer function of FOPI controller (G_c) is given as

$$G_c(s)=\left(k_p+\frac{k_i}{s^\lambda}\right) \quad (25)$$

Assume that $s_d=x+jy$ be a dominant pole of the closed-loop system.

From Euler's form,

$$s_d=x+jy=Ae^{j\theta}=A(\cos\theta+j\sin\theta) \quad (26)$$

where, $A=\sqrt{x^2+y^2}, \theta=\tan^{-1}\left(\frac{y}{x}\right)$

Let the plant function at dominated poles is represented as

$$G_p(s)\big|_{s=s_d}=\alpha+j\beta \quad (27)$$

At dominant pole $s=s_d$, the characteristic equation becomes

$$1+G_p(s_d)G_c(s_d)=0 \quad (28)$$

Substituting values from (25) and (27) into(28), we get

$$1+(\alpha+j\beta)\left(k_p+\frac{k_i}{s_d^\lambda}\right)=0 \quad (29)$$

Substituting the value of s_d from (26) into (29) and then simplifying, we get

$$A^\lambda(\cos\lambda\theta+j\sin\lambda\theta) +(\alpha+j\beta)\left[k_pA^\lambda(\cos\lambda\theta+j\sin\lambda\theta)+k_i\right]=0 \quad (30)$$

Separating real and imaginary parts, we get

Real part:

$$A^\lambda\cos\lambda\theta+\alpha\left(k_pA^\lambda\cos\lambda\theta+k_i\right)-\beta k_pA^\lambda\sin\lambda\theta=0 \quad (31)$$

Imaginary part:

$$A^\lambda\sin\lambda\theta+\beta\left(k_pA^\lambda\cos\lambda\theta+k_i\right)+\alpha k_pA^\lambda\sin\lambda\theta=0 \quad (32)$$

Rearranging above equations, we get

$$k_pA^\lambda(\alpha\cos\lambda\theta-\beta\sin\lambda\theta)+k_i\alpha=-A^\lambda\cos\lambda\theta \quad (33)$$

$$k_pA^\lambda(\beta\cos\lambda\theta+\alpha\sin\lambda\theta)+k_i\beta=-A^\lambda\sin\lambda\theta \quad (34)$$

Here k_p, k_i,and λ are unknown quantities whereas A, α, β, θ are known quantities. There are two equations and three unknown quantities. Therefore, solution for any two variable can be obtained while keeping the third variable constant. There are three possibilities: (i) solution for pair (k_p, k_i) while λ constant (ii) solution for pair (k_p, λ) while k_i constant and (iii) solution for pair (k_i, λ) while k_p constant.

In this paper, the solutions for (k_p, k_i) is obtained while keeping λ constant.

Equations (33) and (34) are written as

$$X_1k_p+Y_1k_i=Z_1 \quad (35)$$

$$X_2k_p+Y_2k_i=Z_2 \quad (36)$$

where

$X_1=A^\lambda(\alpha\cos\lambda\theta-\beta\sin\lambda\theta), Y_1=\alpha, Z_1=-A^\lambda\cos\lambda\theta$

$X_2=A^\lambda(\beta\cos\lambda\theta+\alpha\sin\lambda\theta), Y_2=\beta, Z_2=-A^\lambda\sin\lambda\theta$

Solving (35) and (36), we get

$$k_p=\frac{Y_2Z_1-Y_1Z_2}{X_1Y_2-X_2Y_1} \quad (37)$$

$$k_i = \frac{X_1 Z_2 - X_2 Z_1}{X_1 Y_2 - X_2 Y_1} \quad (38)$$

Using (37) and (38), the values of k_p and ki can be found out for the desired dominant poles with fixing λ to a constant value.

IV. Controller Design for DC-DC Power Converters

In this section, the FOPI controller for the dc-dc buck and boost converters will be designed for the given time domain specifications.

A. Buck converter

The parameters of buck converter used is shown in Table I. Substituting these values in (9), the duty-cycle to output-voltage transfer function of buck converter is obtained as

$$G_{buck}(s) = \frac{24}{9.24\times10^{-8}s^2 + 9.16\times10^{-5}s + 1} \quad (39)$$

The time response of the uncompensated dc-dc buck converter for duty cycle 0.5 is shown in Fig. 3. The peak overshoot is 61.45% and settling time is 8ms. It can be seen that the peak overshoot of open-loop buck converter is very high. Therefore, a feedback control is designed for the buck converter.

The transfer function of the uncompensated closed-loop buck converter is obtained as

$$G_{cl\_buck}(s) = \frac{24}{9.24\times10^{-8}s^2 + 9.16\times10^{-5}s + 25} \quad (40)$$

The unit time response of uncompensated closed-loop buck converter is shown in Fig. 4. It is observed that the response is having very high overshoot of 90% and steady-state error of 5%. An integer-order PI (IOPI) controller is designed to eliminate the steady-state error and the unit step response of closed-loop buck converter is shown in Fig. 5. It can be observed that with IOPI controller steady-state error is eliminated and overshoot is reduced to 38% with settling time of 4.91ms. To further reduce the overshoot and settling time, a FOPI controller is designed using the steps discussed in the previous section. The PI parameters of FOPI controller is k_p=1.12 and k_i=5.95×10^6 for λ=1.9. The FOPI controller for buck converter is

$$G_{buck\_FOPI}(s) = 1.12 + \frac{5.95\times10^6}{s^{1.9}} \quad (41)$$

The unit step response with FOPI controller is shown in Fig.5. As clearly observed, the overshoot is reduced to 30% and settling time to 1ms with the elimination of steady-state error. Therefore, FOPI controller gives better results as compared to IOPI controller. The performance comparison of IOPI and FOPI controller for buck converter is given in Table II.

TABLE I PARAMETERS OF DC–DC BUCK CONVERTER

Parameters	value
Input voltage (V_g)	24 V
Output voltage(V_o)	12 V
Inductance (L)	1.1mH
Capacitance(C)	84 µF
Switching frequency(f)	10 kHz
Load resistance(R)	12 Ω
Duty cycle(D)	0.5

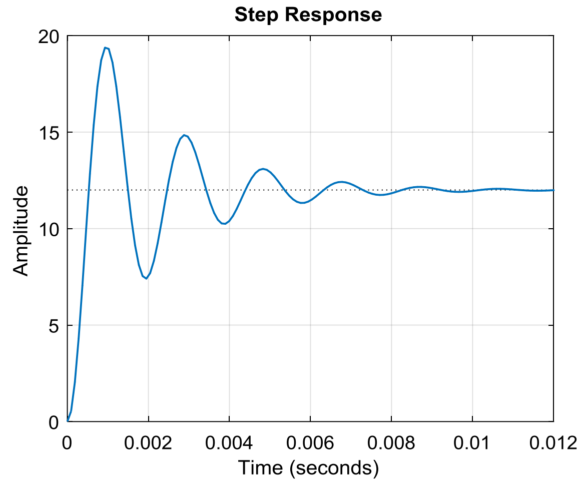

Fig. 3 Step response of open-loop buck converter

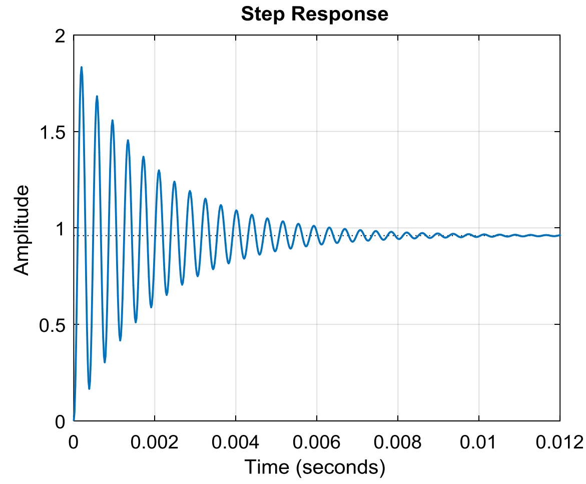

Fig. 4 Step response of uncompensated closed-loop buck converter

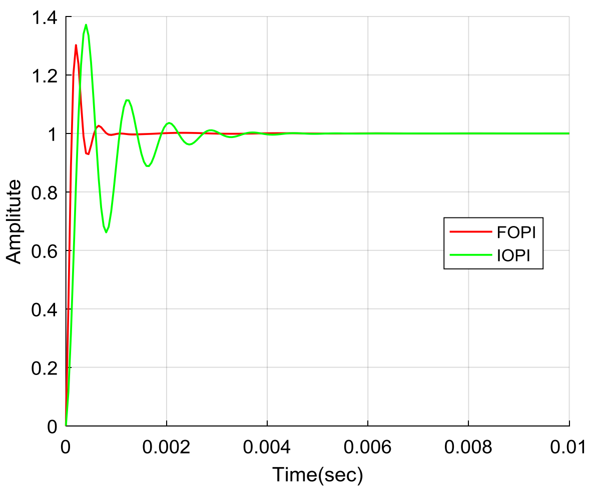

Fig. 5 Step response of compensated closed-loop buck converter

TABLE II PERFORMANCE COMPARISON OF IOPI &FOPI CONTROLLERS FOR CLOSED-LOOP Buck CONVERTER

Parameters	IOPI controllers	FOPI controllers
Rise time	0.2ms	0.1ms
Settling time	4.91ms	1.01ms
Peak overshoot	38%	30%

B. Boost converter:

The boost converter parameters used in this paper is shown in Table III. On substituting these values in (16), the duty-cycle to output-voltage transfer function of buck converter is obtained as

$$G_{boost}(s)=\frac{-28.57s+1.896\times10^{6}}{0.0264s^{2}+s+66360} \quad (42)$$

The time response of uncompensated open-loop dc-dc boost converter for duty cycle 0.58 is shown in Fig.6. The peak overshoot is 96.31% and settling time is 0.21s. As seen, peak overshoot, as well as settling time, are very high. A feedback control is designed for the boost converter to improve these performance parameters.

$$G_{cl\_boost}(s)=\frac{-28.57s+1.896\times10^{6}}{0.0264s^{2}-27.57s+1.962\times10^{6}} \quad (43)$$

The poles of uncompensated boost converters are 522.18±j8605.7, which indicates that the system is unstable. The unit time response of uncompensated closed-loop boost converter is shown in Fig. 7. From this response also, it is observed that the unit response is unstable. An Integer-order PI (IOPI) controller is designed to stabilize the closed-loop system. The step unit response with PI controller for boost converter is shown in Fig. 8. It can be observed that with IOPI controller closed-loop system is stable and overshoot is reduced to 46% with settling time of 40ms. To further reduce the overshoot and settling time, a FOPI controller is designed using the steps discussed in section. The PI parameters of FOPI controller is k_p =0.1787,k_i=1.8144×10^3 for λ=1.5. The FOPI controller for boost converter is

$$G_{boost\_FOPI}(s)=0.178+\frac{1.81\times10^{3}}{s^{1.5}} \quad (44)$$

The unit step response with FOPI is shown in Fig.8. As clearly observed, the overshoot is reduced to 9% and settling time to 12ms with elimination of steady-state error. Therefore, the peak overshoot and settling time for FOPI based closed-loop system in both the cases is less than IOPI controller. The performance comparison of IOPI and FOPI controller for boost converter is given in Table IV.

TABLE III PARAMETERS OF DC–DC BOOST CONVERTER

Parameters	**value**
Input voltage (V_g)	5 V
Output voltage(V_o)	12 V
Inductance (L)	250 µH
Capacitance(C)	1056 µF
Switching frequency(f)	10 kHz
Load resistance(R)	25 Ω
Duty cycle(D)	0.58

TABLE IV PERFORMANCE COMPARISON OF IOPI &FOPI CONTROLLERS FOR CLOSED-LOOP BOOST CONVERTER

Parameters	**IOPI controllers**	**FOPI controllers**
Rise time	1.68ms	1.73ms
Settling time	40ms	12 ms
Peak overshoot	46%	9.0%

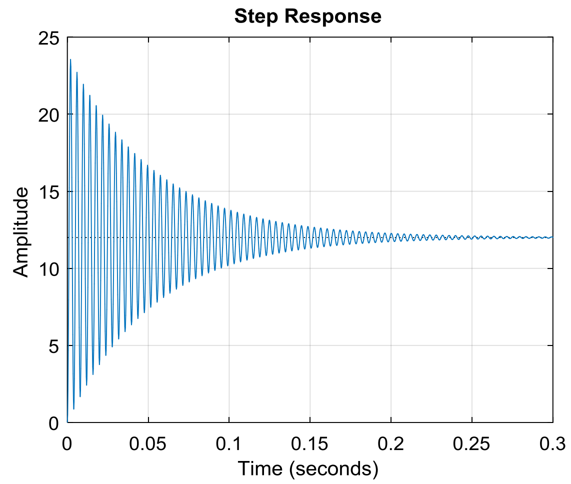

Fig. 6 Step response of open-loop boost converter

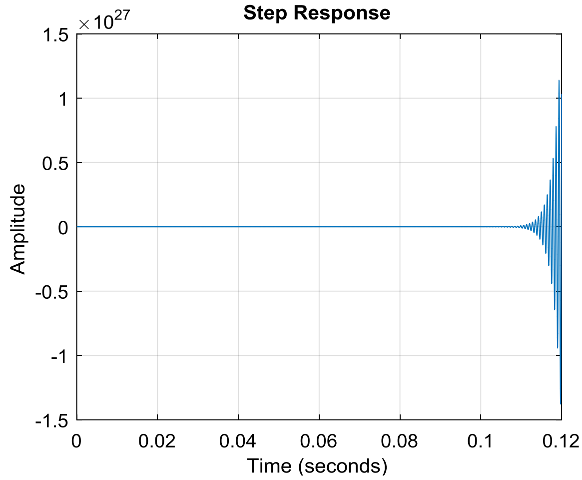

Fig. 7 Step response of uncompensated closed-loop boost converter

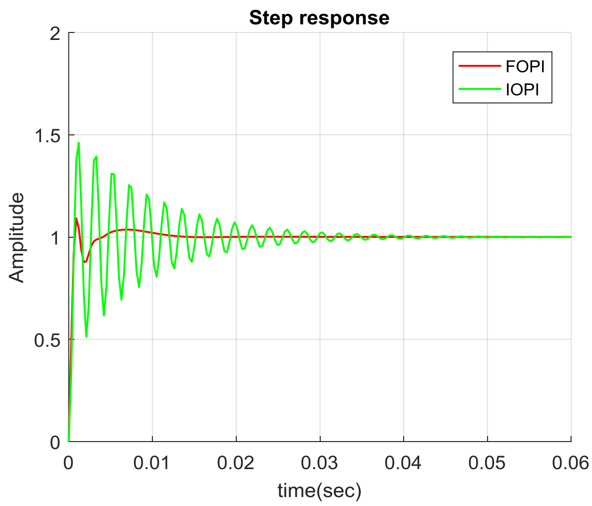

Fig. 8 Step response of compensated closed-loop boost converter

V. Conclusion

In this paper, the dominant pole placement based approach is used for finding the parameters of fractional-order PI controller. The design procedure is explained and controller parameters are obtained for two different dc-dc power converter topologies. The simulation results show that the rise time, peak overshoot and settling time for FOPI based closed-loop systems are lesser than IOPI controller for both dc-dc buck converter and dc-dc boost converter. The control design gives a satisfactory desired response. This pole placement based FOPI method can be extended for designing FOPID controller *i.e.* including a derivative component in systems for further improving the desired response. Also, FOPI based controller can be designed for different types of dc-dc converters having transportation lag.

REFERENCES

[1] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 559–572, 2006.

[2] B. Arbetter, R. Erickson, and D. Maksimovic, "DC-DC converter design for battery-operated systems," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, 1995, vol. 1, pp. 103–109.

[3] J. C. Vilchis, C. Aguilar, and J. Arau, "Multi-mode synchronous buck converter with non-uniform current distribution for portable applications," in *IEEE International Power Electronics Congress*, 2008, pp. 114–120.

[4] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Design and Performance Analysis of a PWM dc–dc Buck Converter Using PI–Lead Compensator," *Arab. J. Sci. Eng.*, vol. 40, no. 12, 2015.

[5] M. Zhuang and D. P. Atherton, "Automatic tuning of optimum PID controllers," *IEE Proc. D Control Theory Appl.*, vol. 140, no. 3, p. 216, 1993.

[6] H. Sira-Ramirez, "Nonlinear P-I controller design for switchmode DC-to-DC power converters," *IEEE Trans. Circuits Syst.*, vol. 38, no. 4, pp. 410–417, Apr. 1991.

[7] J. Alvarez-Ramirez, I. Cervantes, G. Espinosa-Perez, P. Maya, and A. Morales, "A stable design of PI control for DC-DC converters with an RHS zero," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 48, no. 1, pp. 103–106, 2001.

[8] M. M. Garg, Y. V. Hote, M. K. Pathak, and L. Behera, "An Approach for Buck Converter PI Controller Design Using Stability Boundary Locus," in *2018 IEEE/PES Transmission and Distribution Conference and Exposition (T&D)*, 2018, pp. 1–5.

[9] W. K. Ho, C. C. Hang, and L. S. Cao, "Tuning of PID controllers based on gain and phase margin specifications," *Automatica*, vol. 31, no. 3, pp. 497–502, Mar. 1995.

[10] M. Nagurka and O. Yaniv, "Robust PI controller design satisfying gain and phase margin constraints," in *IEEE American Control Conference*, 2003, vol. 5, pp. 3931–3936.

[11] H. S. Khaldi and A. C. Ammari, "Fractional-order control of three level boost DC/DC converter used in hybrid energy storage system for electric vehicles," in *IREC2015 The Sixth International Renewable Energy Congress*, 2015, pp. 1–7.

[12] A. Tepljakov, "Fractional-Order PID Controller Design," Springer, Cham, 2017, pp. 47–76.

[13] Liping Guo, J. Y. Hung, and R. M. Nelms, "Evaluation of DSP-Based PID and Fuzzy Controllers for DC–DC Converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2237–2248, Jun. 2009.

[14] Yu Zhang, Ing-Guo Wang, and K. J. Astrom, "Dominant pole placement for multi-loop control systems," in *Proceedings of the 2000 American Control Conference. ACC (IEEE Cat. No.00CH36334)*, 2000, pp. 1965–1969 vol.3.

[15] E. Steed, E. Quesada, L. Rodolfo, G. Carrillo, A. N. Ramirez, and S. Mondie, "Algebraic dominant pole placement methodology for unmanned aircraft systems with time delay," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 52, no. 3, pp. 1108–1119, Jun. 2016.

[16] M. M. Garg and Y. V. Hote, "Leverrier algorithm based reduced order modeling of dc-dc converters," in *India International Conference on Power Electronics, IICPE*, 2014, pp. 1–6.

[17] K.Ogata, *Modern Control Engineering*, 5th ed. Prentice hall, 2010.

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