

Performance Comparison of Non-ideal and Ideal Models of DC-DC Buck Converter

Man Mohan Garg¹ and Mukesh Kumar Pathak²

¹Department of Electrical Engineering
National Institute of Technology Rourkela
Odisha, India- 769008

²Department of Electrical Engineering
Indian Institute of Technology Roorkee
Uttarakhand, India- 247667

Abstract— In this paper, the mathematical modeling of the non-ideal dc-dc buck converter is carried out. The three important transfer function namely input voltage to output voltage transfer function, load current to output voltage transfer function and duty cycle to output voltage transfer function is derived in terms of non-ideal elements of buck converter operating in continuous conduction mode (CCM). All the major non-idealities which have an impact on the steady-state and dynamic behavior of buck converter have been included. The frequency domain and time-domain responses are obtained to compare the converter behavior in the non-ideal case and an ideal case. The MATLAB simulation results are provided to support the theoretical analysis.

Index Terms— Buck converter, Continuous conduction mode (CCM), Equivalent series resistance (ESR), Mathematical Model.

I. INTRODUCTION

The dc-dc buck converters have been employed in various applications [1]–[5]. Buck converter converts input dc voltage to a lower dc level at output terminals. Proper controller design is required to regulate the output voltage of buck converter in the presence of disturbances in input voltage supply or load. Many control schemes are available in the literature [6]–[11]. The first step in control design is to obtain a good mathematical model of the dc-dc buck converter. Therefore, mathematical modeling is an important research aspect in dc-dc converters [12]. The mathematical modeling of a system is helpful in choosing a proper control scheme. Moreover, it provides a tool to pre-evaluate the steady-state and dynamic behavior of the converter under different input and load conditions. To get the mathematical models of dc-dc converter, many methods do exist in the literature. However, the state-space averaging technique is used widely due to ease of implementation [13], [14]. Any dc-dc converter has parasitic resistances in its storage elements (inductors, capacitors) and switching devices (MOSFET, diodes) *etc* [15]–[18]. Moreover, diode also has forward conduction

voltage drop, which is about 0.7-1.5 V. These parasitic resistances has voltage drop across it when the converter is operated at different loads, thus affecting the transient and steady-state performance the converter. The practical converter is having all these parasitic elements and therefore it is not proper to neglect these elements while modeling and controlling a dc-dc converter. However, to have the lower values of these parasitic are always preferable for higher converter efficiency. Therefore, in this paper, the accurate transfer function models and steady-state output voltage expression are obtained in terms of these non-idealities. A comparison is done between time-domain and frequency domain responses of the buck converter in non-ideal and ideal case. The simulation results show that parasitic elements provide damping which results in more stable and less oscillatory system. However, due to voltage drops across parasitic resistances, the output voltage of dc-dc buck converter reduces and also the efficiency.

This paper is organized in different sections. Section-II gives the dynamic model of non-ideal buck converter under two-switching modes in continuous conduction mode (CCM). The third section provides steady-state and small-signal analysis of non-ideal buck converter. Three importance transfer functions for output voltage are derived in section-IV for non-ideal buck converter and in section-V for an ideal buck converter. The simulation results are discussed in section-VI followed by conclusion in section-VII.

II. DYNAMIC MODELS OF NON-IDEAL AND IDEAL DC-DC BUCK CONVERTER

The circuit diagram of non-ideal dc-dc buck converter is shown in Fig. 1. It consists of power MOSFET switch S , diode D_d , inductor L , capacitor C and load resistance R . For obtaining precise models of buck converter, all the major non-idealities which may affect the dynamic and steady-state response of converter are considered. The different non-idealities are equivalent series resistance (ESR) of inductor r_L , ESR of capacitor r_c , switch on-resistance r_{sw} , diode

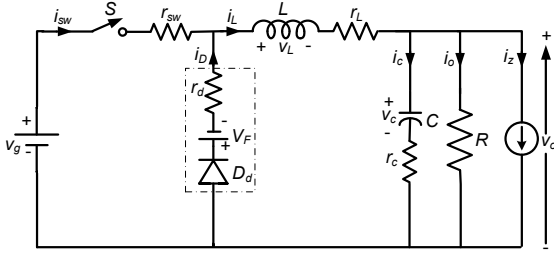


Fig. 1 Non-ideal DC-DC buck converter

forward resistance r_d and diode forward voltage drop V_F . The values of these parasitic resistances are very small in comparison to load resistance R . At the output stage, a current source $i_z(t)$ has been added to determine the dynamic effect of load current variation on output voltage response. The models of non-ideal dc-dc buck converter is obtained by considering it to be operated in continuous conduction mode (CCM) with steady-state duty cycle D and switching frequency f (or switching period $T=1/f$) [19]. In CCM, the buck converter operates in two modes:

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \left(r_{sw} + r_L + \frac{r_c R}{R + r_c} \right) & -\frac{1}{L} \left(\frac{R}{R + r_c} \right) \\ \frac{1}{C} \left(\frac{R}{R + r_c} \right) & -\frac{1}{C} \left(\frac{1}{R + r_c} \right) \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{1}{L} \left(\frac{r_c R}{R + r_c} \right) \\ 0 & -\frac{1}{C} \left(\frac{R}{R + r_c} \right) \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (4)$$

$$v_o(t) = \begin{bmatrix} \frac{r_c R}{R + r_c} & \frac{R}{R + r_c} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{r_c R}{R + r_c} \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} \quad (5)$$

Here, i_L , v_c , v_g and v_o are instantaneous values of the inductor current, capacitor voltage, input voltage and output voltage.

Mode-2 Switch is off (time interval $DT < t \leq T$): For time interval $DT < t \leq T$, the MOSFET switch S is off and diode D_d is conducting. The diode is modelled by its on-resistance r_d and forward voltage drop V_F and switch is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltage, capacitor current and output voltage equations are given as:

$$L \frac{di_L(t)}{dt} = - \left(r_d + r_L + \frac{r_c R}{R + r_c} \right) i_L(t) - \frac{R}{R + r_c} v_c(t) + \frac{r_c R}{R + r_c} i_z(t) - V_F \quad (6)$$

$$C \frac{dv_c(t)}{dt} = \frac{R}{R + r_c} i_L(t) - \frac{1}{R + r_c} v_c(t) - \frac{R}{R + r_c} i_z(t) \quad (7)$$

$$v_o(t) = \frac{r_c R}{R + r_c} i_L(t) + \frac{R}{R + r_c} v_c(t) - \frac{r_c R}{R + r_c} i_z(t) \quad (8)$$

In matrix form,

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{L} \left(r_d + r_L + \frac{r_c R}{R + r_c} \right) & -\frac{1}{L} \left(\frac{R}{R + r_c} \right) \\ \frac{1}{C} \left(\frac{R}{R + r_c} \right) & -\frac{1}{C} \left(\frac{1}{R + r_c} \right) \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L} \left(\frac{r_c R}{R + r_c} \right) \\ 0 & -\frac{1}{C} \left(\frac{R}{R + r_c} \right) \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} -\frac{V_F}{L} \\ 0 \end{bmatrix} \quad (9)$$

$$v_o(t) = \begin{bmatrix} \frac{r_c R}{R + r_c} & \frac{R}{R + r_c} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{r_c R}{R + r_c} \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} \quad (10)$$

III. STEADY-STATE AND SMALL-SIGNAL ANALYSIS

State-space averaging (SSA) technique is used to obtain a large-signal model of non-ideal dc-dc buck converter. In SSA technique, the dynamic models obtained in switch-on and switch-off mode are averaged over one switching cycle of

MOSFET. Then, the averaged model is linearized by introducing small perturbations around a static equilibrium point. The following perturbations in variables are introduced around their respective steady-state (DC) values

$$\bar{i}_L(t) = I_L + \tilde{i}_L(t), \bar{v}_c(t) = V_c + \tilde{v}_c(t), \bar{v}_o(t) = V_o + \tilde{v}_o(t),$$

Mode-1 Switch is on (time interval $0 < t \leq DT$): For time interval $0 < t \leq DT$, the MOSFET switch S is conducting and diode D_d is off. The switch is modeled by its on-resistance r_{sw} and the diode is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltage, capacitor current and output voltage equations are given as:

$$L \frac{di_L(t)}{dt} = - \left(r_{sw} + r_L + \frac{r_c R}{R + r_c} \right) i_L(t) - \frac{R}{R + r_c} v_c(t) + v_g(t) + \frac{r_c R}{R + r_c} i_z(t) \quad (1)$$

$$C \frac{dv_c(t)}{dt} = \frac{R}{R + r_c} i_L(t) - \frac{1}{R + r_c} v_c(t) - \frac{R}{R + r_c} i_z(t) \quad (2)$$

$$v_o(t) = \frac{r_c R}{R + r_c} i_L(t) + \frac{R}{R + r_c} v_c(t) - \frac{r_c R}{R + r_c} i_z(t) \quad (3)$$

In matrix form,

$$d(t) = D + \tilde{d}(t), \bar{v}_g(t) = V_g + \tilde{v}_g(t), \bar{i}_z = I_z + \tilde{i}_z(t) \quad (11)$$

On averaging the dynamic models obtained in (4)-(5) and (9)-(10) and then linearizing using the above perturbations, we get the linearized large-signal model of dc-dc converter below.

$$\begin{bmatrix} \frac{d(I_L + \tilde{i}_L(t))}{dt} \\ \frac{d(V_c + \tilde{v}_c(t))}{dt} \end{bmatrix} = A \begin{bmatrix} I_L + \tilde{i}_L(t) \\ V_c + \tilde{v}_c(t) \end{bmatrix} + B \begin{bmatrix} V_g + \tilde{v}_g(t) \\ I_z + \tilde{i}_z(t) \end{bmatrix} + B_d \tilde{d}(t) + \begin{bmatrix} -\frac{D'V_F}{L} \\ 0 \end{bmatrix} \quad (12)$$

$$V_o + \tilde{v}_o(t) = C_c \begin{bmatrix} I_L + \tilde{i}_L(t) \\ V_c + \tilde{v}_c(t) \end{bmatrix} + E \begin{bmatrix} V_g + \tilde{v}_g(t) \\ I_z + \tilde{i}_z(t) \end{bmatrix} \quad (13)$$

Here,

$$A = \begin{bmatrix} -\frac{1}{L} \left(Dr_{sw} + D'r_d + r_L + \frac{r_c R}{R+r_c} \right) & -\frac{1}{L} \left(\frac{R}{R+r_c} \right) \\ \frac{1}{C} \left(\frac{R}{R+r_c} \right) & -\frac{1}{C} \left(\frac{1}{R+r_c} \right) \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{D}{L} & \frac{1}{L} \left(\frac{r_c R}{R+r_c} \right) \\ 0 & -\frac{1}{C} \left(\frac{R}{R+r_c} \right) \end{bmatrix}, C_c = \begin{bmatrix} \frac{r_c R}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix},$$

$$E = \begin{bmatrix} 0 & -\frac{r_c R}{R+r_c} \end{bmatrix}, B_d = \begin{bmatrix} \frac{V_g + V_F - (r_{sw} - r_d) I_L}{L} \\ 0 \end{bmatrix}$$

The large-signal model in (12) and (13) can be separated to get the corresponding steady-state model and small-signal model.

Steady-state model:

By substituting perturbation terms in (12) and (13) to zero, we get steady-state model as

$$0 = A \begin{bmatrix} I_L \\ V_c \end{bmatrix} + B \begin{bmatrix} V_g \\ I_z \end{bmatrix} + \begin{bmatrix} -\frac{D'V_F}{L} \\ 0 \end{bmatrix} \quad (14)$$

$$V_o = C_c \begin{bmatrix} I_L \\ V_c \end{bmatrix} + E \begin{bmatrix} V_g \\ I_z \end{bmatrix} \quad (15)$$

Upon simplification, we get the expression for dc values of inductor current and output voltage as

$$I_L = \frac{V_o}{R} + I_z \quad (16)$$

$$V_o = V_c = \frac{DV_g - D'V_F - I_z(r_L + Dr_{sw} + D'r_d)}{1 + \frac{1}{R}(r_L + Dr_{sw} + D'r_d)} \quad (17)$$

Small-signal model:

By substituting steady-state terms in (12) and (13) to zero, we get steady-state model as

$$\begin{bmatrix} \frac{d\tilde{i}_L(t)}{dt} \\ \frac{d\tilde{v}_c(t)}{dt} \end{bmatrix} = A \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + B \begin{bmatrix} \tilde{v}_g(t) \\ \tilde{i}_z(t) \end{bmatrix} + B_d \tilde{d}(t) \quad (18)$$

$$\tilde{v}_o(t) = C_c \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + E \begin{bmatrix} \tilde{v}_g(t) \\ \tilde{i}_z(t) \end{bmatrix} \quad (19)$$

Taking Laplace transform of (18)-(19),

$$\begin{aligned} s \begin{bmatrix} \tilde{i}_L(s) \\ \tilde{v}_c(s) \end{bmatrix} &= A \begin{bmatrix} \tilde{i}_L(s) \\ \tilde{v}_c(s) \end{bmatrix} + B \begin{bmatrix} \tilde{v}_g(s) \\ \tilde{i}_z(s) \end{bmatrix} + B_d \tilde{d}(s) \\ \Rightarrow \begin{bmatrix} \tilde{i}_L(s) \\ \tilde{v}_c(s) \end{bmatrix} &= (sI - A)^{-1} B \begin{bmatrix} \tilde{v}_g(s) \\ \tilde{i}_z(s) \end{bmatrix} + (sI - A)^{-1} B_d \tilde{d}(s) \end{aligned} \quad (20)$$

$$\tilde{v}_o(s) = C_c \begin{bmatrix} \tilde{i}_L(s) \\ \tilde{v}_c(s) \end{bmatrix} + E \begin{bmatrix} \tilde{v}_g(s) \\ \tilde{i}_z(s) \end{bmatrix} \quad (21)$$

Substituting (20) into (21), we get

$$\tilde{v}_o(s) = \left(C_c (sI - A)^{-1} B + E \right) \begin{bmatrix} \tilde{v}_g(s) \\ \tilde{i}_z(s) \end{bmatrix} + C_c (sI - A)^{-1} B_d \tilde{d}(s) \quad (22)$$

IV. DERIVATION OF VARIOUS TRANSFER FUNCTIONS FOR NON-IDEAL DC-DC BUCK CONVERTER

The various transfer functions of non-ideal buck converter are derived in this section. From the small-signal model in (18)-(19), nine transfer functions are possible between different input and output variables. However, we will derive only three important transfer function which helps in analyzing output voltage response concerning perturbation in input voltage, load current and duty cycle.

(i) Input voltage to output voltage transfer function:

This transfer function describes that how the variations or disturbances in input voltage affect the output voltage. This transfer function is obtained by setting the perturbations in the duty cycle and output current to be zero in (22).

The input voltage to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \left(C_c (sI - A)^{-1} B_{fc} + E_{fc} \right) \quad (23)$$

B_{fc} and E_{fc} are first column of matrices B and E , respectively. Substituting the corresponding matrices in (23) and simplifying,

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{\frac{RD}{LC(R+r_c)}(r_c Cs + 1)}{s^2 + \left(\frac{1}{L} \left(r_x + r_L + \frac{r_c R}{R+r_c} \right) + \frac{1}{C} \left(\frac{1}{R+r_c} \right) \right) s + \frac{r_x + r_L + R}{LC(R+r_c)}} \quad (24)$$

TABLE I. NON-IDEAL BUCK CONVERTER PARAMETERS

Parameters	Value
Input voltage, V_g	16 V
Output voltage, V_o	12 V
Load resistance, R	11 Ω
Inductance, L/r_L	1.1 mH/0.18 Ω
Capacitance, C/r_c	84 μ F/0.3 Ω
Switch-on resistance, r_{sw}	0.044 Ω
Diode forward resistance, r_d	0.024 Ω
Diode forward voltage, V_F	0.7 V
Duty cycle, D	0.75

(ii) Load current to output voltage transfer function:

This transfer function describes that how the variations or disturbances in load current affects the output voltage. This transfer function is obtained by setting the perturbations in input voltage and duty cycle to be zero in (22).

The load current to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = (C_c(sI - A)^{-1} B_{sc} + E_{sc}) \quad (25)$$

B_{sc} and E_{sc} are second column of matrices B and E , respectively. Substituting the corresponding matrices in (25) and simplifying,

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-R}{LC(R+r_c)} (r_c C_s + 1)(Ls + (r_L + r_x)) \quad (26)$$

$$s^2 + \left(\frac{1}{L} \left(r_x + r_L + \frac{r_c R}{R+r_c} \right) + \frac{1}{C} \left(\frac{1}{R+r_c} \right) \right) s + \frac{r_x + r_L + R}{LC(R+r_c)}$$

(iii) Duty cycle to output voltage transfer function:

It describes that how the variations in duty cycle reflect on the output voltage. This transfer function is obtained by setting the perturbations in input voltage and output current to be zero in (22). This transfer function is used for the control design.

The duty cycle to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = C_c (sI - A)^{-1} B_d \quad (27)$$

Substituting the corresponding matrices in (27) and simplifying,

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{R(V_g + V_F - (r_{sw} - r_d)I_L)}{LC(R+r_c)} (r_c C_s + 1) \quad (28)$$

$$s^2 + \left(\frac{1}{L} \left(r_x + r_L + \frac{r_c R}{R+r_c} \right) + \frac{1}{C} \left(\frac{1}{R+r_c} \right) \right) s + \frac{r_x + r_L + R}{LC(R+r_c)}$$

V. TRANSFER FUNCTIONS FOR IDEAL DC-DC BUCK CONVERTER

By substituting the parasitic elements to zero in the above equations, we get different transfer functions for ideal dc-dc buck converter.

Steady-state model: From (16)-(17),

$$I_L = \frac{V_o}{R} + I_z \quad (29)$$

$$V_o = DV_g \quad (30)$$

(i) Input voltage to output voltage transfer function:
From (24),

$$G_{vg,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{\frac{D}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (31)$$

(ii) Load current to output voltage transfer function:
From (26),

$$G_{vz,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-\frac{s}{C}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (32)$$

(iii) Duty cycle to output voltage transfer function:
From (28)

$$G_{vd,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\frac{V_g}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad (33)$$

The steady-state relationships and transfer functions in (29)-(33) are same as available in the literature [20].

VI. SIMULATION RESULTS

The transfer functions of non-ideal buck converter have different time domain and frequency domain behavior in comparison to ideal buck converter. This comparison will be carried out later in this section.

To obtain the MATLAB simulation results, the parameters of the non-ideal buck converter under consideration are given in Table-I [21]. The non-zero values of parasitic resistances of inductor, and capacitor and forward voltage drop of diode are also given in the table. For ideal dc-dc buck converter, these parasitic parameters are taken as zero. The steady-state value of load current variation (I_z) is assumed zero for the simulation results.

Steady-state model:

The values from Table-I are substituted in steady-state model for non-ideal and ideal cases given in (16)-(17) and (29)-(30), respectively. For ideal case, the inductor current is 1.09A and output voltage is 12V whereas for non-ideal case the inductor current is 1.05A and output voltage is 11.59V. According to these steady-state results, the value of steady-state inductor current and output voltage for non-ideal case is always less than the ideal case. This is due to the voltage drop across the non-ideal elements. The higher the values of these non-ideal elements, the more will be the difference in the steady-state values of both cases.

(i) Input voltage to output voltage transfer function:

By plugging the values of buck converter parameters in (24) and (31) respectively, we get

$$G_{vg,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{199.1s + 7.901 \times 10^6}{s^2 + 1518s + 1.074 \times 10^7} \quad (34)$$

$$G_{vg,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{8.117 \times 10^6}{s^2 + 1082s + 1.082 \times 10^7} \quad (35)$$

It is computed that the ideal buck converter is having two poles and no zero, whereas non-ideal buck converter is having two poles and one real zero. This real zero in non-ideal buck converter does exist due to ESR of the output capacitor. Fig. 2 and Fig. 3 respectively show the Bode plots and step responses for both cases. In both the cases, the system is stable and gain margin is infinite. The phase margin for the ideal case is 34° at gain crossover frequency 667Hz, whereas for non-ideal case, it is 55.4° at gain crossover frequency 634Hz. Thus, non-idealities increase the damping of buck converter and make it more stable and less oscillatory as also seen in the step response.

(ii) Load current to output voltage transfer function:

By plugging the values of buck converter parameters in (26) and (32) respectively, we get

$$G_{vz,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-1.19 \times 10^4 s}{s^2 + 1082s + 1.082 \times 10^7} \quad (36)$$

$$G_{vz,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-0.292s^2 - 1.165 \times 10^4 s - 2.307 \times 10^6}{s^2 + 1518s + 1.074 \times 10^7} \quad (37)$$

In ideal case, there is one zero whereas in non-ideal case it has two-zeros. The Bode plots and step responses of ideal and non-ideal transfer function are shown in Fig. 4 and Fig.5, respectively. The gain margin for ideal case is -20.8dB (at 524Hz) and for non-ideal case, it is -17.6dB (at 533Hz). The phase margin in ideal case and non-ideal case is 84.8° (at 135Hz) and 70° (at 136Hz), respectively. It indicates that the closed-loop uncompensated buck converter will be unstable for the load variations in both the cases.

(iii) Duty cycle to output voltage transfer function:

By replacing the values of different parameters in (28) and (33) respectively, we get

$$G_{vd,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{1.732 \times 10^8}{s^2 + 1082s + 1.082 \times 10^7} \quad (38)$$

$$G_{vd,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{4428s + 1.757 \times 10^8}{s^2 + 1518s + 1.074 \times 10^7} \quad (39)$$

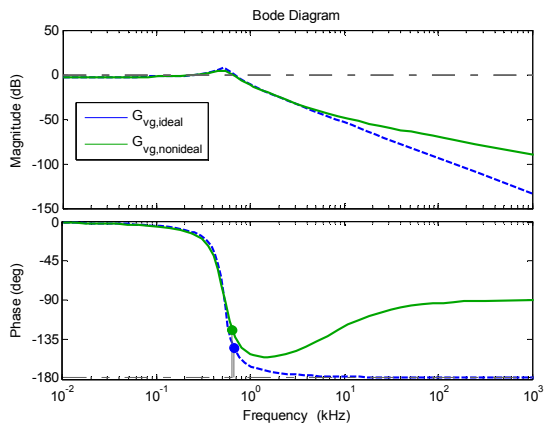


Fig. 2. Bode plots of $G_{vg}(s)$ for ideal and non-ideal buck converter

In this case, non-ideal converter has a real zero which appears due to capacitor ESR. The Bode plots and step responses of ideal and non-ideal buck converter are shown in Fig. 6 and Fig. 7, respectively. As the buck converter is a second-order system, therefore, the gain margin in both cases is infinite. The phase margin in ideal case and non-ideal case is 4.85° (at 2.16kHz) and 26° (at 2.23kHz), respectively. It indicates that the uncompensated closed-loop system will be more stable in non-ideal case. The time response shows that the step response also has less overshoot and oscillations.

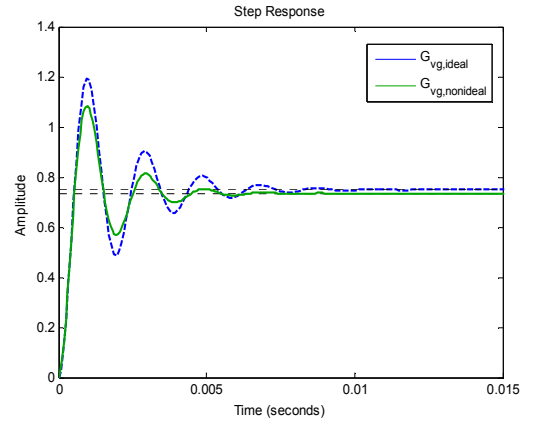


Fig.3. Step responses of $G_{vg}(s)$ for ideal and non-ideal buck converter

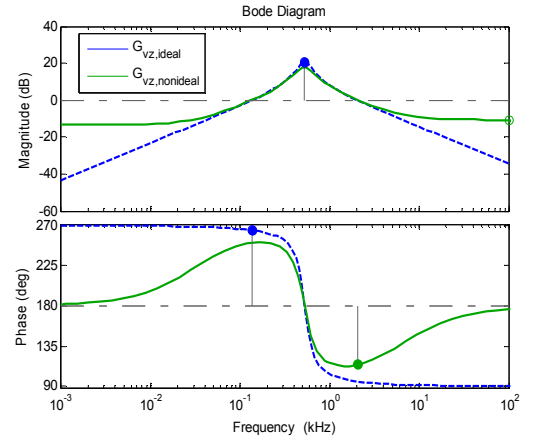


Fig. 4. Bode plots of $G_{vz}(s)$ for ideal and non-ideal buck converter

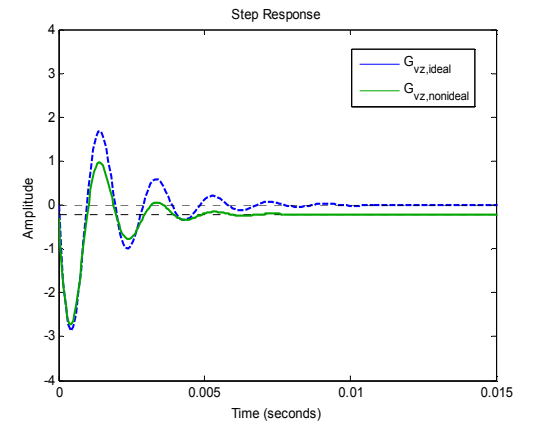


Fig. 5. Step responses of $G_{vz}(s)$ for ideal and non-ideal converter

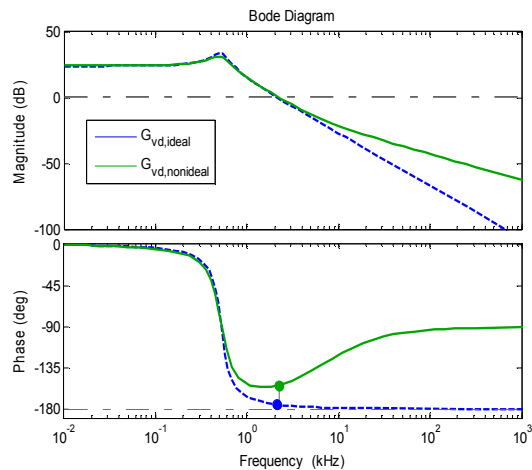


Fig. 6. Bode plots of $G_{vd}(s)$ for ideal and non-ideal buck converter

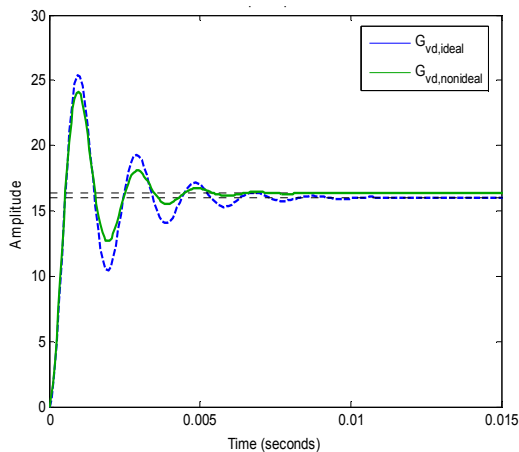


Fig. 7. Step responses of $G_{vd}(s)$ for ideal and non-ideal buck converter

VII. CONCLUSION

The state-space averaging (SSA) technique has been used to derive the transfer functions of non-ideal dc-dc buck converter. The steady-state analysis shows that the inductor current and output voltage values are lesser in non-ideal case because of the voltage drop across the parasitic resistances. The transfer functions models show that the number of poles remains same but the location of poles in non-ideal case is different from ideal case. Also, the number of zeros in non-ideal case is more. This is due to present of ESR in the output capacitor. Bode plots and step responses of the transfer functions shows that responses are better in non-ideal case due to damping provided by the non-ideal elements. These accurate models of buck converter may help in designing a proper feedback control to regulate the output voltage in the presence of various disturbances.

REFERENCES

- [1] C. van der Broeck, R. De Doncker, S. Richter, and J. von Bloh, "Unified Control of a Buck Converter for Wide Load Range Applications," *IEEE Trans. Ind. Appl.*, vol. PP, no. 99, pp. 1–1, 2015.
- [2] J. C. Vilchis, C. Aguilar, and J. Arau, "Multi-mode synchronous buck

- converter with non-uniform current distribution for portable applications," in *IEEE International Power Electronics Congress*, 2008, pp. 114–120.
- [3] R. K. Dokania, S. K. Baranwal, and A. Patra, "Peak current detector based control of DC-DC buck converter for portable application," in *Proceedings of the IEEE INDICON 2004. First India Annual Conference, 2004.*, 2004, pp. 594–596.
- [4] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 559–572, 2006.
- [5] F. C. Lee and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, 2000.
- [6] R. M. Nelms and J. Y. Hung, "Posicast-based digital control of the buck converter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 759–767, Jun. 2006.
- [7] S.-C. Tan, Y. M. Lai, C. K. Tse, and M. K. H. Cheung, "A Fixed-Frequency Pulsewidth Modulation Based Quasi-Sliding-Mode Controller for Buck Converters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1379–1392, Nov. 2005.
- [8] M. Truntic and M. Milanovic, "Voltage and Current-Mode Control for a Buck-Converter based on Measured Integral Values of Voltage and Current Implemented in FPGA," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6686–6699, Dec. 2014.
- [9] F. C. Lee, "Control bandwidth and transient response of buck converters," in *IEEE Power Electronics Specialists Conference*, 2002, vol. 1, pp. 137–142.
- [10] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Design and Performance Analysis of a PWM dc-dc Buck Converter Using PI-Lead Compensator," *Arab. J. Sci. Eng.*, vol. 40, no. 12, pp. 3607–3626, Dec. 2015.
- [11] G. A. Markadeh, J. Soltani, N. R. Abjadi, and M. Salimi, "Indirect output voltage regulation of DC-DC buck/boost converter operating in continuous and discontinuous conduction modes using adaptive backstepping approach," *IET Power Electron.*, vol. 6, no. 4, pp. 732–741, Apr. 2013.
- [12] A. J. Forsyth and S. V. Molloy, "Modelling and control of DC-DC converters," *Power Eng. J.*, vol. 12, no. 5, pp. 229–236, Oct. 1998.
- [13] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching converter power stages," in *IEEE Power Electronics Specialists Conference*, 1976, pp. 73–86.
- [14] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Leverrier's algorithm based modeling of higher-order dc-dc converters," in *IEEE India International Conference on Power Electronics*, 2012, pp. 1–6.
- [15] R. Li, T. O. Brien, J. Lee, J. Beecroft, and K. Hwang, "Analysis of Parameter Effects on the Small-Signal Dynamics of Buck Converters with Average Current Mode Control," *J. Power Electron.*, vol. 12, no. 3, pp. 399–409, 2012.
- [16] A. REATTT, "Steady-state analysis including parasitic components and switching losses of buck and boost DC-DC PWM converters under any operating condition," *Int. J. Electron.*, vol. 77, no. 5, pp. 679–701, Nov. 1994.
- [17] T. Qian, W. Wu, and W. Zhu, "Effect of Combined Output Capacitors for Stability of Buck Converters With Constant On-Time Control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5585–5592, Dec. 2013.
- [18] M. M. Garg, M. K. Pathak, and Y. V. Hote, "Effect of non-idealities on the design and performance of a DC-DC buck converter," *J. Power Electron.*, vol. 16, no. 3, 2016.
- [19] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics-Converters, Applications, and Design*, 3rd ed. John Wiley, 2003.
- [20] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Kluwer Academic Publishers, 2001.
- [21] M. M. Garg, Y. V. Hote, M. K. Pathak, and L. Behera, "An Approach for Buck Converter PI Controller Design Using Stability Boundary Locus," in *2018 IEEE/PES Transmission and Distribution Conference and Exposition (T&D)*, 2018, pp. 1–5.