A Differential Output Switched Capacitor based Capacitive Sensor Interfacing Circuit

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***Abstract*—This paper presents a switched capacitor based capacitive sensor interfacing circuit, which can sense the change in capacitance from differential capacitive sensor and produces differential voltage output. The proposed circuit has the ability to reduce the errors like offset and low frequency noise introduced by the circuit components. The main advantage of this interfacing circuit is, it utilizes a single differential capacitive sensor and a single feedback network to provide differential output. The gain of the interfacing circuit is programmable through the feedback capacitor of the charge amplifier configuration. The interfacing circuit comprises of a fully differential operational amplifier, offset reduction scheme, buffer and low pass filter. The proposed circuit is designed and simulated using UMC 0.18-μm CMOS process technology. Both schematic and post-layout simulation results are presented.**

***Index Terms*—Capacitive sensor, Interfacing circuit, Switched-Capacitor circuits, Application specific integrated circuit (ASIC), Signal conditioning.**

I. Introduction

NOWADAYS most of the electronic devices are smart, because of the sensor integration. Sensing real time analog signal with high precision is a challenging task, where the type of sensor plays significant role. Among the available sensors the capacitive sensors are preferred due to its less tolerance, low temperature coefficient, high resolution, less power dissipation and feasibility to integrate in IC [1]–[4]. Measuring physical signals like acceleration, angular speed, force, position, pressure and strain can be possible with capacitive sensors. Due to micro fabrication technology advancement, micro-electromechanical systems (MEMS) based capacitive sensors are popular for monolithic integration, where sensor and conditioning circuit can be integrated on single silicon die. Particularly MEMS based capacitive accelerometers have numerous applications like consumer electronic systems, biomedical systems, navigational systems and automobiles.

Like each passive sensors, capacitive sensors also require conditioning circuit for generating acceptable voltage signal for processing the measured signal. Differential capacitive half bridge sensing scheme is mostly considered by the researchers, which can improve the accuracy of the measurement by removing the common-mode signals. Signal conditioning techniques like chopper modulation and charge amplifier based switched-capacitor configurations [5] and various circuit topologies are available in literature [6]–[10]. Reference [1] discussed different kind of available circuit topologies and proposed a switched capacitor based interfacing circuit which can provide differential output by utilizing a fully differential operational amplifier (Op-amp), single feedback loop. But this configuration suffers from offset voltage and low frequency noise from the differential Op-amp and the other circuit components.

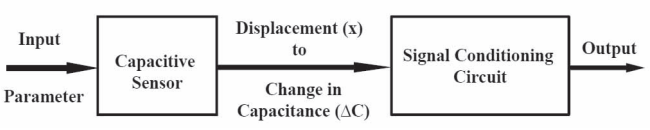

Fig. 1. Block diagram of a capacitive sensor system.

In this work we have analysed the interfacing circuit in [1] and shown that the offset error introduced by the fully differential Op-amp, due to the mismatches of the transistors, degrades the accuracy of measurement and increases the error. We have combined chopper modulation and demodulation with auto-zero technique which reduces the offset error along with low frequency noise to improve accuracy of the complete system. Section II describes a general capacitive sensor system, Section III discusses the proposed signal conditioning circuit, Section IV provides the circuit simulation results.

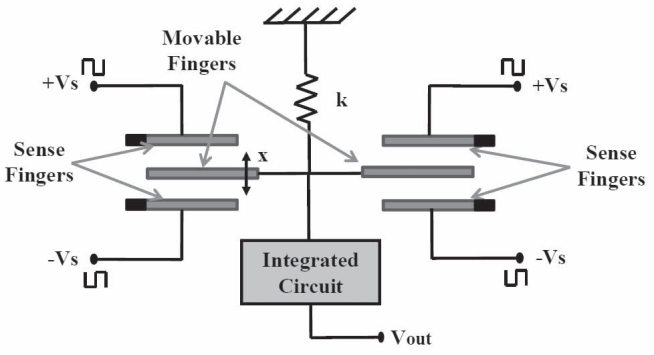

Fig. 2. General model of a capacitive accelerometer.

II. Capacitive Sensor System

In general, a capacitive sensor system consists of a capacitive sensor and a signal conditioning circuit as shown in Fig. 1.

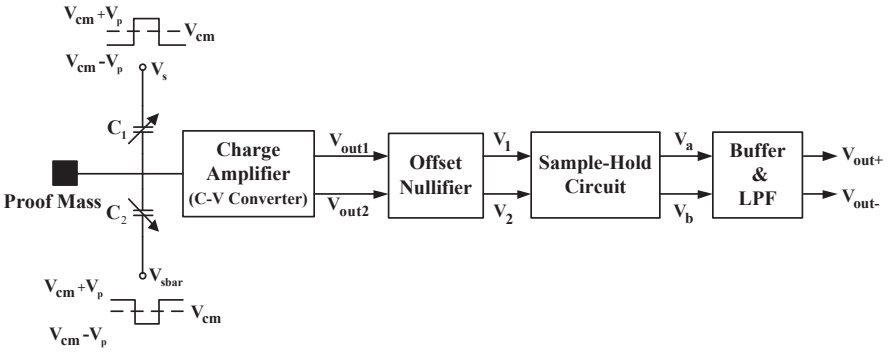

Fig. 3. Block diagram of the proposed architecture.

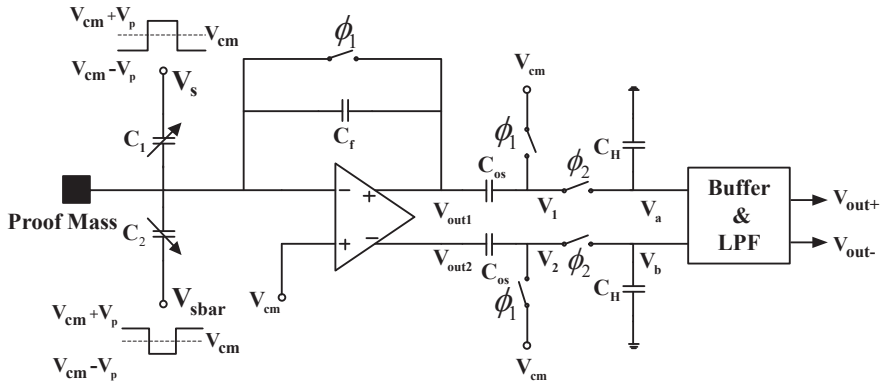

Fig. 4. Schematic of the proposed interfacing circuit.

The capacitive sensor senses the real time physical signal and produces change in capacitance. The amount of capacitance change depends on the intensity of the applied physical signal and the sensitivity of the sensor. The change in capacitance from the sensor is converted to equivalent voltage signal by the signal conditioning circuit, which can be used for further processing. The capacitive sensor can be fabricated using micro-machining technology which can be integrated with the signal conditioning circut to form a complete integrated system. This reduces the size of the complete system as well as cost for bulk requirement.

A general model of a micro capacitive accelerometer is shown in Fig. 2. It is basically a mass, spring and damper system. The proof mass is sensitive to the acceleration and is attached to the movable plate of differential capacitive configuration. Due to acceleration, proof mass moves and displaces the movable plate position towards the fixed sense plates. The direction of capacitor plate displacement is opposite to the applied acceleration, which results the change in capacitance.

III. Signal Conditioning Circuit

The change in capacitance from the half bridge differential capacitive sensor is detected by the signal conditioning circuit and generates output voltage as a function of change in capacitance. While fabricating MEMS half bridge capacitive sensor, there is a possibility of mismatch between two sense capacitors. To overcome this problem on-chip capacitor array can be used to nullify the mismatch [1]. The block diagram of proposed circuit architecture is shown in Fig. 3.

The charge amplifier acts as capacitance to voltage (C-V) converter, which converts the capacitance change to voltage. It provides differential output from a single ended signal, which contains offset error and limits the accuracy of the system. An offset reduction circuit is introduced, which utilizes auto-zero technique to reduce the non-idealities introduced by the charge amplifier. Next is the sample-hold circuit, which demodulates the modulated signal from the charge amplifier and provides the original signal of interest. The demodulated signal is buffered and filtered to remove high frequency noise and produces differential output.

Fig. 4 shows the detailed circuit schematic with fully differential Op-amp. In feedback a switch and a feedback capacitor are placed, which acts as charge amplifier and the gain of amplifier decided by the feedback capacitor.

During phase ϕ_1 the net charge at sensing node is

$$Q_{\phi 1} = (V_{os} - V_p)C_1 + (V_{os} + V_p)C_2 \tag{1}$$

where, Q is the net charge, V_{os} is the offset voltage of the fully differential op-amp, V_p is the peak voltage of excitation square signal and C_1, C_2 are sense capacitors.

$$C_1 = C_0 + \Delta C \tag{2}$$

$$C_2 = C_0 - \Delta C \tag{3}$$

where, C_0 is the nominal capacitance when there is no physical signal, ΔC is the change in capacitance due to the presence of physical signal.

The voltage at V_{out1} and V_{out1} during ϕ_1 can be expressed as

$$V_{out1} = V_{cm} + V_{os} \tag{4}$$

$$V_{out2} = V_{cm} - V_{os} \tag{5}$$

where, V_{cm} is the common mode voltage.

During phase ϕ_2 the net charge at sensing node is

$$Q_{\phi 2} = (V_{os}+V_p)C_1+(V_{os}-V_p)C_2+C_f(V_{cm}+V_{os}-V_{out1}) \tag{6}$$

where, C_f is the feedback capacitance.

Using charge conservation principle and simplifying equations (1) and (6), the single ended outputs can be expressed as

$$V_{out1} = V_{cm} + V_{os} + 4\frac{\Delta C}{C_f}V_p \tag{7}$$

$$V_{out2} = V_{cm} - V_{os} - 4\frac{\Delta C}{C_f}V_p \tag{8}$$

During phase ϕ_1 net charge at the offset nullifier is

$$Q_{\phi 1} = V_{os}C_{os} \tag{9}$$

where, C_{os} is the offset nullifier capacitor.

The offset nullifier voltage during ϕ_1 is

$$V_1 = V_2 = V_{cm} \tag{10}$$

During phase ϕ_2 net charge at the offset nullifier is

$$Q_{\phi 2} = (V_{cm} + V_{os} + \frac{4\Delta C}{C_f}V_p - V_1)C_{os} \tag{11}$$

From equation (9) and (11), offset nullifier output voltages can be expressed as

$$V_1 = V_{cm} + 4\frac{\Delta C}{C_f}V_p \tag{12}$$

$$V_2 = V_{cm} - 4\frac{\Delta C}{C_f}V_p \tag{13}$$

Phase ϕ_2 contains the required signal and can be demodulated by transferring signal during phase ϕ_2 and holding signal during phase ϕ_1. This can be achieved by sample-hold circuit and the output is same as offset nullifier phase ϕ_2 voltage.

$$V_a = V_{cm} + 4\frac{\Delta C}{C_f}V_p \tag{14}$$

$$V_b = V_{cm} - 4\frac{\Delta C}{C_f}V_p \tag{15}$$

The demodulated signal contains high frequency components, which can be suppressed by the low pass filter.

After low pass filter the single ended outputs can be written as

$$V_{out+} = V_{cm} + 4\frac{\Delta C}{C_f}V_p \tag{16}$$

$$V_{out-} = V_{cm} - 4\frac{\Delta C}{C_f}V_p \tag{17}$$

The differential output voltage is expressed as

$$V_{out} = 8\frac{\Delta C}{C_f}V_p \tag{18}$$

The proposed circuit provides higher sensitivity compare to the existing architectures by providing differential output from a single ended signal and reduces the offset as well which improves the accuracy of measurement.

IV. Simulation Results

The proposed circuit is designed and simulated in UMC 0.18-μm CMOS process technology. We have intentionally included an external offset voltage of $10\ mV$ at the input of the differential Op-amp to verify the performance of the proposed configuration. For simulation, $200\ Hz$ a.c. change in capacitance variation is given in the differential capacitance sensor configuration along with the following parameters: $C_0 = 5\,pF,\ \Delta C_p = 100\,fF,\ C_f = 4\,pF,\ V_p = 0.9\,V,\ V_{cm} = 0.9\,V$.

Simulation results without the offest reduction scheme and with the offest reduction scheme are shown in Fig. 5 and Fig. 6 respectively. Waveforms at different circuit nodes are also shown in both the figures. The simulation results show that the proposed circuit effectively reduced the offset and improves the sensitivity as expected from the theoretical analysis. The gain programmability of the proposed configuration is verified by varying the feedback capacitor as shown in Fig. 7.

Layout of the proposed circuit is also carried out in UMC 0.18-μm CMOS process technology, takes about $0.45\ mm^2$ of silicon area, shown in Fig. 8. Fig. 9 compares the post layout simulation result with the schematic simulation. The

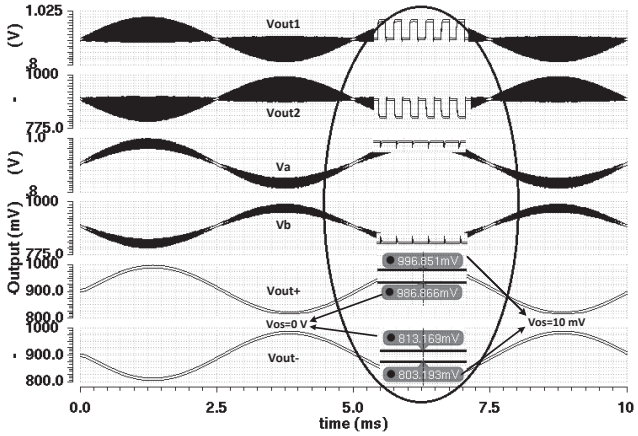

Fig. 5. Simulation results without offset reduction scheme.

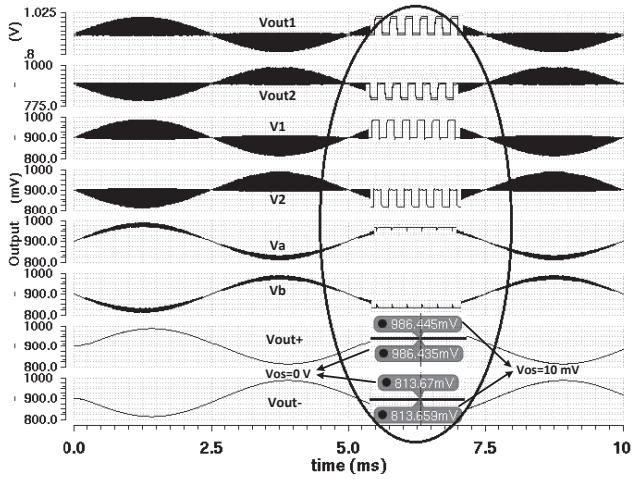

Fig. 6. Simulation results with offset reduction scheme.

deviation is due to the extracted parasitic components in the layout.

V. Conclusion

A switched capacitor based capacitive sensor interface is proposed in this work. The proposed configuration combines synchronous chopper modulation and demodulation and auto-zero technique to reduce the offset and noise in the circuit. It also provides differential output by utilizing a fully differential operational amplifier with a single feedback loop and one differential sensor arrangement. The circuit is implemented in UMC 0.18-μm CMOS process technology and simulation results are presented. The schematic simulation is also compared with the post-layout simulation result. From the the simulation results, it is observed that the proposed circuit is capable of reducing the offset while improving the accuracy of the system.

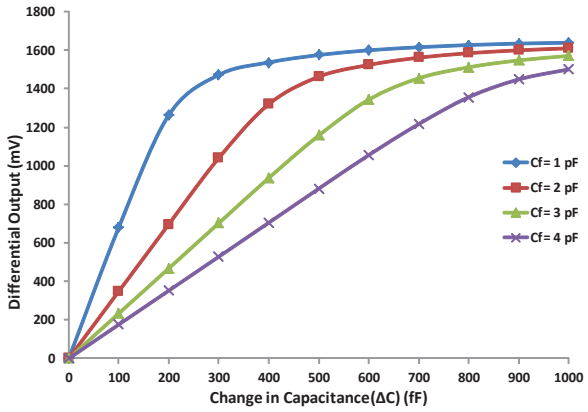

Fig. 7. Differential output with varying sensitivity.

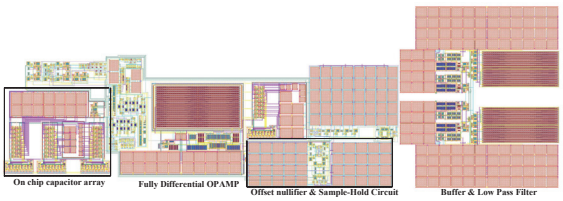

Fig. 8. Layout of the proposed circuit.

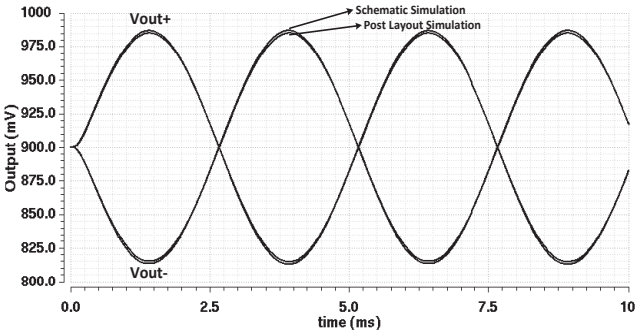

Fig. 9. Comparison between schematic and post layout simulation results.

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