Investigation on the Performance of PV-UPQC under distorted current and voltage conditions

[1]Santanu Kumar Dash, [2]Pravat Kumar Ray
Department of Electrical Engineering
National Institute of Technology Rourkela, Rourkela, India, 769008
[1]santanu4129@gmail.com,[2]rayp@nitrkl.ac.in

***Abstract*— The design, configuration and control of photovoltaic interfaced unified power quality conditioner (PV-UPQC) is discussed in this paper. PV-UPQC is employed to maintain power quality under various current and voltage distortion. PV-UPQC is a multi objective type power conditioning device, which has both shunt and series voltage source converter with a common DC-link. Moreover the photovoltaic system is connected at the DC-link of UPQC to provide power to the load. This paper also proposes a modified synchronous reference frame scheme with an improved phase locked loop (PLL) for control of the UPQC to eliminate power quality issues like unbalanced grid voltage with harmonics, load step change and load harmonics. The dynamic behavior of PV-UPQC under irradiance change is also investigated. The system is simulated and results are presented to validate the efficiency and performance of PV-UPQC.**

***Index Terms*—PV-UPQC, power quality, voltage harmonics, current harmonics, Solar PV**

I. INTRODUCTION

The presence of highly distorted loads at the consumer side makes the power system polluted and various power quality issues arise. Power quality improvement has become major point of focus for researcher nowadays. The integration of renewable energy to the grid with power electronic interfacing system also provides a wide area for power quality improvement. The current perturbations introduced by the loads, grid side voltage quality issues; unbalanced and highly distorted load conditions are major point of focus.

Elimination of the power quality issues requires compensating systems. According to various types of power quality issues, special category of power conditioners have been used as reported in the literature [1]-[3]. The custom power devices have been reported as power conditioners with its various categories. Dynamic voltage restorer (DVR) and Distribution static compensator (DSTATCOM) are developed specially for voltage quality issues and current quality issues respectively [4]-[5]. However, Unified Power quality conditioner (UPQC) combines the functionality of both DVR and DSTATCOM [6], [7]. The UPQC configuration has back to back connected DVR and DSTATCOM, with a common DC-Link. Therefore UPQC become capable to deal with current and voltage quality issues perfectly.

Various topologies for Photovoltaic (PV) grid integration with active filtering capability are reported in [8]-[10]. The integration of Solar PV with UPQC is also reported in [11], [12]. However, PV-UPQC topology is very few in literature. Interfacing of solar energy to the grid through UPQC, increases the utilization and functionality of UPQC. In this case part of the load power is supplied by PV. Literature survey reports about only a few papers about this PV-UPQC configuration. Thereby a detail analysis and performance evaluation is needed.

Control algorithm for UPQC has been studied and implemented in literatures includes instantaneous reactive power theory, synchronous reference frame algorithm, unit vector template algorithm [12]-[14]. To make PV-UPQC systems become more sensitive towards highly distorted conditions of load and source voltage, this paper introduces a modified SRF control algorithm. In this paper the design of PV-UPQC system is along with proposed controller is discussed. The solar PV is interfaced with UPQC through DC-DC boost converter at the DC-link. To extract maximum power from PV Perturb & Obserb (P&O) MPPT algorithm [15] is utilized in the present system. Conventional systems with traditional PLL behave properly under normal distortions, but it becomes helpless during high distortions. Therefore this paper proposes an improved PLL mechanism for highly distorted load and voltage conditions, which work along with SRF control algorithm.

The paper is organized as follows: section II includes the detail configuration of PV-UPQC, with structure involving back to back converters connected at the common DC-Link. The Solar PV array with boost converter interfaced with UPQC at DC-Link. Detail design specification of various parameters of the system is evaluated in Section III. Modified SRF control algorithm is explained in Section IV. Simulation results are discussed in Section V and finally conclusions in Section VI.

II. SYSTEM CONFIGURATION OF PV-UPQC

The configuration block diagram of PV-UPQC is shown in Fig.1. The PV-UPQC consists of a shunt voltage source converter and a series voltage source converter. Both shunt and series VSC share a common DC link capacitor. Shunt VSC is connected at the load side through interfacing inductors. Similarly Series VSC connected in series with the grid through

interfacing inductors. The series transformer is used for injecting the voltage signal by series VSC. The shunt VSC is connected at the point of PCC at the load side to compensate the load current harmonics and to feed the PV power to load.

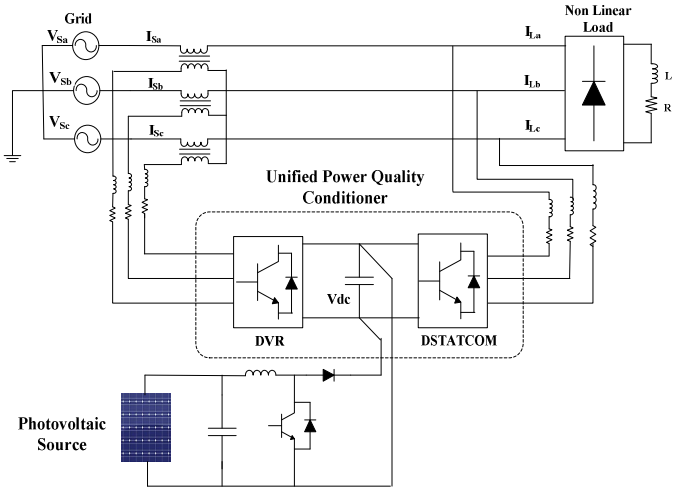


Fig.1 PV-UPQC Configuration

III. DESIGN SPECIFICATION OF PV-UPQC

There are various parameters involved in selection of appropriate specification of DC-bus voltage, sizing of DC-bus capacitor value, interfacing inductor of DSTATCOM and DVR, selection of inductor of DC-DC boost convertor and PV array design.

A. Selection of DC-bus voltage:

The DC-link capacitor present in the PV-UPQC is common to shunt inverter, series inverter as well as Solar PV array. The selection of DC-link voltage magnitude should be evaluated such that its value will be double the peak of phase voltage of the 3-ph system. Therefore DC-bus voltage magnitude is presented as:

$$V_{dc} = \frac{2\sqrt{2}V_L}{\sqrt{3}m} = \frac{2\sqrt{2}\times 415}{\sqrt{3}.1} = 677.692 \qquad (1)$$

where 'm' is the depth of modulation selected as 1 and Vl is the line voltage. It is evaluated that the minimum V_{dc} to be 677.7V and the DC-bus is selected as 700V.

B. Interfacing inductor of DSTATCOM:

Depending on the ripple current, converter switcing and DC-link voltage, inductor value is evaluated. The expression is given as:

$$L_f = \frac{\sqrt{3}mV_{dc}}{12af_s.I_{rip}} \qquad (2)$$

where m is modulation depth, a is value of maximum overload, f_s is switching frequency. After calcualtion the inductor value is 2.5mH. the value selected for simulation is 3.5mH.

Other design parameters also selected in a similar specific manner. The PV Array specification is presented in Table I.

TABLE I PV ARRAY SPECIFICATION

Maximum Power P	17kW
Open circuit voltage V_{oc}	860 V
Short circuit current I_{sc}	26.8A
Voltage at maximum power V_{mp}	705.2V
Current at Maximum power point I_{mp}	25.5A
Parallel Strings	3
Series module in Strings	26

IV. CONTROL ALGORITHM

Several active filtering methods have been presented in the literature with the SRF based control algorithm due to its easy implementation and efficiency. However this SRF methodology becomes helpless during highly distorted voltage and current perturbations. This paper introduces a new SRF methodology with an advanced PLL scheme. The proposed SRF scheme for the PV-UPQC is shown in Fig.3 and Fig.4.

A. Improved PLL Mechanism

Phase Locked Loop algorithms are employed for phase detection of the grid voltages and for the extracting the fundamental system voltage signals. Various PLL techniques are introduced with controllers for better control of power conditioners. However, conventional PLL techniques are found to be less efficient for highly distorted system voltage conditions such as voltage sags, voltage swells. Therefore present paper introduces an improved PLL technique to extract the fundamental sequence of system voltage. As the power system become more polluted with voltage profile disturbances, UPQC performance and efficiency needs to be improved with advanced PLL circuit. The improved PLL evaluates three phase auxiliary total power by employing instantaneous three phase source voltages, which results in determination of transformation angle of supply grid voltage. The improved PLL technique is designed perfectly to operate properly during various distorted voltage conditions. The three phase grid voltages are sensed, measured and used as input signals for the PLL. The transformation angle is evaluated as output for PLL circuit. The evaluated line voltages are multiplied by auxiliary feedback currents along with unity amplitude and three phase auxiliary instantaneous active power is determined. The improved PLL technique can behave satisfactorily during distorted grid voltage conditions depending upon perfect tuning of PI gains of present PLL scheme.

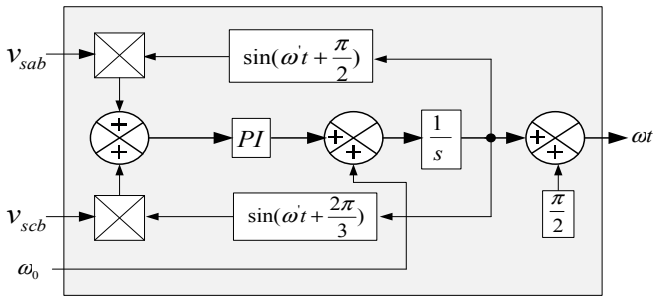


Fig.2 Improved PLL Scheme

The improved PLL circuit is implemented with SRF Control scheme for PV-UPQC in the present research work. The applied method has shown its effectiveness under highly distorted and unbalanced load conditions.

B. Reference signal generation for series APF

The control methodology implemented is based on SRF algorithm and improved PLL scheme presented in Fig.3. The grid voltage is sensed and converted to d-q-0 frame with the utilization of matrix D presented in (8). The obtained v_{sd} and v_{sq} contains the ossilating components $\tilde{v}_{sd}$ and $\tilde{v}_{sq}$ as well as average components $\bar{v}_{sd}$ and $\bar{v}_{sq}$. These component inclusions are due to the unbalanced grid voltage with harmonics. The presence of ossilating components $\tilde{v}_{sd}$ and $\tilde{v}_{sq}$ shows the inclusion of harmonics and negetive sequeence components of the grid voltages due to distorted load conditions. The average component indicate about the presence of positive sequence components of the voltages. The unbalanced grid voltages referes to presence of zero sequence component v_{s0}. The d-axis component include both avarage and oscillating components presented in (5).

$$D = \sqrt{\frac{2}{3}}\begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (3)$$

$$D^{-1} = \sqrt{\frac{2}{3}}\begin{bmatrix} \frac{1}{\sqrt{2}} & \sin(\omega t) & \cos(\omega t) \\ \frac{1}{\sqrt{2}} & \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (4)$$

$$v_{sd} = \bar{v}_{sd} + \tilde{v}_{sd} \quad (5)$$

The reference load voltages have been evaluated through the inverse transformation matrix D^{-1}. The grid voltage positive sequence component is passed through the low pass filter to obtain the average value. The zero and negative sequence part are considered as zero to eliminate the voltage harmonics, voltage unbalances and distortions. The evaluated load reference voltages $v^*_{La}, v^*_{Lb}, v^*_{Lc}$ are compared with actual load voltages v_{La}, v_{Lb}, v_{Lc} in sinusoidal PWM controller to generate switching signals for insulated gate bipolar transistor (IGBTs) of DVR.

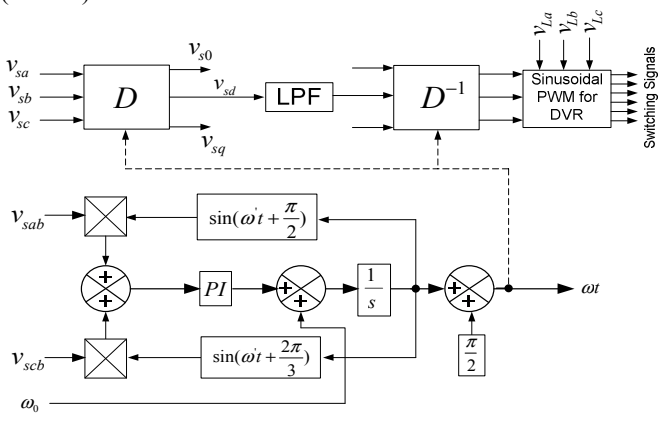


Fig.3 Control algorithm of DVR

The load reference voltages and actual sensed load voltages are compared in sinusoidal pulsewidth modulation to generate the gate pulses.

C. Reference signal generation for DSTATCOM

The shunt APF of the PV-UPQC is employed for extraction of power from the PV system by maximum power point tracking algorithm which generates reference for DC link of the PV-UPQC. Various MPPT algorithms are studied in the literature [11], for this research work P & O algorithm is used. However a PI controller is engaged to maintain DC link at reference level. Due to the presence of the non linear loads load current become contaminated with harmonics. Therefore compensation of load current harmonics and sinusoidal source current maintenance is desired. Various control algorithms have been implemented for extraction of fundamental active component of load current.

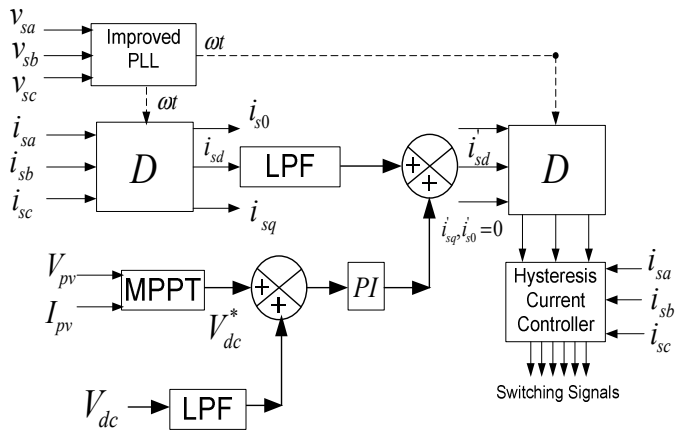


Fig.4 Control algorithm of *DSTATCOM*

The discussed SRF based control algorithm requires grid currents and transforms them to d-q-0 coordinates given as:

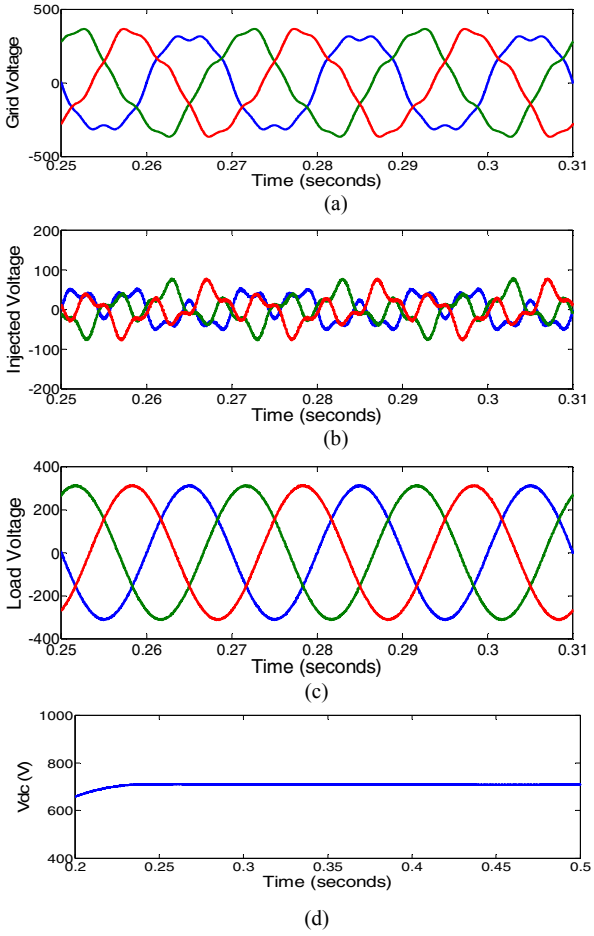
$$\begin{bmatrix} i_{s0} \\ i_{sd} \\ i_{sq} \end{bmatrix} = D \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \quad (6) \qquad , \qquad \begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = D^{-1} \begin{bmatrix} 0 \\ i'_{sd} \\ 0 \end{bmatrix} \quad (7)$$

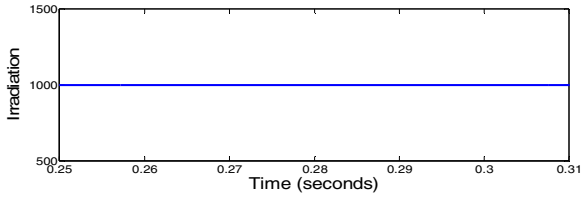
The transformation utilizes the improved PLL scheme. In the present methodology zero and negative sequence component of the source current reference in 0-axis and q-axis are set to zero to normalize the harmonics, unbalances in source current. The reference source currents can be calculated by the equation (7). The generated reference currents and the actual source currents are compared by hysteresis current controller to generate switching signals. The detail controller is given in Fig.4.

V. Simulation Results and Discussion

The performance of PV-UPQC is analyzed and evaluated for various conditions in this section. The system PV-UPQC is simulated through Matlab/Simulink. A nonlinear load is connected to the system and the detail design parameter is presented in the Appendix.

A. PV-UPQC under unbalanced grid voltage with harmonics





(e)

Fig.5 Unbalanced and distorted grid voltage (a); Compensating Signal (b); balanced load voltage (c); DC Link voltage (d); PV Irradiance(e).

The presence of unbalanced grid voltage with harmonics is shown in Fig.5 (a), the injected signal from series inverter is given in Fig.5(b). The compensation by PV-UPQC maintains the load voltage at constant level shown in Fig.5(c). It is assumed that the PV irradiance is constant at 1000W/m^2.

B. PV-UPQC under unbalanced grid voltage

Presence of unbalanced grid voltage makes the load voltage also unbalance presented in Fig.6 (a) which is eliminated by DVR injected voltage shown in Fig.6 (b). Load voltage after compensation is shown in Fig.6(c).

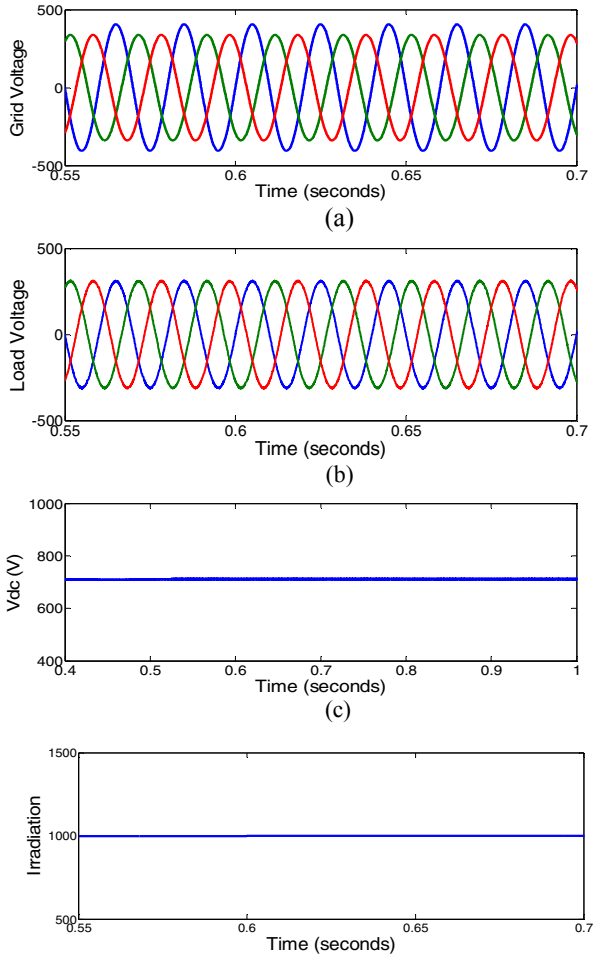


Fig.6 Unbalanced grid voltage (a); balanced load voltage (b); DC Link voltage (c); PV Irradiance(d).

C. PV-UPQC under nonlinear load step change

Nonlinear loads inject harmonics to the source current and make it polluted. Harmonic rich load current with sudden change in load shown in Fig.7 (a) and sinusoidal source current after compensation given in Fig.7(c).

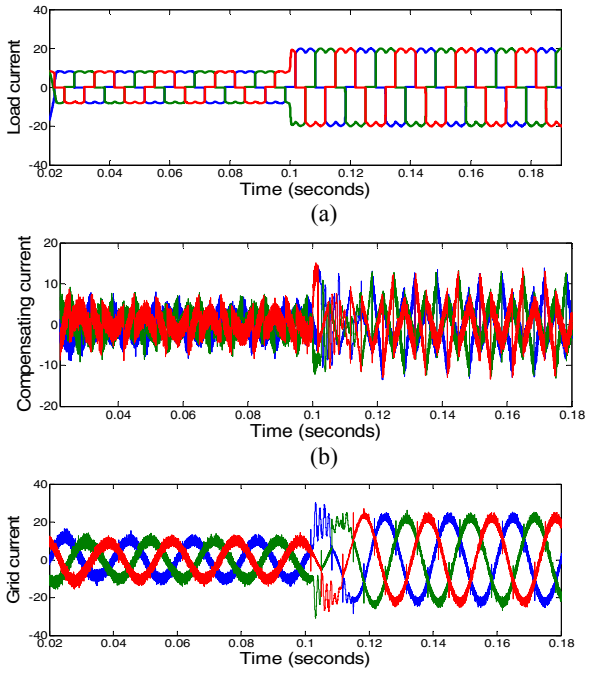


Fig.7 Unbalanced grid voltage (a); Compensating Signal (b); balanced load voltage (c).

D. PV-UPQC under change in Irradiation

Increase or decrease in irradiance affects directly current drawn by the load from the grid. Decrease in solar irradiance force the load to draw more current from grid.

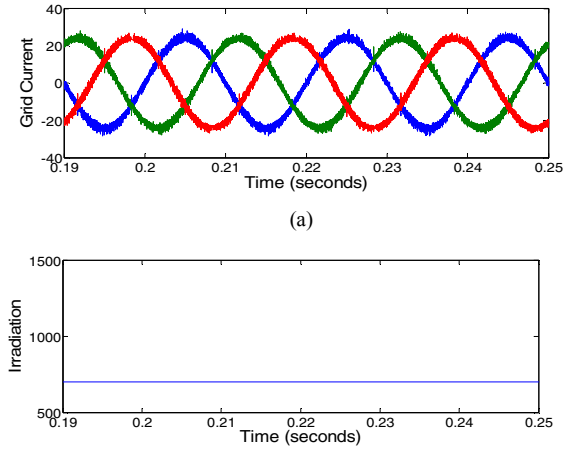


Fig.8 Decrease in Solar Irradiance (a); Increase in current drawn from grid (b).

VI. CONCLUSION

The performance of PV-UPQC is evaluated in this paper. A SRF based control algorithm with improved PLL mechanism is presented. Unbalanced load voltage with harmonics and purely unbalanced load voltages have been compensated and balanced load voltage is maintained by PV-UPQC. Harmonic rich source currents are compensated even under load change conditions. The system is noticed to be stable and load voltage is maintained at desired level even under variation of solar irradiance. Therefore Solar PV integrated with UPQC has shown satisfactory performance for power quality improvement.

APPENDIX: System parameters of PV-UPQC

Line voltage: 415V,50Hz;Source impedance:0.15mH,0.25Ω; Load: 60Ω,30mH; DC-Link voltage:700V; DC-Link capacitance $5000\mu F$; Shunt VSC interfacing inductor: 3.5mH,Series VSC interfacing inductor: 6.5mH, Ripple filter: 9μF,10Ω switching frequency: 20kHz.

REFERENCES

[1] Gayadhar Panda, Pravat Kumar Ray, Pratap S Puhan, Santanu K Dash "Novel schemes used for estimation of power system harmonics and their elimination in a three-phase distribution system" International Journal of Electrical Power & Energy Systems 53, pp. 842-856, 2013.

[2] Hurng-Liahng Jou, Jinn-Chang Wu, Yao-Jen Chang, Ya-Tsung Feng " A novel active power filter for harmonic suppression" *IEEE Trans on Power Delivery*,vol.20, no.2, pp. 1507-1513. April.2005.

[3] Gayadhar Panda, Santanu Kumar Dash, Nirjharini Sahoo "Comparative performance analysis of Shunt Active power filter and Hybrid Active Power Filter using FPGA-based hysteresis current controller" IEEE 5th India International Conference on Power Electronics (IICPE), Dec.2012.

[4] Soumya Mishra, S. K. Dash, P. K. Ray "Performance analysis of L-type PV-DSTATCOM under ideal and distorted supply voltage" 2016 IEEE Students Technology Symposium (TechSym), Sep.2016.

[5] A Ghosh, G.Ledwich "Compensation of distribution system voltage using DVR" *IEEE Trans on Power Delivery*,vol.17, no.4, pp. 1030-1036.Oct.2002.

[6] S K Dash, S Mishra, P K Ray "Photovoltaic tied unified power quality conditioner for mitigation of voltage distortions" IEEE ICCECE, Dec. 2016.

[7] S.Devassy, Bhim Singh "Dynamic Performance of Solar PV integrated UPQC-P for Critical Loads" IEEE INDICON, Dec.2015.

[8] Soumya Mishra, Pravat Kumar Ray "Power Quality Improvement Using Photovoltaic fed DSTATCOM Based on JAYA Optimization" *IEEE Trans. on Sustainable Energy*, vol. 7, no. 4, pp.1672-1680, Oct 2016.

[9] S.K Dash, P.K. Ray "Design and Analysis of grid connected Photovoltaic fed Unified Power Quality Conditioner" Int. J. of Emerging Electric Power Sys. vol.17, no.3, pp. 301-310, April 2016.

[10] M.Kesler, E.Qzdemir "Synchronous Reference Frame Based control method for UPQC Under unbalanced and distorted load conditions" *IEEE Trans on Indus.Electronics*, vol. 58, no. 9, pp.3967-3975, Sep. 2011.

[11] Pallavee Bhatnagar', R.K.Nema: "Maximum power point tracking control techniques: State-of-the-art in photovoltaic applications", IEEE Trans. Renewable and Sustainable Energy no.23, pp- 224-241, 2013.