A Low Power Square-Wave Generator with Wide Tuning Range for Instrumentation Applications

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***Abstract*—In this paper a waveform generator with wide low frequency tuning range is presented. Due to its low-frequency tuning range, it finds various applications in biomedical devices, used to treat many diseases and disorders. The waveform generator (WFG) consists of hysteresis Schmitt trigger and gm-C integrator. The WFG circuit is implemented using UMC 180 nm CMOS process technology, operating with single supply voltage of 1.8 V. The amplitude and frequency of WFG can be controlled independently through bias voltage as well as bias current adjustment. Amplitude tuning range of 0.9 V_{P-P} is achieved while the nominal frequency is at 10 kHz. Low frequency range of 7 kHz – 1318 kHz is achieved by adjusting bias voltage or by varying bias current IB4 from 220 nA – 58 uA.**

Keywords— WFG, low-frequency, hysteresis Schmitt trigger, gm-C integrator, amplitude control, frequency control

I. INTRODUCTION

In recent times, demand for small size healthcare electronic devices is increasing; a major plunge is given in direction of technological advancement for biomedical devices. Designing any IC chip with low power, smaller size and higher speed is major concern in these days. Advancement of CMOS technology enables the researchers to design power-efficient and low cost WFG for various biomedical as well as low frequency applications. These WFGs can also be a part of implantable devices and used in treatment of various diseases and disorders. The WFG is used in cardiac pacemaker as a source of low frequency, which has to provide electrical stimulation to improve heartbeat. It is also necessary in hearing aid systems for the hearing impaired people. WFGs can be used in micro-machined resistive and capacitive sensors as well. Generally, WFG generates a low frequency square/triangular waveform whose amplitude and frequency can be controlled using appropriate biasing current or component parameter [1]. Waveform shape, periodicity, speed and component parameters are considered in any WFG design. Multiple WFGs can be designed using a simple oscillator with significant amount of positive feedback. But designing a WFG for low power applications is a challenging task. Relaxation oscillator is one of the low power oscillators, which is used in wireless systems, low power signal processors and sensors. Selection of CM (current mode) and VM (voltage mode) technique for WFG design is also an important issue, because it affects the overall performance. WFG can be designed using CM technique with high linearity, low power and better simplicity as compare to VM technique. The voltage mode circuits using operational amplifiers suffer from poor frequency stability and low slew rate. Further, CM WFG designed with Schmitt trigger uses one more building block like Current Conveyors (CCII-second version) [2], Operational Trans-conductance Amplifiers (OTA) [3] [4] [5] [6] [7], Operational Transresistance Amplifier [8] [9]. WFG designed with current conveyor (CCII), exploit good frequency stability by adjusting the ratio of passive elements that been used in the circuit. The amplitude and frequency of these realizations are mainly controlled by the passive elements. But in fully on-chip design, it is very difficult to maintain the values of these passive elements, as their values will surely deviate due to PVT (Process, Voltage and Temperature) variation. In CCII, matching of passive elements is required, which increases complications in the design. Due to this problem CCII ruled out by operational transconductance amplifiers (OTA). In this design OTA is used with Schmitt trigger, where OTA makes design more robust, simple and also provides good frequency stability. The frequency and amplitude of the generated waveform can be controlled by bias currents. So, WFG designed with OTA, consists bias currents as controlling parameters. One advantage of using OTA is, to generate low frequency range with smaller g_m values [10]. In this realization, OTAs are used like a switching current source for charging and discharging the capacitor followed by a Schmitt trigger circuit. This circuit implementation shows excellent frequency stability as its frequency is determined by the ratio of bias currents. Moreover it requires a single supply of 1.8 V compared to other designs where dual supply is required [2] [4].

II. CIRCUIT DESIGN AND TOPOLOGY

Amplifier with positive feedback is used as waveform generator. Proposed WFG, composed with hysteresis Schmitt trigger, shown in Fig. 1, forms positive feedback and bias resistance R, gm-C integrator forms negative feedback (due to output terminal of integrator is connected to inverting terminal (V_{in2-}) of Schmitt trigger). Transistors M1 and M2 forms basic differential amplifier, M3 and M4 acts as active loads by forming basic current mirror configuration. Transistors M5 and M6 are common source PMOS transistors belongs to gain stages STG2 and STG3 respectively, used for amplification purpose. The STG1, STG2 and STG3 are cascaded together as voltage amplifiers and with resistor R, these are connected in positive feedback to form a hysteresis Schmitt trigger, which determines the amplitude of the generated square waveform. The generated Square waveform V_{WFG} has oscillation frequency around 10 kHz and peak-to-peak output voltage of around 0.9 V, which fed as input to gm-C integrator to generate

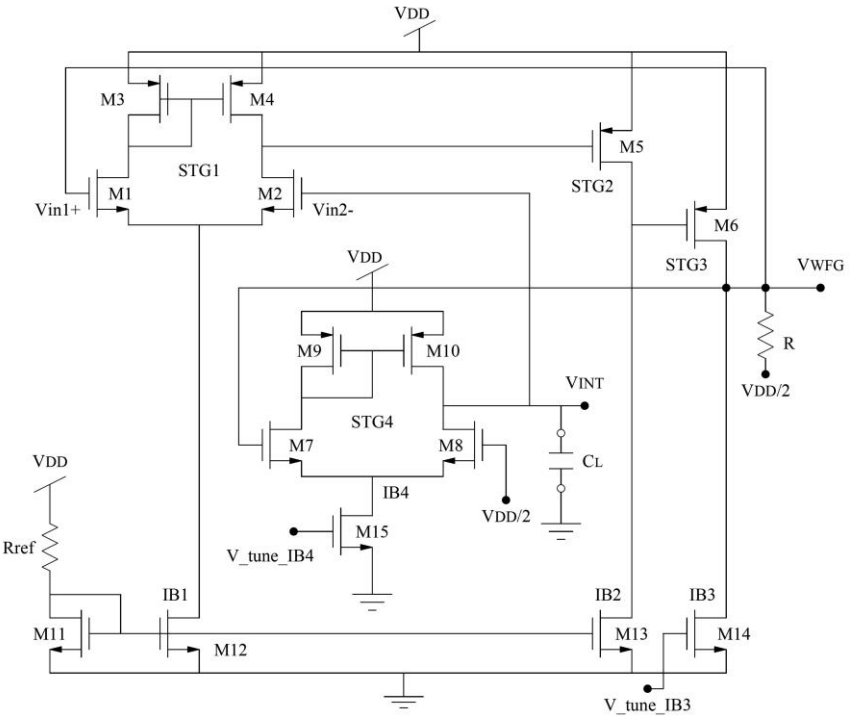

Fig. 1. The core square/triangular waveform generator (WFG) circuit

ramp waveform V_{INT}. Ramp waveform is generated by constant charging and discharging of load capacitance with bias current (IB4) provided by gm-C integrator. This bias current IB4 controls the transcondutance (gm) of OTA. The gm-C integrator is an important part of WFG and a first order gm-C integrator building block (STG4) has been used as a part of the timing circuit. In WFG, single ended gm-C topology is utilised, which offer high input impedance, wide bandwidth, high slew-rate. With inverting terminal of STG1 it forms a negative feedback and controls the waveform frequency. In order to have better amplification, transconductances of first three gain stages should be selected very high, which can be achieved with relatively larger aspect ratio. Transistors M1, M2 and M7, M8 in the input stage of Schmitt trigger and integrator respectively should be properly matched. Transistors M11 and M12 form a basic current mirror and provide constant bias current IB1. The values of W/L of M11, M12 and R_{ref} should be selected according to requirement of IB1. Bias currents of STG1, STG2, STG3 and STG4 are IB1, IB2, IB3 and IB4 respectively. These bias currents play crucial role in amplitude and frequency control of square waveform. The NMOS M14 provides a bias current IB3, which controls the amplitude of waveform and the NMOS M15 used a voltage controlled current source which provides biasing current IB4 to gm-C integrator, which controls the frequency of waveform. These bias currents are controlled by gate voltages V_tune_IB3, V_tune_IB4 of transistors M14, M15 respectively. We can see that gm controls the oscillation frequency, and wide range of variation in gm is achieved by tuning IB4. So transconductance (gm) design is an important aspect in gm-C integrator design. A wide-range of frequencies can be achieved by tuning the gm of the integrator. In general, the W/L ratios and transconductances of transistors at input stage of integrator should be relatively high.

A. WFG Circuit Operation

From Fig. 1, we observe that there is no additional input to hysteresis Schmitt trigger, the positive feedback is responsible for generation of square waveform, when triggered by noise. The operation is shown in Fig. 2. Schmitt trigger has two quasi-stable states V_{max} and V_{min}, in which the output is transient. Consider the V_{WFG} is initially at V_{max} and holds this state for duration T1. This voltage appears at non-inverting terminal V_{in1+} of Schmitt trigger. Initially output of integrator (V_{INT}) is at lowest level V_{INTL} and connected to inverting terminal V_{in2-} of Schmitt trigger. Basically V_{INT} is the voltage across the load capacitor C_L. At t=0, the difference between inputs V_{in1+} and V_{in2-} is relatively large, so most of the bias current IB1 flows through M1, and M2 will turn off because at that point $V_{GS2} < V_{TN2}$, which drives M4 into deep triode region. So the output of STG1 becomes vicinity to V_{DD}, which again fed as input to PMOS transistor M5, and becomes in cut-off region. So the drain current of M5 will be zero, and in this situation the bias current IB2 will charge the gate of PMOS M6 up to some positive voltage which drives M6 in deep triode region results in $V_{WFG} \approx V_{DD}$. Within same duration this output voltage is supplied to non-inverting terminal (gate of M7) of integrator and inverting terminal (gate of M8) of integrator is at 0.9 V. In this case M7 allows more bias current IB4, there by current through M8 will be very-very small (it will be barely on). The drain current of M7 will be almost equal to IB4 and this current will be mirrored using M9, M10 to the output of integrator. This current IB4 now will charge load capacitance from V_{INTL} to V_{INTH}, so V_{in2-} also changes with same rate. The difference between V_{in1+} and V_{in2-} will eventually decrease and

M2 will also conduct part of IB1. At t = t1, V_{WFG} changed to V_{min} and remain for duration T2 and C_L is fully charged and V_{INT} is at V_{INTH}, now M2 will conduct most of IB1.

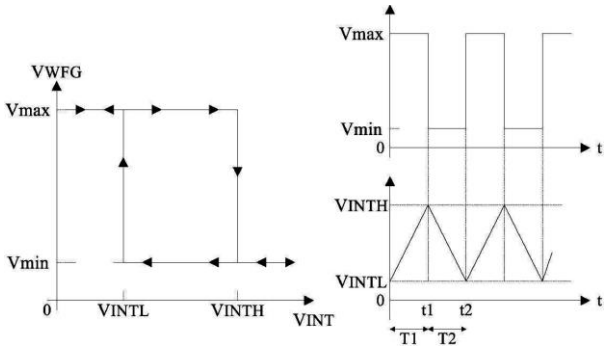

Fig. 2. Transfer characteristic of the core Schmitt trigger (LHS), in relation to the square and triangular wave-shapes of the waveform generator (RHS)

The potential at gate of M5 will be some positive voltage and so M5 will behave as closed switch. The gate of M6 will be at V_{DD} and so M6 will be turned off. Now the most of IB3 will flow through resistor R. The minimum output voltage V_{min} achieved by circuit will be approximately equals to 0.9-IB3*R. Now when V_{WFG} is at V_{min} capacitor will discharge from V_{INTH} to V_{INTL}, providing linear ramp voltage. As V_{INT} will decreases, so does V_{in2-}. And when it approaches V_{in1+}, then M1 starts conducting. If the magnitude of V_{INT} is greater than V_{INTL} then V_{WFG} will remain at V_{min} and when magnitude of V_{INT} approaches V_{INTL} then eventually, the output V_{WFG} becomes V_{max}.

III. Simulation Results and Discussion

The proposed square/triangular waveform generator with amplitude and frequency tuning was simulated using Cadence Virtuoso using UMC 180 nm CMOS process technology. The overall performance of WFG depends upon gain stage which comprises Schmitt trigger and common source amplifiers. Input differential pair (M1, M2) must have larger W/L ratios and must be properly matched for equal transcondutances for proper amplification. The W/L ratios of M5, M6 also must be selected very high, so that they can provide larger voltage gain. The channel length of all transistors in gain stage is kept at 300 nm. In order to obtain larger output swing, widths of M3, M4 is taken large, which gives W3 = W4 = 15 um. And minimum channel length 2.25 um and width 5 um is taken for input transistors (M7, M8) of integrator (STG4). M14, which provides bias current IB3 is used for amplitude tuning. W/L ratios of PMOS current mirror in gm-C integrator not necessarily has to be same rather we have small mismatch in aspect ratios. Due to this mismatch the duty cycle of the V_{WFG} can then be controlled by varying the width of PMOS load M9. Here wider the device the larger the duty cycle will be. The purpose of M15 is to provide bias current IB4 for integrator, which controls the frequency of square wave. The WFG provides a peak-to-peak output voltage of around 0.9 V for R=10 kΩ, R_{ref}=10 kΩ and C_L=10 pF. A nominal load capacitor (C_L) of 10 pF is used, so that the overall chip is not increased much. With these design values square waveform with duty cycle of 50% and frequency of 10 kHz is generated.

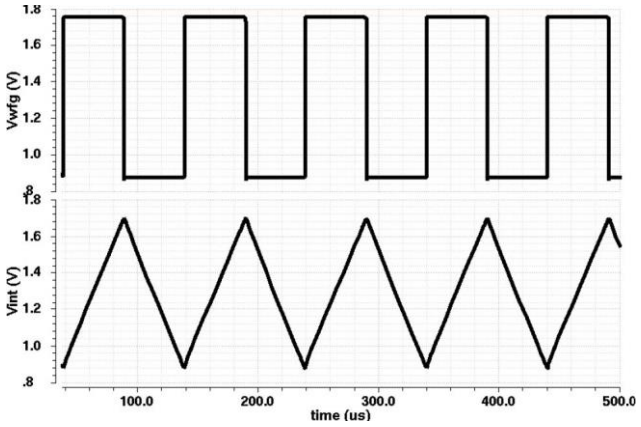

Fig. 3. Simulated square/triangular waveform output of the WFG.

A. Amplitude Control

There are two different ways to tune peak-to-peak voltage. Since V_{min} = 0.9 - IB3 * R and V_{max} = 0.9 + I * R (Assuming current I is flowing through R when output is at V_{max}). The value of current will be very high in this case. Due to which $V_{max} \approx V_{DD}$. So the peak-to-peak voltage $V_{p-p} = V_{max} - V_{min}$. So, one way to tune V_{p-p} is by varying bias current IB3 and other by changing bias resistance R. Fig. 4, Fig. 5 and Fig. 6 shows the simulated results of the measured amplitude control. The peak-to-peak (V_{p-p}) of the measured square waveform linearly varies from 0.9 V to 1.5 V (for fixed R=10 kΩ and V_tune_IB4 =0.4 V) with V_tune_IB3 variation between 0.4 V to 0.65 V. This V_tune_IB3 variation is equivalent to 2.4 uA to 83 uA variation in IB3. On the other hand, peak-to-peak (V_{p-p}) variation of 0.82 V to 0.94 V (for fixed V_tune_IB3= 0.4 V and V_tune_IB4= 0.4 V) can be achieved with R variation between 5 kΩ to 25 kΩ.

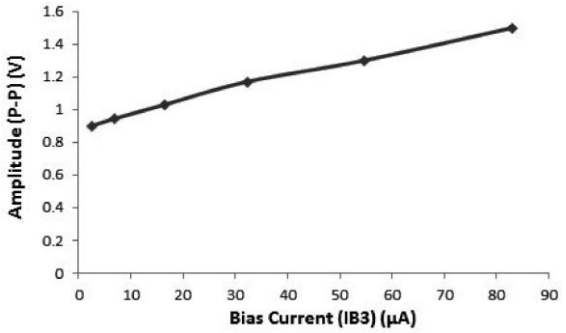

Fig. 4. Amplitude (P-P) variation with IB3.

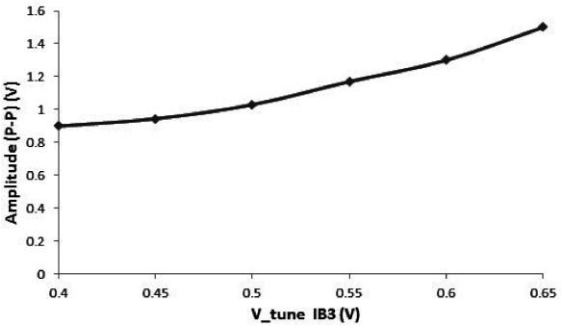

Fig. 5. Amplitude (P-P) variation with V_tune_ IB3.

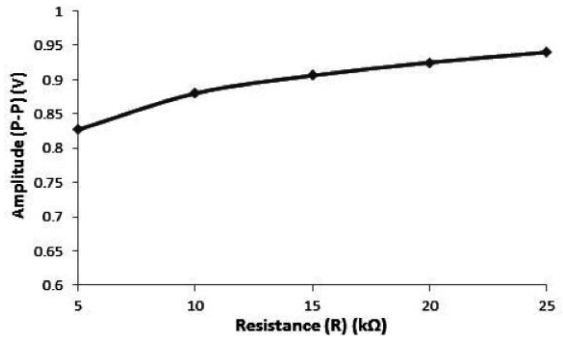

Fig. 6. Amplitude (P-P) variation with R.

B. Frequency Control

By adjusting the bias current IB4 through tuning V_tune_IB4 of M15, frequency of square waveform can be controlled like shown in Fig. 7. For this, the bias voltage (V_tune_IB3) of M14 is fixed to 0.4 V. As V_tune_IB4 is varied in the range 0.35 V to 1.6 V (for fixed R=10 kΩ and load capacitance =10 pF), tuning range of 7 kHz – 1318 kHz is obtained as shown in Fig. 8.

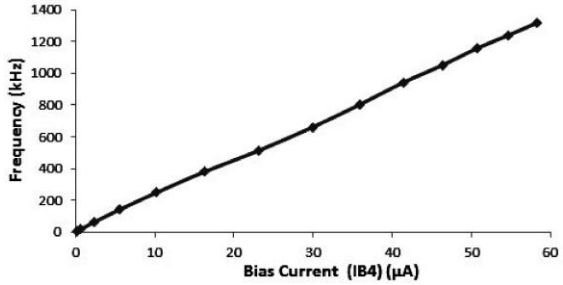

Fig. 7. Frequency variation with V_tune_IB4.

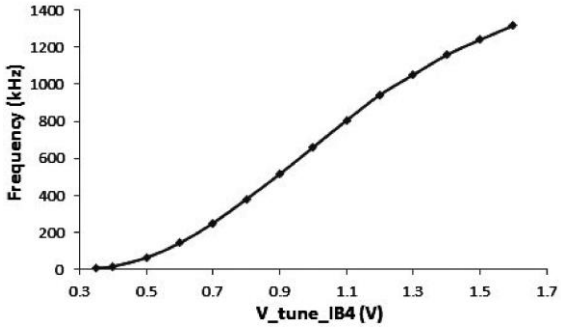

Fig. 8. Frequency variation with IB4.

Finally Table: I compare the performance with other related works. From comparison it is clear that proposed waveform generator provides ultra-wide low frequency tuning range, even wider than the others. It is also designed using a single supply. One of attractive feature of this WFG is, its frequency and amplitude can be linearly controlled by bias currents. Moreover the proposed design achieved best optimized power dissipation compare to other reported design in the Table: I.

IV. CONCLUSION

An OTA-based WFG generator has been described here, that generates low frequency square/triangular waveforms. One of attractive feature of this WFG is that its frequency and amplitude can be linearly and independently controlled by bias currents. The WFG circuit has been designed in UMC 180 nm CMOS process technology. Design parameter details and simulated results have been presented. Simulated results show almost linear behavior for both amplitude and frequency control with the bias voltages. A wide tuning range of amplitude from 0.9 V_{p-p} to 1.5 V_{p-p} and frequency from 7 kHz to 1318 kHz is achieved through adjustment of bias currents.

TABLE I

PERFORMANCE COMPARISION

Reference	[3]	[4]	[2]	This Work
Technology	180 nm CMOS	130 nm CMOS	AD844 (Discrete)	180 nm CMOS
Amplitude	0.75 Vp-p	1.5 Vp-p	1 V	0.9 Vp-p
Core Frequency	780 kHz	17 kHz	24.1 kHz	10 kHz
Type of circuit elements	4 OTA	2 OTA + 2 PMOS	2 CCII+	2 OTA + 2 PMOS
Resistors	3	2	6	2
Capacitors	20 pF	10 pF	50 pF	10 pF
Supply Voltage	1.8 V	±1 V	±15 V	1.8 V
Power Consumption	4.4 mW	457 uW	400 mW	403 uW
Tuning Range	120 - 900 kHz Single band	6.44 - 1003 kHz 0.1 Hz - 502 kHz Dual band	0.78 – 390 kHz Single band	7 – 1318 kHz Single band

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