Design and Analysis of Signal Conditioning Circuit for Capacitive Sensor Interfacing

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***Abstract*—This paper presents design and analysis of a capacitive sensor interfacing circuit, which detects the physical signal as a change in capacitance and provides voltage output. Theoretical analysis of synchronous chopper modulation and demodulation is carried out and it is shown that how this technique is utilized to remove the low frequency noise and offset voltage introduced by the operational amplifier. The signal conditioning circuit comprises of a buffer, amplifier, demodulator and low pass filter. Detailed analysis of the circuit, considering sinusoidal variation of change in capacitance is presented. Two demodulator circuit topologies are analysed and their merits and demerits are highlighted. The complete circuit is designed and simulated in UMC 180 nm CMOS process technology and the simulation results are presented.**

***Index Terms*—Capacitive sensor, Signal conditioning, Chopper modulation and demodulation.**

I. Introduction

Nowadays capacitive sensors are preferred to use in various applications like consumer electronics, biomedical systems, navigational systems, and auto mobile applications due to their higher sensitivity, independent nature with temperature and feasibility of integrating in an IC. Worldwide research is going on, in this aspect to improve the performance and accuracy of the capacitive sensor system. Multiple circuit configurations are available in literature having the goal to improve the sensitivity and resolution of the signal conditioning circuit. Techniques like chopper modulation and demodulation [1]–[7], switched-capacitor circuits along with correlated double sampling [8]–[12] and Auto-zeroing [13], [14] techniques are popularly used to remove the non-idealities of the circuit components. Switched-Capacitor circuits consist complex structures and synchronization is a main issue to consider, due to high KT/C noise [5]–[10]. Where as chopper modulation and demodulation method is simple in structure and efficient to remove the low frequency noise and offset by shifting them to higher frequencies.

In this work we have analysed the synchronous chopper modulation and demodulation in the context of capacitive sensor interfacing circuits for two different configurations and shown that, the double switch demodulator configuration effectively reduces the low frequency noise and offset better than the single switch configuration. Section II describes a general capacitive sensor system, Section III provides the detailed analysis of the two circuit configurations and Section IV presents the simulation results.

II. Capacitive Sensor System

General block diagram of an integrated capacitive sensor system is shown in Fig. 1. In this system, the capacitive sensor provides the change in capacitance due to the input sensing parameter to be measured and this change in capacitance is detected by the signal conditioning ASIC and the voltage output is provided.

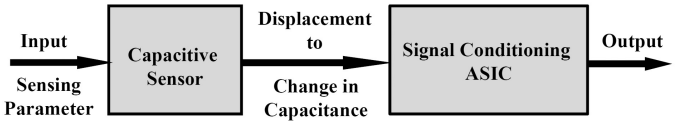

Fig. 1. Block diagram of a capacitive sensor system

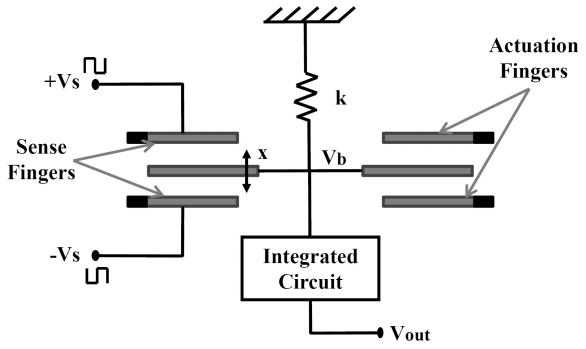

Fig. 2. General model of a capacitive accelerometer

One of the major applications which utilizes capacitive sensing principle is accelerometers. Micro-accelerometers are quite popular in recent times due to their small size, higher sensitivity and low cost for bulk requirement. A general model of a capacitive accelerometer is shown in Fig. 2. It is basically a proof-mass, spring and damper system. This configuration uses a differential capacitive sensor arrangement which increases sensitivity and reduces common-mode variations. Here, due to applied acceleration, the proof-mass is displaced, which changes the gap between the two capacitors and

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hence capacitance changes. The integrated circuit measures the change in capacitance and provides output. Sometimes, the accelerometer structure also contains actuation fingers for self test purpose.

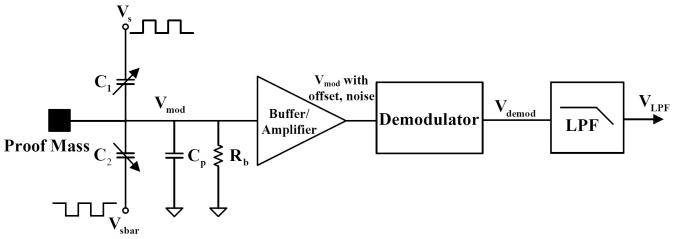

Fig. 3. Signal conditioning circuit

III. Signal Conditioning Circuit

The basic architecture of the signal conditioning circuit is shown in Fig. 3. In this configuration, the sensing capacitors in the differential sensor arrangement is excited by two out of phase square waves. This excitation square waves modulate the original signal, change in capacitance, due to input acceleration or any other input sensing parameter. This modulated signal is then buffered, amplified, demodulated and filtered to get the proper output.

A. Modulation

Differential capacitive structure, figure 3 containing two fixed plates, excited with two out of phase square signals and one movable plate, which attached with proof mass acts as modulator. The amplitude of the modulated signal is proportional to change in capacitance. Primary target to use this modulator is to shift the low frequency signal (change in capacitance) to higher frequency. The modulator output signal can be mathematically expressed as

$$V_{mod} = V_{cm} + \frac{\Delta C}{C_0}\left(V_p * \text{square}\left(2\pi \text{f}_{\text{ch}}\text{t}\right)\right) \tag{1}$$

Where V_{cm} is the common mode voltage, ΔC is the change in capacitance (DC + AC variation), C_0 is the nominal capacitance, V_p is the peak voltage of the square signal, f_{ch} is the chopper frequency.

Square wave signal is the composition of infinite odd harmonics and first two or three terms holds most of the signal characteristic. So, in this paper to analyse the system first two terms were considered. Expanding the equation 1, considering sinusoidal capacitance variation and two terms of square signal, equation 1 becomes

$$V_{mod} = V_{cm} + \frac{C\ \sin\left(2\pi f_m t\right)}{C_0}\left(1.27V_p \sin\left(2\pi f_{ch} t\right)\right. \\ \left. +0.42V_p \sin\left(6\pi f_{ch} t\right) .....\right) \tag{2}$$

Where C is the amplitude of the sinusoidal capacitance.

B. Buffer

Modulated signal containing high frequency components should be pass through a unity gain buffer, which improves the driving capability of the modulator. Designing ideal buffer with zero input offset voltage is practically impossible. Assuming finite offset voltage and finite noise, the buffered signal will be expressed as

$$V_{mod\ with\ offset,\ noise} = V_{os} + V_n + V_{cm} \\ + \frac{C\ \sin\left(2\pi f_m t\right)}{C_0}\left(1.27V_p \sin\left(2\pi f_{ch} t\right)\right. \\ \left. +0.42V_p \sin\left(6\pi f_{ch} t\right) + ...\right) \tag{3}$$

Where V_{os} is the offset voltage, V_n is the noise voltage (DC+AC).

$$V_n = V_{dcn} + V_{acn} \sin 2\pi f_n t$$

After the buffer, in general, amplifier is essential to enhance the signal amplitude but the frequency components of the signal remain same. The theoretial anaysis shown below does not include the amplification factor for simplicity.

C. Demodulation

Demodulation is the process of extracting the original signal from modulated signal. Effective design of demodulator can eliminate the additive noise and offset voltage. Two demodulation circuit configurations are proposed and analysed in this paper.

1) Demodulation with single switch: Simple switch configuration, which behaves like a pass transistor, acts as a demodulator. Unipolar square signal having chopper frequency controls the switch. It acts as a multiplier between unipolar square signal and modulated signal. It allows the signal when the switch is in ON state and provides 0 V when the switch is in OFF state. This demodulator is sensitive to the noise and offset voltage, so it fails to remove the noise and offset voltage. Mathematically single switch demodulator output is expressed as

$$V_{ss\ demod} = V_{mod\ with\ offset,\ noise} * Clk \tag{4}$$

Where Clk is the square signal, expressed as.

$$Clk = 0.5 + 0.5\,\text{square}(2\pi \text{f}_{\text{ch}}\text{t}) \tag{5}$$

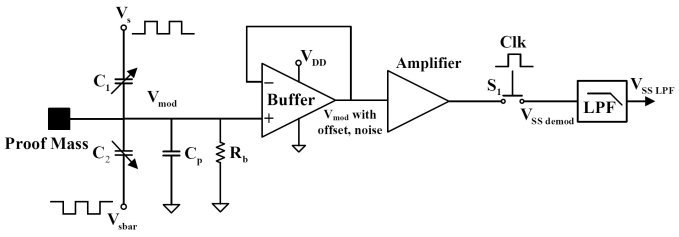

Fig. 4. Interfacing circuit with single switch demodulator

From equation 3 and 5, equation 4 can be written as

$$\begin{aligned} V_{ss\,demod} &= 0.5V_{cm} + 0.5V_{os} + 0.5V_{dcn} \\ &+0.635V_{cm}\sin(2\pi f_{ch}t) + 0.635V_{os}\sin(2\pi f_{ch}t) \\ &+0.635V_{dcn}\sin(2\pi f_{ch}t) + 0.5V_{acn}\sin(2\pi f_n t) \\ &+0.3175V_{acn}\cos(2\pi(f_{ch}-f_n)t) \\ &-0.3175V_{acn}\cos(2\pi(f_{ch}+f_n)t) \\ &+0.3175\frac{CV_p}{C_0}\cos(2\pi(f_{ch}-f_m)t) \\ &-0.3175\frac{CV_p}{C_0}\cos(2\pi(f_{ch}+f_m)t) \\ &+1.27A\ \sin(2\pi f_m t) + 0.42B\sin(2\pi f_m t) \\ &+..... \end{aligned} \tag{6}$$

Where $A = \frac{1.27}{4}\frac{CV_p}{C_0}$ and $B = \frac{0.42}{4}\frac{CV_p}{C_0}$.
Equation 6 represents the presence of various frequency components at the output of single switch demodulator.

2) Demodulation with double switch: Figure 5 shows the double switch demodulator circuit, where two switches and a 180° phase shifter with respect to V_{cm} is used. Clk signal controls the switch S_1 and anti-phase Clk signal controls the switch S_2. Output of the circuit is expressed as

$$\begin{aligned} V_{ds\,demod} = &(V_{mod\ with\ offset,\ noise} * Clk) \\ &+ \\ &\left(\overline{V_{mod\ with\ offset,\ noise}} * \overline{Clk}\right) \end{aligned} \tag{7}$$

Where $\overline{V_{mod\ with\ offset,\ noise}}$ is the anti-phase $V_{mod\ with\ offset,\ noise}$ signal, $\overline{Clk}$ is the anti-phase Clk signal, expressed as.

$$\begin{aligned} \overline{V_{mod\ with\ offset,\ noise}} = V_{cm} - V_{os} - V_n - \\ \frac{C\ \sin(2\pi f_m t)}{C_0} V_p\,\mathrm{square}\,(2\pi \mathrm{f_{ch}} \mathrm{t}) \end{aligned} \tag{8}$$

and

$$\overline{clk} = 0.5 - 0.5\,\mathrm{square}(2\pi \mathrm{f_{ch}} \mathrm{t}) \tag{9}$$

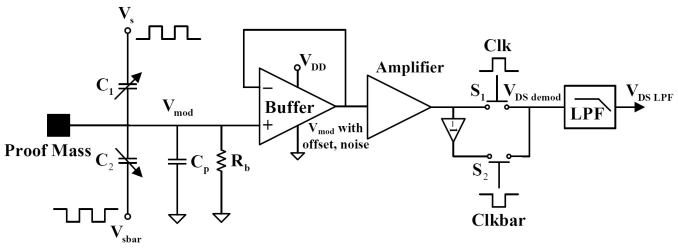

Fig. 5. Interfacing circuit with double switch demodulator

From equation 7, 8 and 9, the double switch demodulator output can be written as

$$\begin{aligned} V_{ds\,demod} &= V_{cm} + 1.27V_{os}\sin(2\pi f_{ch}t) \\ &+1.27V_{dcn}\ \sin(2\pi f_{ch}t) \\ &+0.635V_{acn}\cos(2\pi(f_{ch}-f_n)t) \\ &-0.635V_{acn}\cos(2\pi(f_{ch}+f_n)t) \\ &+0.635A(-\sin(2\pi(-f_m)t)) \\ &+0.21A(-\sin(2\pi(-2f_{ch}-f_m)t)) \\ &-0.635A(\sin(2\pi(2f_{ch}+f_m)t) - \sin(2\pi(f_m)t)) \\ &-0.21A(-\sin(2\pi(-2f_{ch}+f_m)t)) \\ &+0.635B(-\sin(2\pi(2f_{ch}-f_m)t)) \\ &+0.21B(-\sin(2\pi(-f_m)t)) \\ &-0.635B(-\sin(2\pi(2f_{ch}+f_m)t)) \\ &-0.21B(-\sin(2\pi f_m t)) + ... \end{aligned} \tag{10}$$

Where $A = \frac{1.27}{2}\frac{CV_p}{C_0}$ and $B = \frac{0.42}{2}\frac{CV_p}{C_0}$
Equation 10 represents the presence of various frequency components at the output of double switch demodulator.

D. Low Pass Filter

Demodulated signal having higher frequency components has to pass through a low pass filter, to attenuate the high frequency components. Equation 11 is the low pass filtered signal expression for the case single switch demodulator, which indicates the presence of offset and noise voltage.

$$\begin{aligned} V_{ss\,LPF} &= 0.5V_{cm} + 0.5V_{os} + 0.5V_{dcn} \\ &+0.5V_{acn}\sin 2\pi f_n t + 0.5\frac{CV_p}{C_0}\sin 2\pi f_m t \end{aligned} \tag{11}$$

Equation 12 is the low pass filtered signal expression for the case double switch demodulator, which indicates the absence of offset and noise voltage.

$$V_{ds\,LPF} = V_{cm} + \frac{CV_p}{C_0}\sin 2\pi f_m t \tag{12}$$

Mathematical analysis is showing that the signal conditioning circuit with single switch demodulator is capable to remove 50 % of the offset and low frequency noise, where as double switch demodulator is capable to remove 100 % of the offset and low frequency noise.

IV. Simulation Results

The signal conditioning circuit is designed in cadence virtuoso platform with UMC 180 nm process technology. Signals at various stages of the signal conditioning circuits are shown in figure 6 to figure 12.

Modulated signal represented by equation 2, considering $V_{cm} = 0.9\,V$, $V_p = 0.9\,V$, $\Delta C = 0.1\sin(2\pi f_m t)\ pF$, $C_0 = 5\,pF$, $f_{ch} = 100\,kHz$, $f_m = 10\,Hz$ is shown in figure 6

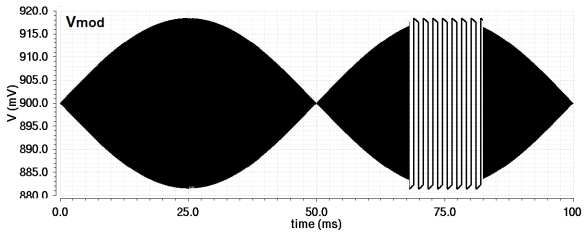

Fig. 6. Modulated signal without offset and noise

Buffer stage, which is next to the differential capacitive structure consist operational amplifier, which offers offset and noise to the modulated signal. The buffered signal represented in equation 3 is shown in figure 7.

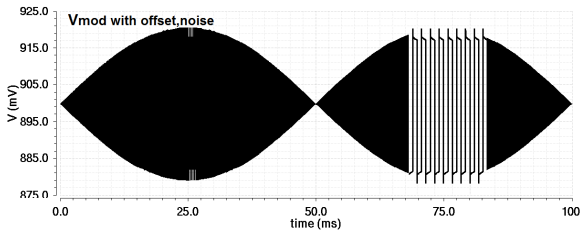

Fig. 7. Modulated signal with offset and noise

Amplified signal with gain of 10 is shown in figure 8.

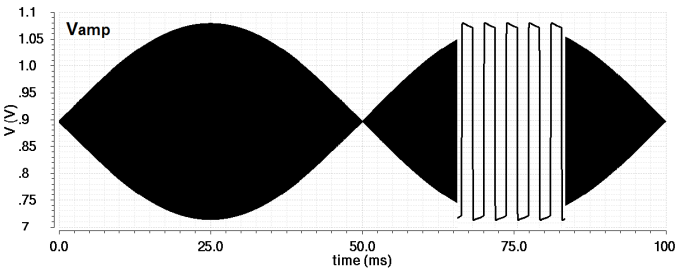

Fig. 8. Amplified buffered signal

A. Single switch demodulation

Demodulated signal with single switch demodulator expressed in equation 6 is shown in figure 9.

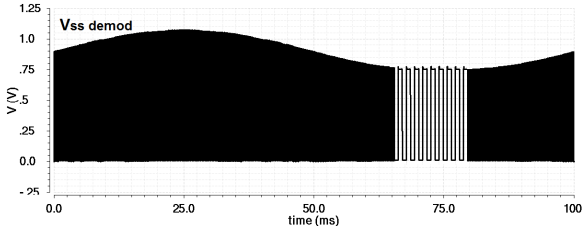

Fig. 9. Single switch demodulated signal

Filtered signal with single switch demodulator, expressed in equation 11 is shown in figure 10.

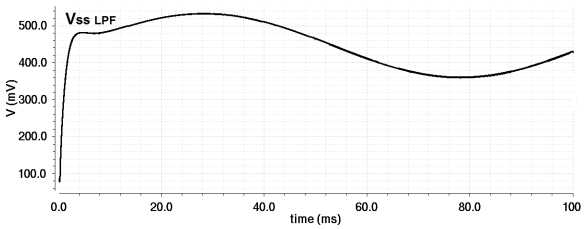

Fig. 10. Single switch demodulator filtered signal

B. Double switch demodulation

Demodulated signal with double switch demodulator, expressed in equation 10 is shown in figure 11.

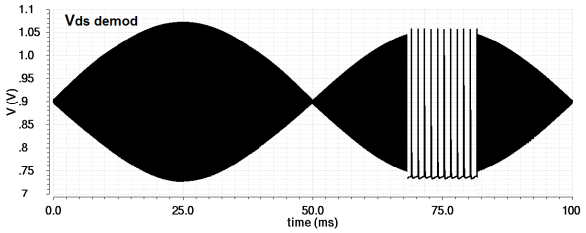

Fig. 11. Double switch demodulated signal

Filtered signal with double switch demodulator, expressed in equation 12 is shown in figure 12.

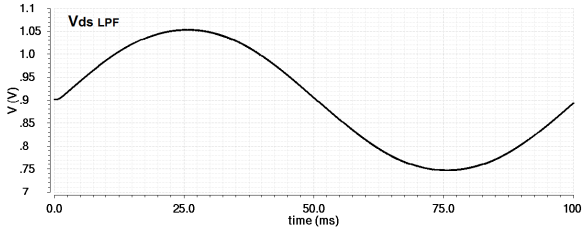

Fig. 12. Double switch demodulator filtered signal

As a result figure 10 indicates the presence of offset and noise, where as figure 12 indicates the absence of offset and noise.

V. Conclusion

Signal conditioning circuit for capacitive sensor is designed, analysed mathematically, and implemented using UMC 180 nm process technology. Two circuit topologies with single switch demodulator and double switch demodulator is studied. Single switch demodulator, which is having simple structure is removing $50\,\%$ of the offset and noise. Whereas double switch demodulator, perfectly removing the offset and low frequency noise. The presented demodulator topologies are having simple structure with compare to existing circuits, and occupies less chip area.

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