Category (Thin Films)

Study of Leakage Current and Interface of ZrO_2 gate oxide on Silicon

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Abstract

Now-a-days scaling of gate oxide thickness has led to a large enhancement in the leakage current, so high-k gate dielectrics has been focused to overcome the physical roadblock of SiO_2 thickness. A Zirconium oxide (ZrO_2) thin film was prepared using sol-gel method and deposited on n-Si substrate using spin coating method followed by annealing at 500 °C and 700 °C for 1 hour respectively. In order to provide electrical contacts to the metal oxide semiconductor (MOS) capacitor, aluminium was deposited on both sides of the sample. The structural characteristics of the MOS capacitor were studied from X-Ray Diffraction pattern. The leakage current density was found to be 10^{-4} A/cm^2 at -0.5V with ZrO_2 annealed at 700 °C. Moreover, the capacitance voltage (C-V) measurements were taken in order to study the interface properties. The calculated interface trap density (D_{it}) is found to be 13.6 x 10^{11} cm^{-2}eV^{-1} for ZrO_2/Si interface at 700 °C.

In semiconductor industry, the continued device scaling required to follow the International Technology Roadmap of Semiconductors (ITRS). One of the way to achieve it, by the continuous reduction of gate oxide (SiO_2) thickness which leads to exponential rise in leakage current through the gate oxide. According to ITRS, SiO_2 needs to be replaced with high-K dielectrics for the 65nm technology, so that the equivalent oxide thickness can go as low as 2nm [1]. The reported leakage current increases by 8 orders of magnitude for a thickness change by factor of 2 at a given gate bias [2]. Among many possible high-K gate dielectrics, Zirconium based oxides are the promising candidates due to its good thermal stability [3], large band-offset with Si-substrate [4], high dielectric constant and band gap [5]. However, ZrO_2 forms defects at the interface of oxide and Si-substrate during the high temperature post deposition annealing processes that results in the formation of interface charges.

Numerous methods like sputtering, atomic layer chemical vapor deposition have been used to deposit ZrO_2 films [6]. Among these, spin coating has been preferred presently, as it is fast, easy and cost effective method. Furthermore, the deposited thin film is homogeneous films. Moreover, sol-gel method is simple, size tailoring and feasible method of preparing thin films [7].

In this work, the effect of post deposition thermal treatment on the structural and electrical properties of ZrO_2 gate dielectric thin films deposited on n-type silicon (Si) substrate have been studied.

Zirconium oxychloride ($ZrOCl_2.8H_20$) was used as the precursor for the synthesis of ZrO_2 thin films. 0.1M $ZrOCl_2.8H_20$ was dissolved in 50ml ethanol with vigorous stirring. The solution was spin coated at 4000 rpm for 30 sec on a cleaned n-type Si (100) substrate (ρ=1-20 Ω cm). Then samples were heated at 70 °C for 5 minutes to evaporate the solvent. Multiple coatings were deposited in order to achieve an optimised thickness. An aluminum film was deposited on both side of silicon by thermal evaporation process to realise a MOS structure. The current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed using Keithley 6487 picoammeter/ voltage source and Agilent E4980A precision LCR meter respectively.

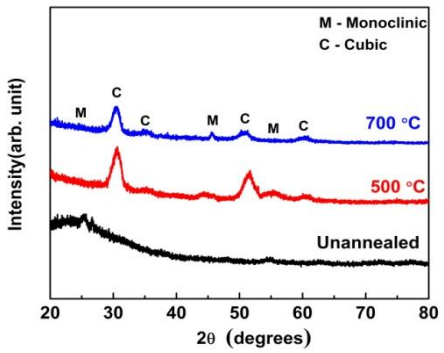

Figure 1. XRD pattern of ZrO_2 thin films at different annealing temperature.

Figure 1 depicts the XRD pattern of ZrO_2 thin film deposited on Si. The unannealed thin film shows a broad amorphous peak around 24°

indicating the monoclinic structure. However the annealed samples show distinct crystalline peaks of ZrO_2 monoclinic and cubic phases. These phases are difficult to distinguish only by examining the XRD patterns as the annealed samples have similar lattice parameter and peak broadening. The high intense crystalline peaks (111) at 30.53°and (220) at 50.66° corresponds to the cubic phase of ZrO_2.

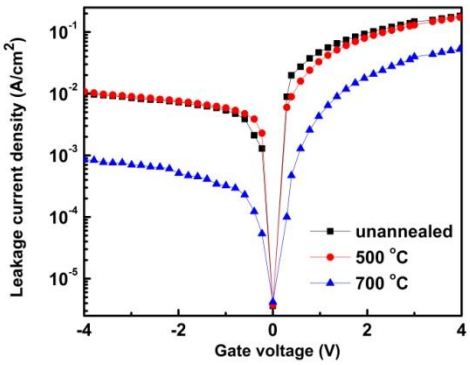

Figure 2. Comparison of leakage current density with annealing temperature of Al/ZrO_2/n-Si MOS structure.

The leakage current behaviour due to the post annealing temperature is demonstrated by I-V measurements. The I-V characteristics of ZrO_2 thin films at different annealing temperatures are shown in figure 2. The leakage current density of ZrO_2 at -0.5 V is 2.2 x 10^{-4} A/cm^2 for 700 °C annealing, 2.1 x 10^{-3} A/cm^2 for 500 °C annealing. It is observed that the leakage current through the gate dielectric decreases by an order with the increase in the post deposition anneal temperature as the electrons get energized thermally and fill up the interface oxide traps thereby leading to the reduction in the flow of leakage current.

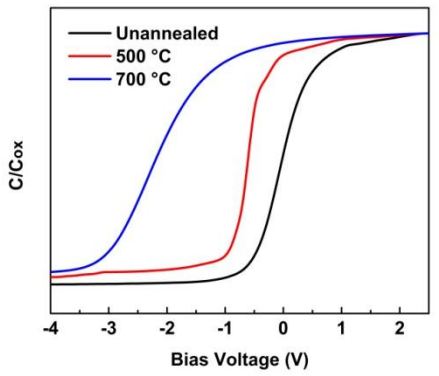

Figure 3. Comparison of Capacitance-Voltage (CV) curve with annealing temperature of Al/ZrO_2/n-Si MOS structure.

The oxide-semiconductor interface properties were extracted from the C-V and conductance-voltage (G-V) measurements. With the increase in anneal temperature there is an increase in negative flat-band voltage shift as shown in figure 3. The large negative shift indicates the presence of fixed positive oxide charges. Moreover, there are fewer oxygen atoms, those might have accepted electrons from Zr atoms [8]. Moreover, the charge transfer from oxygen to gate electrode is easy with high work function metal, leads to the presence of dipole layer near the gate-oxide interface which results in the flat-band voltage shift [9]. The fixed oxide charges calculated increases from 5.13 x 10^{12} cm^{-2} to 5.8 x 10^{12} cm^{-2} with the increase in anneal temperature from 500 °C to 700 °C. The increase in the slope of the depletion region indicates the increase in the interface trap density (D_{it}) with the annealing temperature. The value of D_{it} was calculated from C-V and G-V measurements taken at 1MHz. D_{it} increases from 1.2 x 10^{11} cm^{-2}eV^{-1} for unannealed sample to 13.6 x 10^{11} cm^{-2}eV^{-1} for 700 °C annealing, which is close to that of state of art high-k materials [10].

The XRD pattern of annealed ZrO_2 thin film show distinct crystalline peaks of ZrO_2 monoclinic and cubic phases. The reduction of leakge current from 2.1 x 10^{-3} A/cm^2 to 2.2 x 10^{-4} A/cm^2 with the increase in annealing temperature from 500 °C to 700 °C is observed. Moreover, the fixed oxide charges calculated increases from 5.13 x 10^{12} cm^{-2} to 5.8 x 10^{12} cm^{-2} with the increase in anneal temperature from 500 °C to 700 °C. D_{it} increases from 1.2 x 10^{11} cm^{-2}eV^{-1} for unannealed sample to 13.6 x 10^{11} cm^{-2}eV^{-1} for 700 °C annealing, thereby indicating a good interface of ZrO_2 and Silicon.

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