A Circuit Technique for Leakage Power reduction in CMOS VLSI Circuits

Venkata Ramakrishna Nandyala* and Kamala Kanta Mahapatra
Electronics & Communication Engineering Department
National Institute of Technology, Rourkela
Rourkela-769008, Odisha, India
*e-mail: 512ec107@nitrkl.ac.in

***Abstract*— Scaling of CMOS technology improved the speed nevertheless the leakage currents are leftover as an adverse effect. The problem has taken a serious turn as the scaling extends into ultra-deep-submicron (UDSM) region. These unsolicited leakage currents should be minimized for the smooth functioning of the circuit. Designing of such leakage free nanoscale CMOS circuits turns to be a challenging task. In this work, we address the issue of leakage power that arises with the device channel length scaling to sub-100nm. We present a circuit technique to mitigate the leakage currents of MOSFET through controlling the voltage at the source terminal of the MOSFET. CMOS inverter designed using the proposed technique results in 98% and 30% improvement in static and total power dissipation respectively compared with its conventional design. The simulation results of NAND and NOR gates designed using the same technique indicates 15.89% and 18.83% improvement in the total power compared with their corresponding conventional designs. 11-stage CMOS ring oscillator designed using the proposed technique is analyzed, and corresponding simulation results are reported. Comparison of the proposed circuits in terms of power dissipation and delay with two existing techniques is presented. The circuits designed using the proposed technique results in good Power-Delay Product (PDP).**

Keywords—CMOS; UDSM; leakage power; CMOS inverter; low power dissipation.

I. INTRODUCTION

With the rapid technological growth in the semiconductor industry, the high computational and even complex applications are being implemented in a small size VLSI chip with the use of Complementary Metal Oxide Semiconductor (CMOS) technology. Fortunately, the growth in the semiconductor technology is capable of providing required feature size. With the utilization of each new technology node, the speed of the Integrated Circuit (IC) has increased by 30% roughly [1]. The Requirement of high density chips and high speed systems made MOS devices to scale to smaller dimensions that increased the current drive (g_m) capability. These smaller transistors and shorter interconnects results in less capacitance and altogether increased the speed of the integrated circuit [1]. Nonetheless, the extent of scaling is constrained by physical limitations such as short-channel effects. The main consequences are the leakage currents contributing to massive static power dissipation. The leakage current increases with the scaling of device channel length. With the overall effect, power dissipation has become the critical issue in the design of microelectronic circuits. Enormous efforts have been paid [2][3][4] and need to do more to mitigate these leakage currents. Few of the efforts for reducing leakage currents include techniques, MTCMOS Power Gating, Super Cutoff CMOS Circuit, Forced Transistor Stacking and Sleepy Stack. Multi threshold CMOS (MTCMOS) inserts extra transistor(s) either PMOS/NOMS or both called sleep transistor(s) into the design. During the normal mode of operation, these transistors set to "*on"* state without disturbing the functionality of the circuit. During the standby mode, these transistors switched to "*off"* state to isolate the power supply from the circuit. The isolated supply voltage causes the leakage currents to minimize [2]. Nevertheless, this technique increases the dynamic power dissipation of the circuit. Super Cutoff CMOS, an alternate to MTCMOS uses low threshold voltage sleep transistors instead of high threshold voltage transistors. It turns off sleep transistors with a small negative voltage to reduce the subthreshold leakage current leaving a difficulty of designing of the controller circuit to generate negative gate voltage for the sleep transistors [2].

Stacking is another technique that uses series connected transistors to reduce subthreshold leakage currents. If the natural stacking of transistors does not exist in the circuit, then one can achieve stacking effect by replacing a single transistor with two transistors in the design called forced stacking [2]. This technique works efficiently when more than one transistor in the stack of series connected transistors are in "*off"* state [3]. Due to extra transistors, this technique results in delay penalty. Sleepy stack is another method that can reduce this delay by adding additional transistor in parallel to the additional stack transistor. However, sleepy stack approach results in higher dynamic power consumption, and it needs an extra complex sleep signal circuitry [2]. LECTOR [5] is a circuit technique for achieving low power dissipation. It inserts two extra transistors in the circuit for achieving low leakage design. Complex circuit techniques have to be developed to get power savings as technology scaling itself doesn't provide enough savings [6].

In this paper, we present a circuit technique to mitigate the leakage currents of sub 100-nm CMOS VLSI circuits by using two extra transistors.

The rest of the paper is organized as follows. Section II describes leakage power dissipation in CMOS VLSI circuits and its importance. Section III describes our proposed technique. Section IV describes the results followed by the conclusion in Section V.

II. Leakage Power Dissipation

Leakage or static power dissipation occurs due to the presence of various leakage currents such as subthreshold leakage, reverse-bias source/drain junction leakages, gate oxide tunneling leakage, Gate Induced Drain Leakage (GIDL) [3][4]. Subthreshold leakage current is the dominant leakage current in sub-100nm circuits [2]. Even when the gate voltage is less than the threshold voltage of the device, the current flows between the drain and source due to the diffusion of minority carriers. The subthreshold leakage current, I_{sub} can be expressed as [7]

$$I_{sub} = I_{D0} \times e^{\frac{V_G}{mV_T}} \times (e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}}) \qquad (1)$$

Subthreshold leakage current is due to the diffusion of minority carriers in the channel of MOS transistor [4]. This current depends on temperature, size of the device, supply voltage and process parameters [4]. For the desired speed of operation, the supply voltage and threshold voltage should be minimized as the CMOS technology subjected to scales down. However, subthreshold current increases exponentially with the decrease in the threshold voltage.

The power dissipation of Intel process technologies are shown in Fig. 1 [8]. In 1µm technology the leakage power is only about 0.01% of the active power. But as the technology scales down to 100 nm, the leakage power contribution raised and became 10 % of the active power dissipation. It means that leakage currents are increasing with the scaling of channel length. This has motivated many researchers to work on it, and many innovations have been proposed to circumvent the leakage power problem.

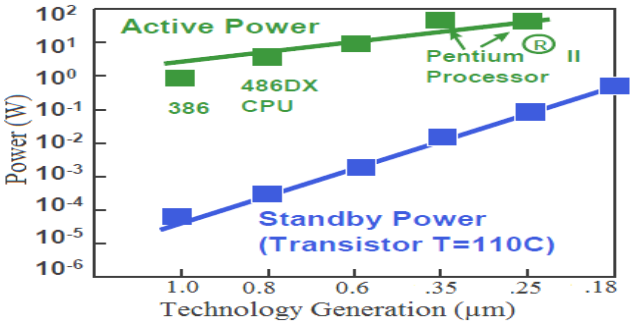

Fig. 1. Power consumption of Intel technologies [8].

III. Proposed Technique

The basic idea behind our proposed approach is to raise the voltage at the source terminal of the MOS transistor to reduce the leakage currents so as to minimize the static power dissipation. It is known that the subthreshold current increases exponentially with the decrease in the threshold voltage. And it is observed that the threshold voltage of a short channel MOSFET reduces with increase in the drain to source voltage (V_{DS}) [3]. It implies more subthreshold current occurs at higher drain to source voltage. With reference to the subthreshold current equation (1), the subthreshold current can be minimized significantly by decreasing drain to source voltage (V_{DS}). Considering these two facts, subthreshold current can be minimized by reducing the drain to source voltage. Drain to source voltage can be reduced by raising the voltage at the source terminal of the MOSFET [9] called source biasing. For better understanding of the approach, we consider CMOS inverter circuit. The corresponding circuit designed using the proposed approach is shown in Fig. 2 along with the conventional circuit.

Here, we have used two extra transistors labeled PM2 (PMOS) and NM2 (NMOS) for the purpose of raising the voltage at the source terminal of the MOSFET. Transistor PM2 is configured to work in "*cut off*" mode (source and gate connected) while the transistor NM2 follows the circuit input conditions. The transistor PM2 is connected between the output node of the circuit and the source terminal of the transistor NM1. The purpose of the transistor PM2 is to supply the leakage currents to the source terminal of the upper NMOS transistor (NM1) to charge the node (source terminal of NM1). During the logic '0' condition at the input, the two NMOS transistors NM1 and NM2 turned *off* and a logic '1' appears at the output node. As the extra PMOS transistor PM2 set to "*cut off*" state, it supplies leakage currents and establishes a certain voltage at the source terminal of the upper NMOS transistor NM2 depending on the amount of leakage current provided by the transistor PM2.

The increased source voltage (V_S) of the upper NMOS transistor (NM1) reduces the drain-to-source voltage (V_{DS}) of the transistor NM1 and then the subthreshold leakage current. The dependency of node voltage on the width of PMOS transistor PM2 is depicted in Fig. 3.

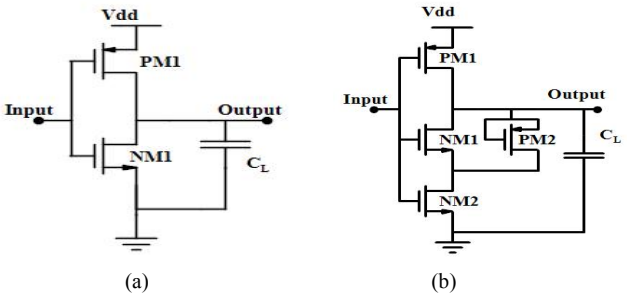

Fig. 2. Circuit schematic of CMOS inverter designed using: (a) Conventional technique, (b) proposed technique.

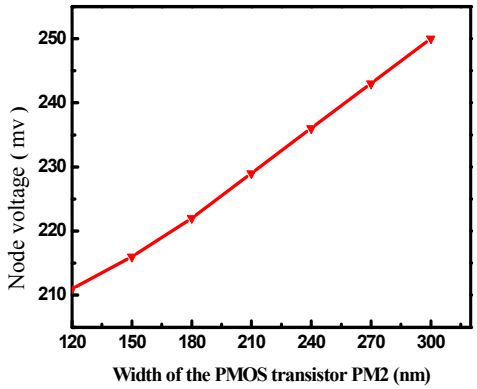

Fig. 3. Dependency of node voltage (source terminal of NM1) on the width of the transistor PM2.

The source voltage of the transistor NM2 increases with the width of PM2 as the amount of leakage in PM2 increases with its width. Exclusive charging of source terminal of the lower NMOS transistor (NM1) in the proposed inverter circuit keeps V_{GS} more negative. Voltage transfer characteristic (VTC) for proposed CMOS inverter circuit along with conventional circuits are shown in Fig. 4. The proposed CMOS inverter circuit exhibits good characteristic curve than the circuit designed using LECTOR technique, and it is comparable to the conventional circuit. We have designed NAND and NOR gates using the proposed approach. Using the proposed CMOS inverter, we have designed an 11-stage CMOS ring oscillator. Fig. 5 shows the circuit schematic of NAND gates designed using conventional, LECTOR and proposed techniques. It also shows the schematic of CMOS inverter designed using LECTOR technique. We have discussed the results of all these circuits in the following section.

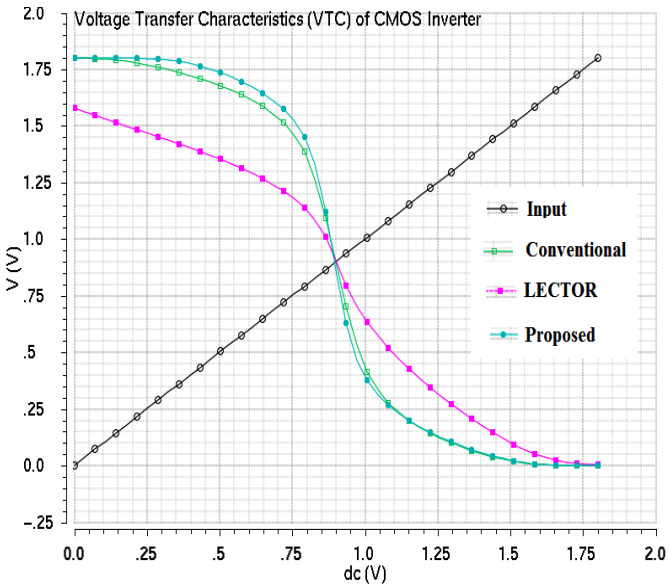

Fig. 4. Voltage Transfer characteristc (VTC) of CMOS Inverter circuit.

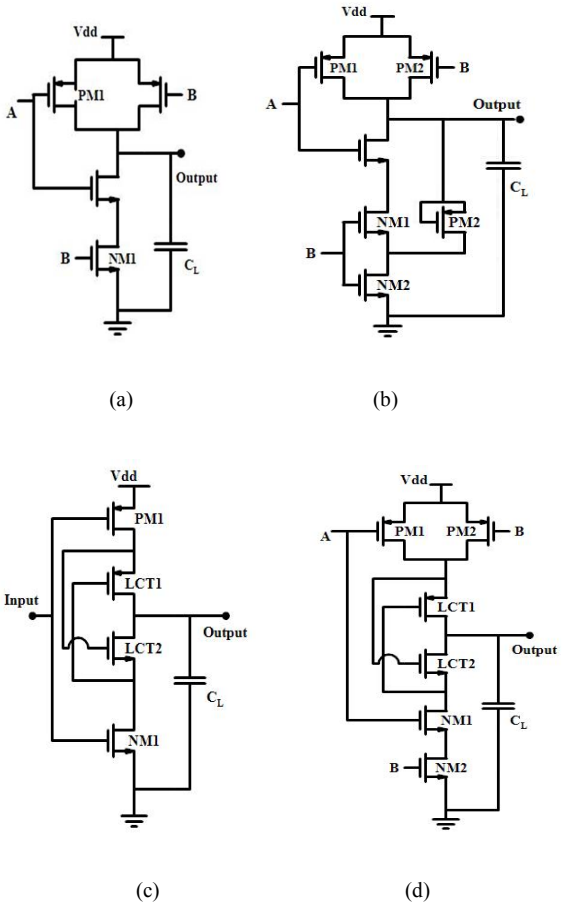

Fig. 5. Circuit schematic of: (a) conventional NAND gate, (b) proposed NAND gate, (c) LECTOR[5] CMOS inverter, (d)LECTOR [5] NAND gate.

IV. Results And Discussions

In this section, we have made an elaborate discussion on the simulation results of the proposed and conventional designs obtained using 90nm technology file. Simulations are carried out in Cadence Spectre simulation tool. Fig. 6 shows the output waveforms of CMOS inverter circuits designed using conventional, LECTOR [5] and proposed techniques. It is well observed that our proposed circuit results in full swing output voltage similar to the case of conventional circuit. But the output of the circuit designed using the LECTOR technique [5] does not reach to full swing voltage. The reason could be as at least one among two extra transistors inserted for leakage control set to be "*cut off*" state at any time, the output voltage may not get full swing. Among two additional transistors, one is inserted in pull-up path and the other is in the pull-down path. In the case of the proposed design, the working mode of the extra transistor (NM2) inserted in the pull down path is similar to the transistor NM1. There is no additional transistor inserted in the pull up path of the proposed circuit. So the circuit can attain full value (logic "1") at the output.

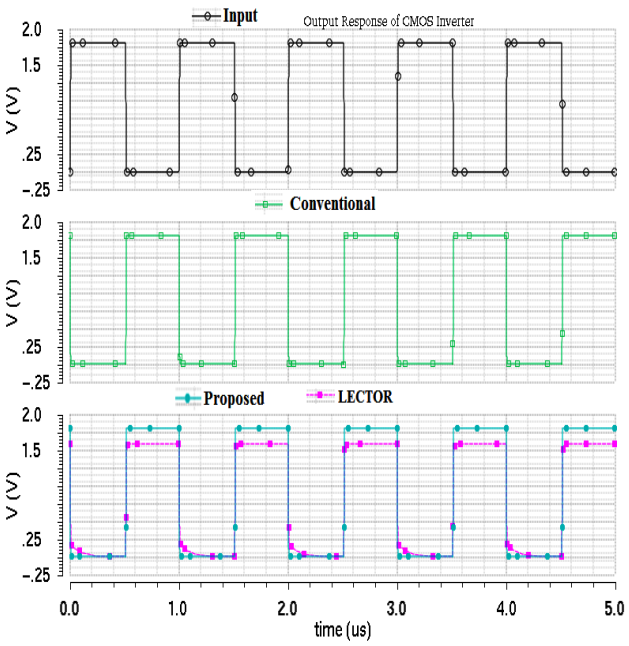

Fig. 6. Output waveforms of CMOS inverter circuit.

Table I shows the static power consumption of the CMOS inverter circuit. Proposed CMOS inverter circuit dissipates less power compared to the other two circuits. The total power dissipated by CMOS inverter, 2- input NAND and NOR gates and 11-stage ring oscillator circuits is presented in Table II. For a considered simulation setup, all the circuits dissipated less power compared to conventional circuits. CMOS inverter and 11-stag ring oscillator designed using proposed approach dissipate less power compared to the corresponding circuits designed using LECTOR technique. Static power consumed by NAND and NOR gates designed using conventional, LECTOR and proposed circuit techniques is summarized in Table III. We have listed the leakage power dissipated during each possible input vector. In the table, 'A' and 'B' represents the inputs to the gate.

Power-Delay-Product (PDP) is the important parameter to assess the quality and performance of logic circuits. It represents the energy consumed for switching event. It is preferred to have the least value of PDP for the logic circuits. We measured PDP for the all three designs (conventional, LECTOR and proposed) and summarized in Table IV. CMOS inverter circuit along with the two logic gates NAND and NOR designed with proposed technique results in less PDP compared with the conventional design. Proposed CMOS inverter exhibits less PDP compared to the CMOS inverter circuit designed through LECTOR approach. PDP plays a significant role in low power designs [10]. On overall comparison, our proposed technique results in full swing operation along with good PDP. All the results of the proposed circuits are obtained by choosing the width of the extra PMOS transistor PM2 equal to 120nm. Extra PMOS transistor PM2 is the transistor connected between the output and the node.

TABLE I. STATIC POWER DISSIPATION OF CMOS INVERTER

Circuit/ Design	Conventional (w)	LECTOR (w)	Proposed (w)	% Improvement comparison with	
				Conventional	LECTOR
CMOS Inverter	489.2 e^{-9}	253.9 e^{-9}	8.9 e^{-9}	98.2 e^{-9}	96.5 e^{-9}

TABLE II. TOTAL POWER DISSIPATION

Circuit/Technique	Conventional (µw)	LECTOR (µw)	Proposed (µw)	Improvement (%) Comparison with	
				conventional	LECTOR
Inverter	1.35	0.96	0.94	30.7	2.81
NAND	0.89	0.66	0.75	15.9	-13.1
NOR	1.13	0.76	0.92	18.8	-20.3
11-stage RO	296.67	318.9	285.1	3.9	10.6

TABLE III. STATIC POWER DISSIPATION OF NAND AND NOR GATES

Input vector		Conventional (nw)		LECTOR (nw)		Proposed (nw)	
A	B	NAND	NOR	NAND	NOR	NAND	NOR
0	0	9.67	1008	9.53	508.47	9.69	528.89
0	1	569.6	47.5	285.69	35.82	572.77	47.49
1	0	336.3	16.12	278.21	14.31	7.97	16.12
1	1	9.96	0.07	6.08	0.07	9.96	0.07

TABLE IV. POWER-DELAY PRODUCT(PDP)

Design	Conventional (J)	LECTOR (J)	Proposed (J)
Inverter	854.66 e^{-18}	707.31 e^{-18}	621.73 e^{-18}
NAND	537.84 e^{-18}	451.76 e^{-18}	447.97 e^{-18}
NOR	457.32 e^{-18}	358.48 e^{-18}	377.21 e^{-18}

V. CONCLUSION

In this paper, a low leakage power circuit technique that controls the source voltage of the MOSFET through the leakage currents of another MOSFET is presented. Maximum improvement in the power dissipation depends upon the amount of leakage currents that are supplied to the source terminal of the subjected MOSFET. CMOS inverter circuit designed using the proposed technique results in full swing operation along with better power improvement. 11-stage ring oscillator designed using proposed technique attained 3.9 % and 10 % improvement in the total power consumption compared with the conventional and LECTOR techniques respectively. Power-delay product of the proposed circuits improved well compared with conventional designs. The

proposed CMOS inverter can be used in the design of inverter based designs like SRAM, CMOS ring oscillator for low power operation.

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