Power Efficient Design of a Novel SRAM Cell with Higher Write Ability

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Abstract— **The modern high-performance portable communication devices are the key to make the world more inclusive than before. There is a great demand for high-performance SOC inside the high-performance portable devices. According to ITRS and current research, on chip memory technology plays a great role in the SOC performance. Hence enhancing on-chip memory performance will lead to performance enhancement of the device. A novel SRAM cell is designed which reduces the total power consumption by 15.33%. It also increases the write-ability by 63.61% with respect to the conventional 6T-SRAM cell. It blocks the short-circuit current during state transition to reduce the dynamic power consumption. During a write operation, it initiates the feedback loop process for data latching, earlier than the 6T-SRAM cell which increases the write-ability of the proposed cell by a large amount. A thorough analysis about power consumption, write-ability and physical layout design of the proposed cell array is carried out and compared with that of a conventional 6T-SRAM cell array.**

***Index Terms*— Short-circuit current, Low power, Dynamic power, N-Curve, SVNM, SINM, SPNM, WTV, WTI, WTP**

I. Introduction

The adoption of moor's law by the semiconductor industry has become a boon to the SOC designer as more the device size shrinks more will be the integration and more will be the functionality that can be embedded into the SOC [1]. As per recent studies memory block plays an important role in the SOC design as it occupy a large portion inside the SOC. So the performance of the memory block has to be enhanced at par with that of the rest part of SOC. Power consumption, data integrity and area consumption are the mostly focused performance indices of the SOC which are contradictory to each other unfortunately.

As SRAM cell is designed with minimum possible feature size further scaling of it escalates its issue of conflicting behavior between read stability and write-ability. Hence during SRAM cell design maintaining data stability, write-ability along with power reduction is of high importance.

A seven transistor based SRAM cell, the current-controlled SRAM cell (CC-SRAM) is designed and presented in this paper which reduces the total power consumption in comparison to the conventional 6T-SRAM cell as well as increases the write-ability of the cell.

The rest of the paper is described as mentioned. The proposed SRAM cell is described in section II. The comparative performance analysis is carried out in section III. The physical layout design is described in section IV. Finally section V represents the conclusion of the work.

II. The Proposed SRAM Cell

The proposed CC-SRAM cell is shown in Fig. 1. It consists of NM1-PM1 and NM2-PM2 transistors which forms the basic cross coupled inverter pair. NM3 and NM4 are two access transistors connected to the inverter pair for data extraction to the bit lines. NM5 is connected to the source of NM1 and NM2 and its gate is supplied with a controlled gate voltage to restrict the current flow through it.

The proposed cell has two advantages over the conventional 6T-SRAM cell.

- Enhancement of write-ability
- Reduction of power consumption.

A. Write Ability Enhancement of CC-SRAM Cell

The write operation is apparently a two-step process.

Step 1: First one of the bit lines is dragged to '0' from its initial pre-charged value by the write-driver circuit. When the bit-line is dragged to '0' it also drags the corresponding internal data node of the enabled SRAM cell towards '0'.

Step 2: When this data node voltage goes lower than the switching threshold voltage of the other cross-coupled inverter, the feedback loop operation begins and then the latching of the data take place.

Let the time consumed in step 1 is denoted by $T_{discharge}$ and the time consumed by step 2 is denoted by $T_{latchup}$. The process variation in high frequency operation increases $T_{discharge}$ beyond the word-line activation period (T_{wl}) which leads to a write-failure. For a successful write operation the summation of $T_{discharge}$ and $T_{latchup}$ should be at most the T_{wl} [2].

Fig. 1 shows the schematic of a CC-SRAM cell which stores a 1 at 'Q' node and 0 at 'QB' node. To write a 0 to 'Q' node, the initially pre-charged bit-line 'BL' has to be dragged to 0 and 'BLB' has to be fixed at VDD. As per the stored data initially the NM1 is off and NM2 is on. Since NM2 is on initially the pre-charged bit line 'BLB' tries to elevate 'QB' node as well as the 'X' node by a little amount. This elevated 'X' node will come back to its original position after NM1 start conducting. So the 'X' node gets a temporary glitch during the state transition which can be marked from Fig. 3.

During the write operation the 'Q' node is discharged to 0. Since the 'X' node is temporarily increased during state transition, the V_{GS} of NM2 is less, in comparison to that in the case of a 6T-SRAM. Hence the NM2 stops conduction earlier and the feedback loop operation also starts earlier with respect a 6T-SRAM cell. This provides a higher probability of the summation of $T_{discharge}$ and $T_{latchup}$ to be smaller than the T_{wl}. Hence write-ability of the proposed SRAM cell increases than the conventional 6T-SRAM cell.

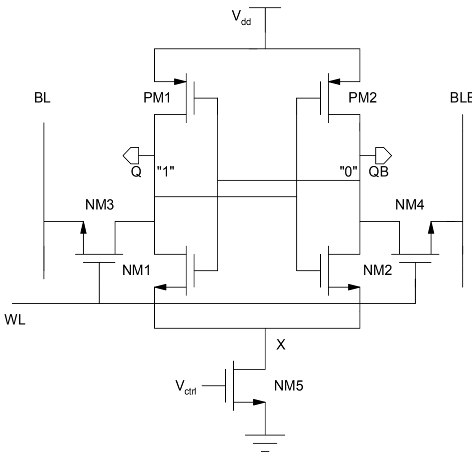

Fig. 1. Proposed CC-SRAM cell topology.

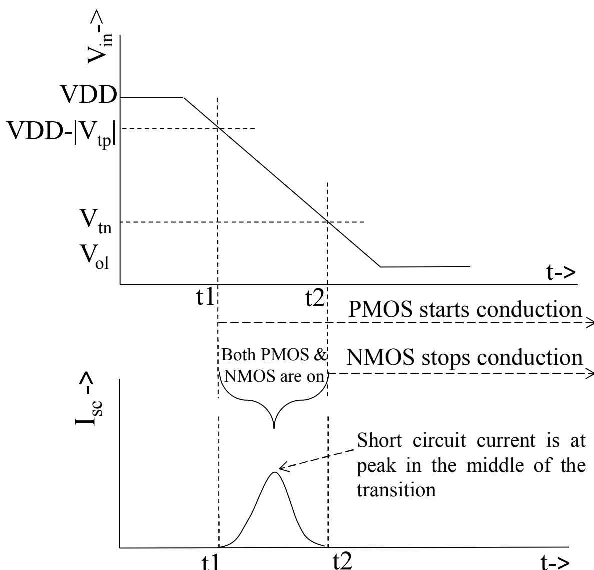

Fig. 2. Short circuit current during state change.

B. Reduction of Dynamic Power Consumption

During any dynamic operation a significant amount of power is wasted through the unavoidable short-circuit current. This is because of the fact that both pull-up and pull-down side transistor conducts in the interval between t1 to t2 as shown in Fig. 2 [3]. The dynamic power can be lowered by temporarily reducing the V_{ds} of the transistors undergoing state change. As the node 'X' voltage is elevated temporarily during state transition the V_{ds} of NM2 decreases. This reduces the short-circuit current of NM2 which leads to the reduction of the dynamic power consumption.

III. Comparative Performance Analysis

A SRAM array using the proposed SRAM cell was designed using Complimentary MOS technology. The memory block is simulated in cadence analog design environment at room temperature (27^0C) and using a power supply of 0.8V.

The conflicting nature between read stability and write-ability of the SRAM cell requires a careful selection of transistor size. During a read process the pre-charged bit lines tries to elevate the node containing '0'. If this elevated voltage increases than the switching threshold voltage of the other cross-coupled inverter than the stored data may flip erroneously. To avoid such situation the access transistor resistance should be kept more than the pull-down transistors resistance [4-6]. Keeping the above fact in mind the width of the pull-up transistors and access transistor are taken as 120nm. The width of the pull-down transistors and NM5 are taken as 240nm and 180nm respectively. The lengths of all the transistors are taken to be the minimum value as 100nm. The NM5 is provided a gate voltage of 500mV which keeps a balance between the read stability and write-ability.

A. Performance Enhancement in Term of Power

The SRAM array is accessed at a frequency of 1GHz and its transient analysis output is provided in Fig. 3. From the figure it is found that a '0' and a '1' are written to the cell at 1ns and 3ns respectively. Similarly the data is read out at 2ns and 4ns respectively. The power consumption of the SRAM cell for a simulation window from 1ns to 5ns is shown in Fig. 4. The power consumption during dynamic operations such as the read and write are added up and termed as total dynamic power. The power consumption during the stable interval are added up and termed as total static power. The dynamic and static power of the proposed cell is estimated and compared with that of the conventional 6T-SRAM cell. The power consumption of the 6T-SRAM cell is shown in Fig. 5. The comparison of power consumption is shown in Table I. from Table I it is found that the total power consumption of CC-SRAM cell is 15.3% lesser than the 6T-SRAM cell.

The power consumption during write operation decreases drastically which can be marked from Table I. This is because of the rise in node 'X' voltage from 0 to 191.232mV during the state transition (refer Fig. 3) which blocks the short-circuit current through the pull-down transistor.

TABLE I

POWER CONSUMPTION OF DIFFERENT SRAM CELLS DURING 1GHZ ACCESS

Operations → / SRAM Cells ↓	POWER CONSUMPTION (aW) DURING DYNAMIC OPERATIONS				TOTAL DYNAMIC POWER (aW) = A+B+C+D = (E)	TOTAL STATIC POWER (aW) (F)	TOTAL POWER (aW) =E+F	DECREMENT W.R.T. 6T-SRAM CELL (%)
	0-WRITE (A)	0-READ (B)	1-WRITE (C)	1-READ (D)				
CC-SRAM	1463	1265	1464	1246	5438	195.0	5633	15.33
6T-SRAM	1945	1320	1945	1305	6515	138.0	6653	-

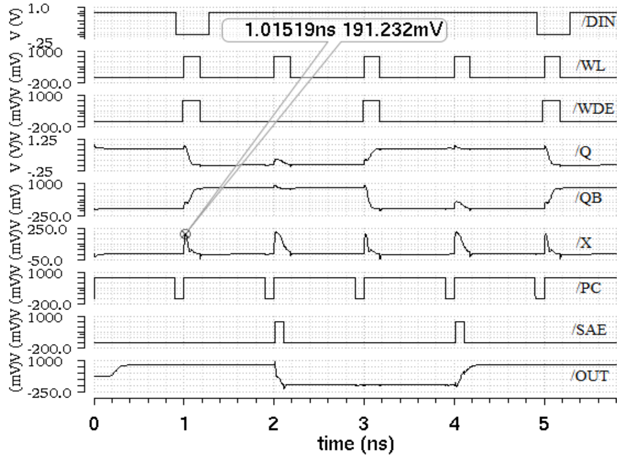

Fig. 3. Transient analysis of CC-SRAM cell at high frequency.

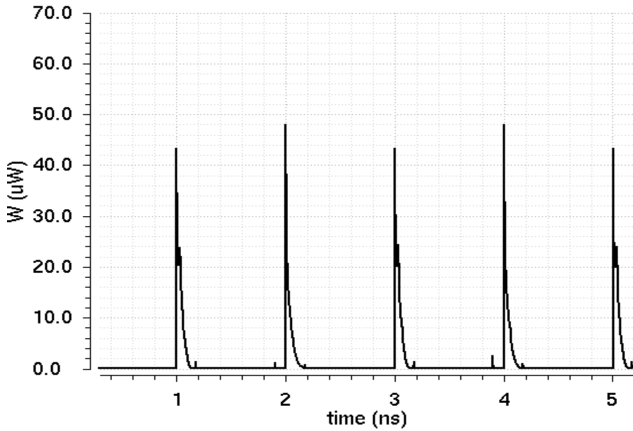

Fig. 4. Power consumption of CC-SRAM cell during 1GHz access

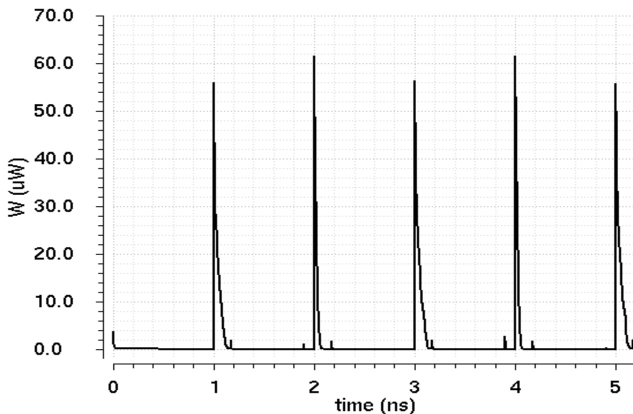

Fig. 5. Power consumption of 6T-SRAM cell during 1GHz access

B. Performance Enhancement in Term of Write-ability

The stability and write-ability of the SRAM cell are of equal importance as that of the power consumption. The two most commonly used techniques for stability measurement are Static Noise Margin (SNM) [7] and N-curve method [8]. There is no inline tester in SNM technique which is a major drawback of it [9]. N-curve is a simple technique which measures both the voltage and current information about the stability and write-ability of the SRAM cell with less effort.

There are four important parameters of N-Curve. The static voltage noise margin (SVNM) and static current noise margin (SINM) represents the stability of the SRAM cell. The write trip voltage (WTV) and write trip current (WTI) represents the write-ability of the SRAM cell. SVNM is the maximum input voltage which can flip the state of the cell. The maximum DC current that can be fed to the SRAM cell before flipping the state is known as SINM. The voltage required for writing a data to the cell is termed as WTV. WTI is the maximum trip current during the cell write when both lines are kept at V_{dd}.

For higher write-ability the WTV and WTI should be less. WTP which is the area under the curve from point B to C of the N-Curve (shown in Fig. 6) should be less for better write-ability. Similarly SPNM which is the area under curve from point A to B of the N-curve should be more for better stability [10].

The N-Curve for the CC-SRAM and 6T-SRAM are shown in Fig. 6 and 7 respectively. The N-Curve analysis shows that the SVNM and WTV of both the cell are nearly equal. But the SINM and WTI vary significantly. The SPNM of the proposed CC-SRAM cell decreases by 22.795% whereas the write-ability enhances by 63.610% which is a great enhancement in write-ability.

The improvement in write-ability is explained as follows. The 'X' node is raised to 191.232mV during the middle of state transition which can be found from Fig. 3. The increase in 'X' node voltage decreases the V_{gs} of NM2 which stops its conduction earlier. So the feedback loop operation starts earlier. This phenomenon can also be marked from Fig 8. Fig. 8 shows that in a CC-SRAM cell the feedback loop operation starts at 1.054ns when the 'Q' node is discharged up to 324.694mV. But Fig 9 shows that in 6T-SRAM cell the feedback loop operation starts at 1.070ns when the 'Q' node is discharged up to 252.394mV. Hence the write-cycle is finished within less time in CC-SRAM cell in comparison to 6T-SRAM cell. So the write-ability of the proposed CC-SRAM cell is much higher than the 6T-SRAM cell

TABLE II

N-CURVE ANALYSIS OF DIFFERENT SRAM CELLS

Different Cells	**SVNM** (mV)	**SINM** (μA)	**SPNM** (μW)	**WTV** (mV)	**WTI** (μA)	**WTP** (μW)
CC-SRAM	160.573	24.579	3.160	454.168	17.448	3.890
6T-SRAM	184.012	34.833	4.093	464.989	36.408	10.690
Decrement (%)			-22.795			63.610

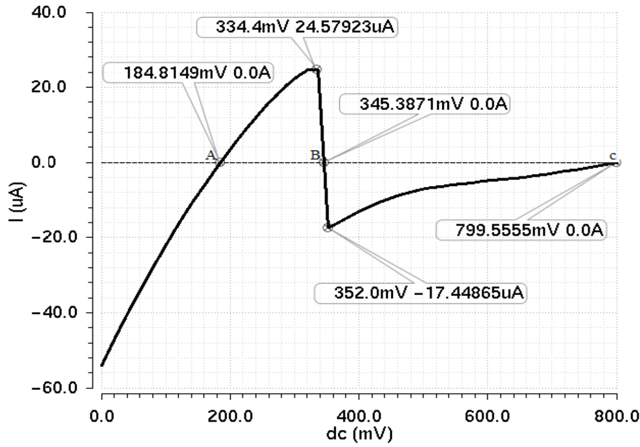

Fig. 6. N-Curve analysis of the proposed CC-SRAM cell

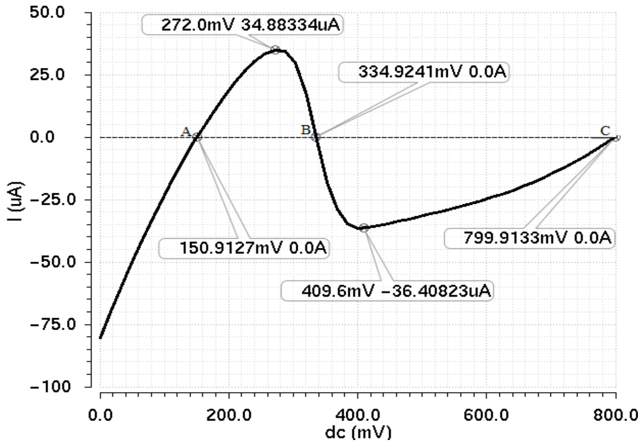

Fig. 7. N-Curve analysis of conventional 6T-SRAM cell

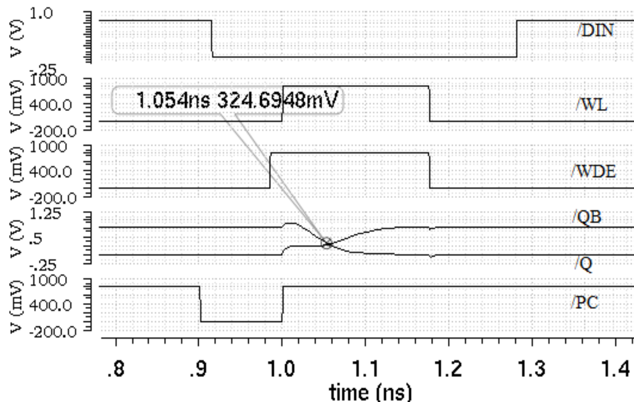

Fig. 8. Data write in case of the proposed CC-SRAM cell

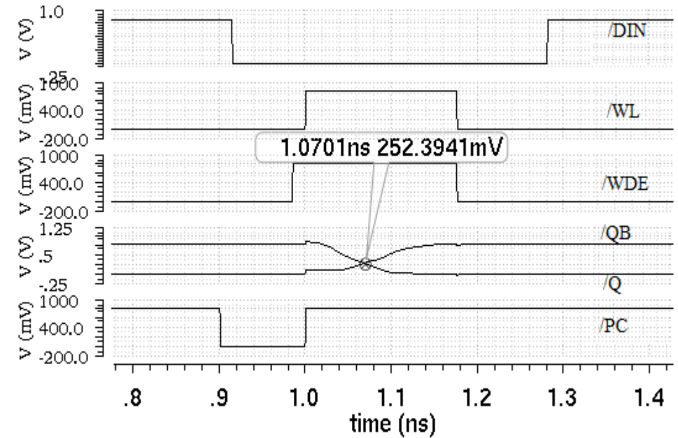

Fig. 9. Data write in case of the conventional 6T-SRAM cell

IV. PHYSICAL LAYOUT CONSIDERATIONS

The physical layout is designed for both the proposed CC-SRAM cell and the conventional 6T-SRAM cell using GPDK technology library. The SRAM cells are designed with great care such that they can be compact and symmetric. The layout is designed using a one-directional poly silicon layer [11] so that the word line resistance will be low. The array of the SRAM cell is designed in such a way that they can share a common VDD, GND, BL, BLB, WL port etc. with the neighboring cells wherever possible.

Fig. 10 shows the physical layout of the 6T-SRAM cell and Fig. 11 shows that of the proposed CC-SRAM cell. From the layout it can be found that there is a manageable area increment of the CC-SRAM cell considering its other advantage in terms of power and write-ability. Fig. 12 shows a smaller part of the large array which is designed using conventional 6T-SRAM cell and Fig. 13 shows that of the proposed CC-SRAM cell.

From Fig. 12 it is found that the cell(0,1) is flipped horizontally and overlapped on cell(0,0) so that the 'WL0' node can be shared by both cell(0,0) and cell(0,1). Similarly 'WL1' node is shared by both cell(1,0) and cell(1,1). The cell(1,0) is flipped vertically and overlapped on cell(0,0) so that the VDD, GND, BLB0 node are shared between them.

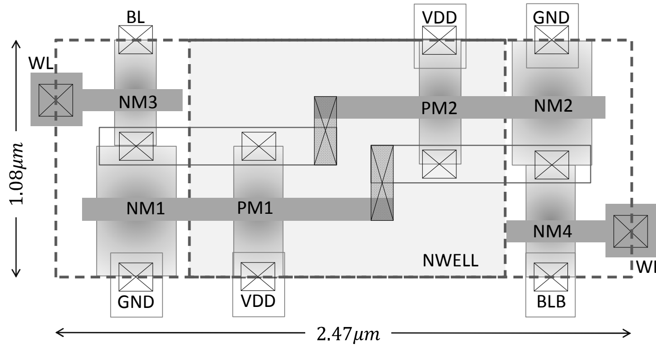

Fig. 10. Physical layout of 6T-SRAM cell

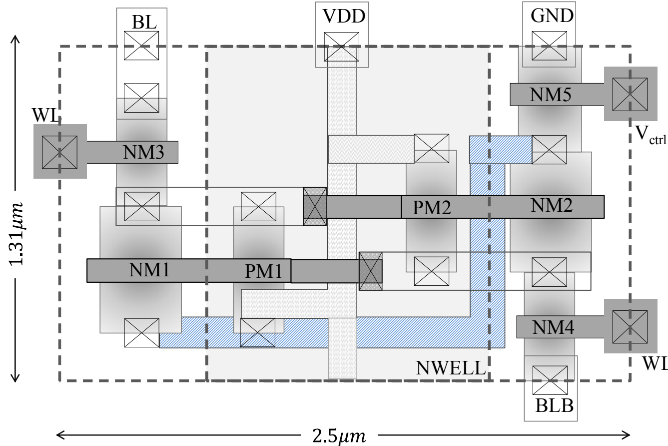

Fig. 11. Physical layout of CC-SRAM cell

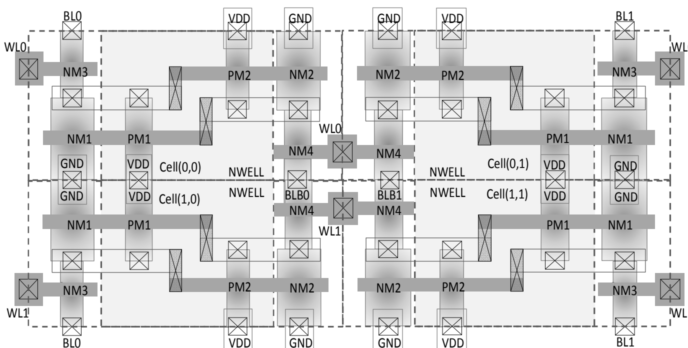

Fig. 12. Architecture of 6T-SRAM array

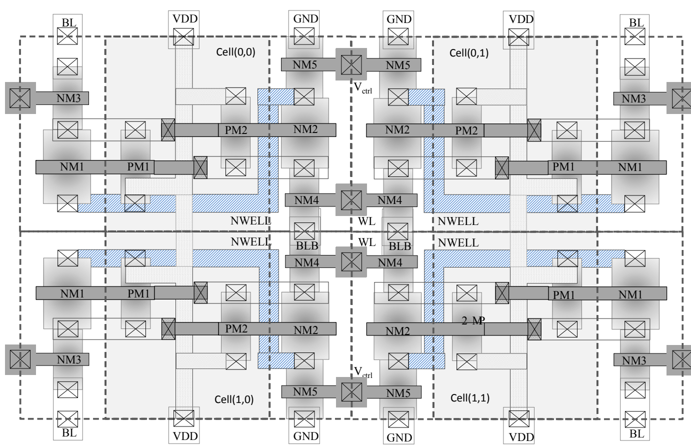

Fig. 13. Architecture of CC-SRAM array

V. Conclusion

A novel seven transistor based SRAM cell is designed using GPDK technology library. An array of this SRAM cell is designed and simulated at a frequency of 1GHz. Cadence analog design environment was used for the simulation purpose.

The cell has two advantages over 6T-SRAM cell. It reduces the total power consumption by 15.33% in comparison to 6T-SRAM cell. This is done by blocking the short-circuit current during state transition.

Secondly it increases the write-ability of the proposed CC-SRAM cell by 63%. This is achieved by starting the feedback-loop operation earlier than that in the 6T-SRAM cell.

The physical layout of the array of the proposed and conventional SRAM cells is designed and presented. The layout is designed such that they can share a single common node between each other which reduces area occupancy.

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