A 10-bit 500 MSPS Segmented DAC with Distributed Octal Biasing Scheme

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***Abstract*—The effect of bias node voltage fluctuations on the performance of the current steering (CS) DAC is studied in this work. For that purpose a 10-bit segmented CS-DAC has been designed in 0.18 μm CMOS n-well technology provided by National Semiconductor. All current sources connected to the same bias cell act as correlated noise sources and generates more nonlinearity at the output. To improve the spurious free dynamic range (SFDR) of the DAC a new octal biasing technique is used in this paper. In the octal biasing technique 8-bias cells are used and they are placed in a 4×2 array structure. There is no direct connection between any two bias cells and they are considered as non-correlated cells. Thus the octal biasing and the non-correlated current sources help to reduce the noise and the input code dependent nonlinearities at the output. In Monte Carlo mismatch simulation the proposed DAC achieves 60.83 dB SFDR for 15.136 MHz signal at 500 MSPS sampling rate. The DAC shows a Nyquist SFDR of 60.57 dB in for 500 MSPS sampling rate. The DAC consumes only 31.62 mW of power at Nyquist signal frequency for 500 MSPS sampling rate with 1.8 v supply.**

***Index Terms*—Current steering DAC, Segmentation, Octal Biasing, Matching, INL, DNL, Nyquist SFDR;**

I. Introduction

With the evolution in digital CMOS technology modern wireless communication systems utilize several complex digital modulation techniques to support the high data rate and wide signal bandwidth. The number of global subscribers for the 3G and 4G communication market have increased exponentially over the last decades. This has increased the production of smart phones and others portable wireless communication devices [1]. For that reason the demand of high speed DACs with improved spectral purity for the wireless transceivers has increased over the last few years [2], [3]. As the DAC is the first analog block in the signal path, the performance of the overall system depends on the accuracy of the DAC [4], [5] and often a poorly designed DAC could become the bottleneck for the system.

For high speed applications mostly segmented current steering DACs are used [9]. CS-DACs are fast and can drive a typical 50 Ω resistive load, without using any output buffer [6]. In current steering architecture some current sources are turned on or off depending on the input digital bits and the total output current is analogous to the digital inputs [7]. An on-chip current reference is used to generate the bias voltage for the current sources. The performance of the CS-DAC depends on the matching of the current sources [10] and the accuracy of the bias cells. The mismatch of the transistors is inversely proportional to the area of the transistor [16]. So matching can be improved by using larger transistors. Although, use of larger transistors increases the overall area and implementation cost of the DAC. Another disadvantage of using larger size for the current source transistor is that the associated parasitic capacitance will increase at the output node. Due to the increased parasitic capacitances, the output impedance of the current sources will drop rapidly at high signal frequency which will degrade the spectral performance of the DAC [11]–[13]. To overcome that problem, current sources should be implemented with optimum size transistors [14] to improve both static as well as dynamic performances of the DAC.

At high signal frequency the input code dependent switching noise and modulated output impedance dominates the spectral performance of the DAC. Due to switching transients, the bias node voltage fluctuates and affects all connected current sources that are common to that bias cell. This input code dependent bias node voltage variations create correlated noise in the associated current sources and degrades the overall linearity of the DAC.

In this work, to reduce the correlated noise among the current sources, eight separate and independent bias cells are used. The optimum size of the current source is calculated in this paper, to achieve improved spectral performances and better linearity. The rest of the paper is organized as follows. The architecture of the DAC and its major blocks are described in Section II. The simulation results are described in Section III and finally, Section IV, summarizes the paper.

II. Architecture

The schematic of the 10-bit DAC is shown in Fig. 1, where, four (B0-B3) least significant bits (LSB) control the 4-bit binary DAC. The binary part is implemented with four binary weighted current cells of amplitudes I, 2I, 4I and 8I respectively, where, I represent the weight of the LSB current source. In this work the value of I is chosen as 5 μA. The six (B4-B9) most significant bits (MSB) are implemented in unary architecture. The 6-bit MSB unary DAC is composed

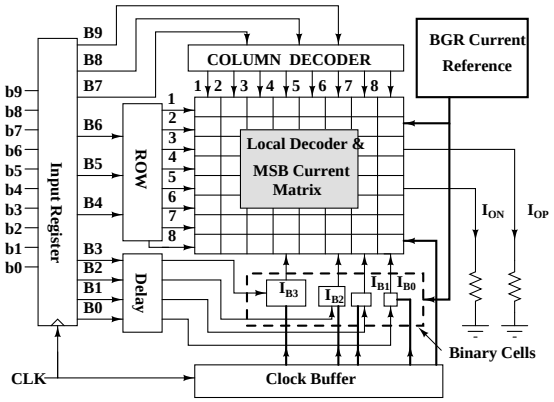

Fig. 1. Architecture of the 10-bit segmented DAC

with 63 unit current sources of weight 16I. To realize the current cells in a compact and regular geometrical structure an 8×8 current source matrix is used. The MSB binary-to-thermometric decoders are further segmented in row and column decoders. The 3-MSB bits (B7-B9) are used to design the 3-to-8 column decoder and the next three-bits (B4-B6) are used for the 3-to-8 row decoder. The row and column decoder outputs are combined in the local decoder matrix, which generates the final control signals for the MSB unit cells. To synchronize the MSB and LSB sub-DACs a delay equalizer block is designed for the binary part. Differential current switches are used to generate the differential current outputs. The design of the major building blocks of the DAC are described in the next sub-section.

A. Design of the 10-bit Segmented DAC

1) Binary-to-Thermometric Row and Column Decoder: In the proposed DAC, six-MSB bits are implemented in unary DAC, which is composed of 63-weighted unit current sources. To control these unit cells, 63 number of binary-to-thermometric decoder outputs are required. The 63 decoder outputs are implemented in an 8×8 array for a compact rectangular area. The first three MSB bits (B7-B9) are used for column decoding and next three bits (B4-B6) are used in row decoding. The schematic of the 3-to-8 row and column decoders are shown in Fig. 2(a) and Fig. 2(b) respectively.

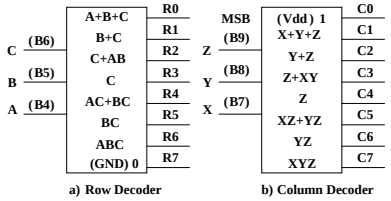

Fig. 2. Schematic of the row and column decoders

2) Local Decoder: As shown in Fig. 1, the row and column decoder outputs are again combined in the local decoder matrix to generate the final control signals for the current switches. The local decoding logic of the MSB unit cells are equivalent to an AND-OR gate function [9] and is shown in Fig. 3.

3) Design of the Final Re-timing Latch: The circuit of the final re-timing latch is shown in Fig. 4 [13], [15]. Differential switch transistors are used to steer the DC current of the current sources to any of the differential output. As shown in Fig. 5 (a), slightly overlapped differential switch control signals are used for that purpose, so that during transition both of the switch transistors are never turned off simultaneously. Extra NMOS transistors (N3 and N4) are used in the design of the latch to generate the overlapped differential switch control signals by modifying the rise and fall times [13].

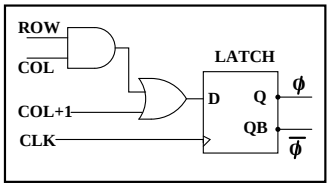

Fig. 3. Local decoder for the MSB unit current cells

4) Current Sources and Differential Current Switches: In CS-DAC, the INL is mainly determined by the matching of the current sources. Matching among the current sources depends on the area of the transistors. Over-sizing of the current sources degrades the performance of the DAC at high signal frequencies. So, the current sources are designed with optimum sizes to achieve high static and dynamic performances up to Nyquist signal frequency. The minimum required area of the current sources is obtained following Eq. 1 [16].

$$(W \times L)_{min} = \frac{\frac{4A_{Vt}^2}{(V_{GS}-V_t)^2} + A_\beta^2}{2 \times \frac{\sigma^2(I)}{I^2}} \quad (1)$$

In Eq. 1, A_{Vt} and A_β are process mismatch parameters. V_{GS} is the gate-to-source voltage and V_t is the threshold voltage of the MOS transistor. Following Eq. 1, the size the LSB cell for the LSB current of 5 μA, is chosen as 1.5 μm×1.5 μm as shown in Fig. 5 (b). The size of the cascode transistor is chosen as 1.5 μm×0.3 μm. The fingering of the PMOS transistors have been increased proportionally with the weight of the current sources.

Care has been taken to design the switch control signals, so that the differential switches work in make before break fashion to avoid unnecessary switching transients and nonlinearity at the output of the DAC. The differential overlapped switch control signals are shown in Fig. 5 (a). As shown in Fig. 5 (b), the size of the LSB current switches are 450 nm×180 nm. The number of finger of the PMOS switch transistors increases according to the weight of the current sources.

5) Biasing scheme of the current sources: To bias the current sources a bandgap current reference circuit is designed. Options of using external reference current is also included in the circuit. In that case the on-chip current reference will be put in sleep mode to save power. The bias generators are divided into 8-bias cells placed in 4×2 array structure as

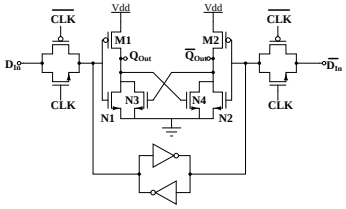

Fig. 4. Final latch circuit

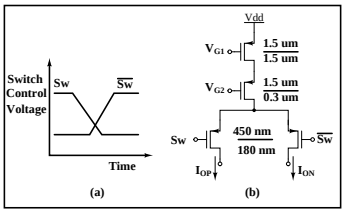

Fig. 5. LSB current source with differential current switches

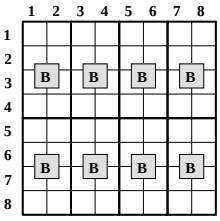

Fig. 6. Biasing scheme of the MSB unit current sources

shown in Fig. 6. There is no direct connection between any two bias cells and they are considered as non-correlated cells. In the CS-DAC, whenever any switch transistor is turned on the corresponding current cell draws additional switching currents and creates transitional glitches at the DC bias voltage. The other current sources connected with the same bias cell, suffers from this bias voltage fluctuation, even if it is not transiting. All current sources connected to the same bias cells thus suffer from input code dependent switching noise and as these current sources are correlated, total output noise increase. The current sources connected with different bias cells are independent and are not affected due to the switching of current sources connected with other bias cells. Thus the octal biasing scheme proposed in this work helps to reduce the correlated noise among the current sources. Use of array structure for the bias sources also help to reduce the input code dependent nonlinearities at the output and improves the SFDR. Use of octal bias cells also help to improve the INL and DNL by reducing the gradient errors [8].

III. Simulation Results

In simulation the DAC achieves a maximum DNL of 0.047 LSB and a maximum INL of 0.057 LSB, respectively. The DNL and INL plots are shown in Fig. 7 and Fig. 8, respectively. In Monte Carlo mismatch simulation the 6+4 segmented DAC achieves 60.83 dB SFDR for 15.136 MHz signal at 500 MSPS sampling rate and the output spectrum

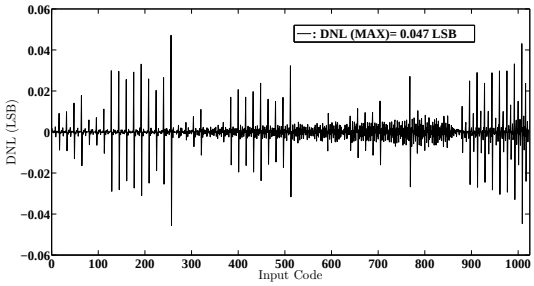

Fig. 7. Simulated DNL plot of the DAC

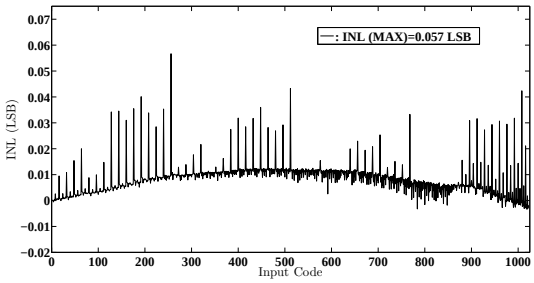

Fig. 8. Simulated INL plot of the DAC

is shown in Fig. 9. The DAC shows a Nyquist SFDR of 60.57 dB in Fig. 10 for 500 MSPS sampling rate. A two-tone test gives better information about the DAC's ability to output real modulated signals [13]. As shown in Fig. 11, the proposed DAC achieves 62.57 dB IM3 for dual tone spectrum with 245.60 and 247.56 MHz signals at 500 MSPS sampling rate in mismatch condition. The DAC consumes 31.62 mW of power at Nyquist signal frequency at 500 MSPS sampling rate with 1.8 v supply. The details of the simulation results

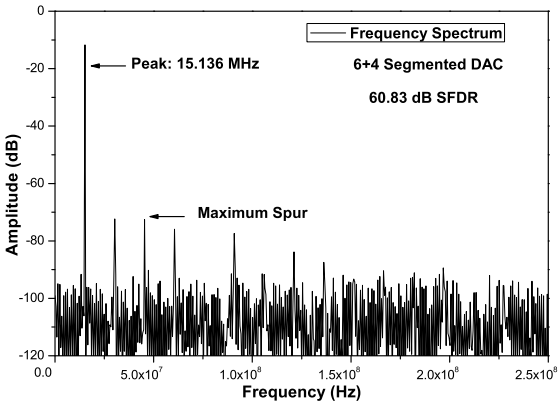

Fig. 9. Frequency spectrum of the DAC for 15.136 MHz signal with 60.83 dB SFDR at 500 MSPS sampling rate

are summarized in Table I. It is evident from the table, that the proposed DAC with the octal biasing scheme is able to maintain a constant SFDR of >60 dB throughout the Nyquist band even in mismatch condition.

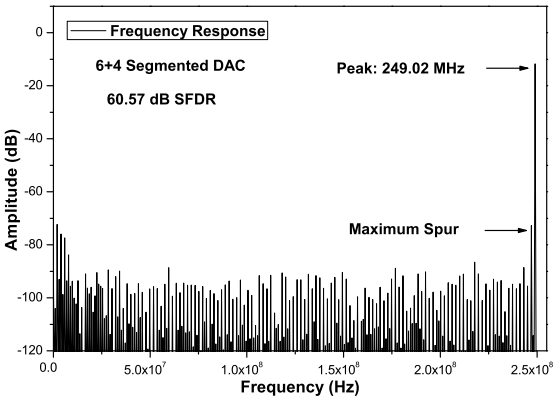

Fig. 10. Frequency spectrum of the proposed DAC showing 60.57 dB SFDR for 249.05 MHz signal

TABLE I
SUMMARY OF THE PROPOSED 10-BIT DAC

Sampling Rate	500 MSPS
DNL (LSB)	0.047 LSB
INL (LSB)	0.057 LSB
Power Supply	1.8 V
Power Dissipation (at Nyquist)	31.62 mW@500 MSPS
SFDR	60.83 dB@15.136 MHz 60.57 dB@249.05 MHz
IM3	62.57 dB 245.60 and 247.56 MHz
Process	0.18 μm CMOS

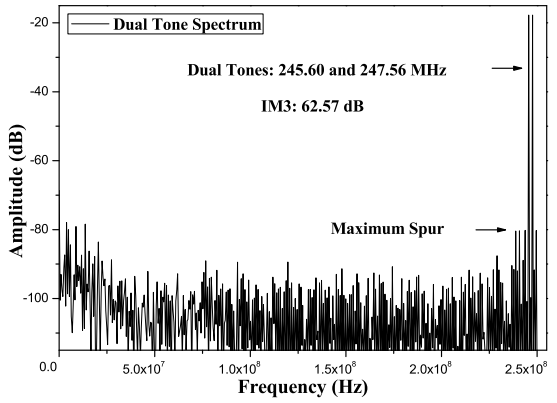

Fig. 11. Dual tone spectrum of the proposed DAC showing 62.57 dB IM3, considering the mismatch effect

IV. CONCLUSIONS

This paper presents the design of a 10 bit 500 MS/s segmented CS-DAC with octal biasing scheme. The DAC has been designed in 0.18 μm five-metal CMOS process. To improve the matching of the current sources optimum transistor sizes are selected. An on chip bandgap current reference circuit is used to provide the bias voltages for the current sources. To reduce the input code dependent variation of the bias node voltages, eight different bias cells are used for the MSB unit current source matrix. Simulation results show that the DAC achieves a maximum DNL of 0.047 LSB and an INL of 0.057 LSB. The proposed DAC achieves an almost constant SFDR of $>$60 dB throughout the Nyquist band even in mismatch environment. The third order inter modulation distortion of the DAC is 62.57 dB for a dual tone spectrum of 245.60 MHz and 247.56 MHz signals sampled at 500 MSPS. The simulated power consumption of the DAC is 31.62 mW at Nyquist signal sampled at 500 MSPS with 1.8 V of DC power supply.

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