A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect

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***Abstract*—This paper describes the design techniques of a segmented current steering (CS) digital-to-analog converter (DAC) with optimum sizing of the current sources. The DAC has been designed in 0.18 μm CMOS n-well technology provided by National Semiconductor. The 10-bit DAC is segmented as 5+5, where the 5-LSB bits are implemented in binary and the 5-MSB bits are implemented in unary architecture. The matching of the unit current sources plays an important role in determining the overall linearity of the DAC. Static linearity of the DAC can be improved by using larger area of the current source transistors, sacrificing the dynamic performances. At high frequency the spectral performance of the DAC degrades due to the increased parasitic. In this work the current sources are designed with optimum sizes to achieve improved static as well as dynamic performances. In simulation, the DAC achieves a maximum DNL of 0.248 LSB and a maximum INL of 0.440 LSB. The DAC achieves a maximum spurious free dynamic range (SFDR) of 59.79 dB for 5.37 MHz signal in mismatch environment at 500 MSPS sampling rate. The DAC shows a Nyquist SFDR of 57 dB at 500 MSPS sampling rate with mismatch. The DAC consumes only 17.85 mW of power for Nyquist signal at 500 MSPS sampling rate with 1.8 V supply.**

***Index Terms*—Current steering DAC; Segmented DAC; Matching; INL; DNL; Low Power; SFDR; Nyquist Signal Frequency;**

I. Introduction

Due to the recent growth in 3G and 4G communication systems the demand of low power, single chip wireless transceivers for portable terminals is growing rapidly. To realize the concept of always connectivity, the wireless transceiver uses reconfigurable baseband and RF architectures to operate at different standards (GSM, UMTS, WLANs, Bluetooth) [1]. With the advancement of digital CMOS technology, it is now possible to implement the reconfigurable and multimode digital transmitters for wireless communications. Present transceiver systems, use several complex digital modulation techniques. Inclusion of more features into the system demands more spectral purity from the output signal. As DAC is the first analog block in the signal chain, it determines the performance of the overall system [1]. Unless design with high care, the DAC could become the bottleneck for the signal path [2]. For that reason the demand of high performance and high speed DAC has increased over the years [3]. Typical block diagram of a direct transmitter system is shown in Fig. 1, where the digital I and Q baseband signals are converted to analog form by using two baseband DACs [4].

For high speed applications current steering architecture is most suitable as it is inherently fast and can drive a typical resistive load of 50 Ω without using any output buffer [5]. Conventional CS-DACs are classified in three sub-categories, namely, unary, binary and segmented architectures [6]. For DACs with larger resolution, segmented CS-architectures are used. Segmented DAC, which is composed of both unary and binary DACs [7], [8] retains the advantages of both architectures. Generally segmented DAC is divided in two parts, the MSB section and the LSB section [6]. To achieve better linearity the MSB section is implemented in unary DAC, and to save the total area, LSB section is implemented in binary DAC.

The performance of the current steering DAC depends on

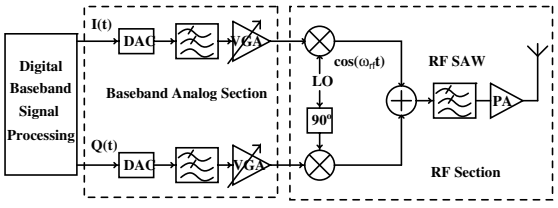

Fig. 1. Block diagram of a typical direct transmitter system

the matching of the current sources [9]. Use of larger transistors to implement the current sources helps to improve the matching [10], [11] among the current cells. Use of larger transistors increase the overall area and implementation cost of the DAC. Also due to increased parasitic the performance of the DAC degrades at high frequency. For that reason, it is always better to implement the current sources with optimum size to improve the static as well as the dynamic performances. In this work the optimum sizes of the current source transistors are determined to achieve improved spectral performances. To

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reduce the correlated noise of the current sources due to the common bias cells, distributed bias sources are used for the 10-bit DAC. The remaining sections of the paper are organized as follows. The architecture and the design of the different sub-blocks of the DAC are described in Section II. The simulation results of the proposed DAC are described in Section III. Finally, Section IV, concludes the paper.

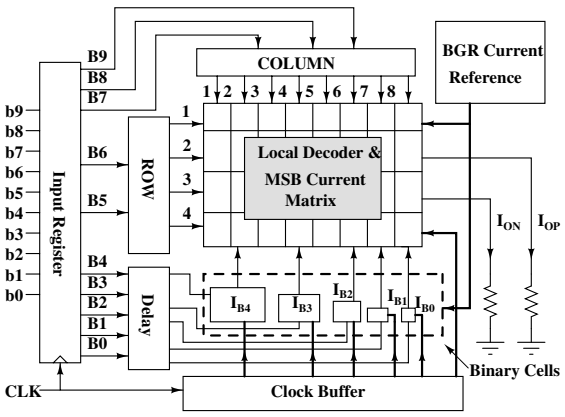

Fig. 2. Block diagram of the 10-bit segmented DAC

II. Architecture

The block diagram of the proposed DAC is shown in Fig. 2. In the figure, (B0-B4) the five-least significant bits (LSB) are used to control the 5-bit sub-binary DAC. The binary sub-DAC is implemented with five binary weighted current sources of amplitudes I, 2I, 4I, 8I and 16I respectively. Here, I is the weight of the LSB current cell and the value of I is chosen as 5 μA. The (B5-B9) five-most significant bits (MSB) are used to generate the binary-to-thermometric decoder outputs to control the MSB unit weighted cells. The 5-bit MSB-unary DAC is composed of 31 unit cells of weight 32I. A 4×8 current matrix is used to realize the current cells in a rectangular geometrical structure. The 3-MSB bits (B7-B9) are sent to the 3-to-8 binary-to-thermometric column decoder and the next two-bits (B5-B6) are sent to the 2-to-4 binary-to-thermometric row decoder. The row and column decoder outputs are again combined in the local decoder matrix to generate the final control signals for the MSB unit cells. As the binary sub-DAC does not require any decoder, a delay equalizer block is designed for the binary section to synchronize the control signals of the two blocks. Cascoded PMOS transistors are used to implement the current sources and differential current switches are used to generate the current outputs. An on chip bandgap current reference (BGR) circuit is used to generate the bias voltages for the current sources.

There are several digital blocks in the digital-to-analog data converter. Important digital blocks include input registers, row and column decoders, local decoders and final re-timing latch. The analog part of the DAC includes, current sources, current switches and current reference circuit. The design technique of the important building blocks are described in the next sub-sections.

A. Design of the Input Register

In the proposed DAC, 10-bit input registers are used to synchronise the digital data with respect to the internal clock. A master-slave positive edge triggered D-flip flop is used as the input register [12]. A multiplexer-based latch is used for that purpose and the schematic is shown in Fig. 3. The multiplexer is implemented by using transmission gates. When the clock is low, the master stage is transparent and the D-input is passed to the master stage output. During this phase the slave is in hold mode and keeps the value of the previous clock by using feedback. On the rising edge of the clock the slave stage samples the data of the master stage output and the master stage stops sampling the input. The value of the output is the value of the D-input right before the rising edge of the clock and so it acts as a positive edge-triggered register. Static CMOS design style is used to achieve a robust design.

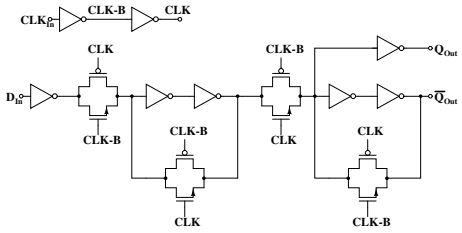

Fig. 3. Schematic of the D-flip flop

B. Design of the Row and Column Decoder

The proposed DAC uses five MSB bits for binary-to-thermometric decoder design. For the 10-bit inputs the first three MSB bits (B7-B9) are used for column decoding and next two bits (B5-B6) are used in row decoding. For the 32 decoder outputs an 4×8 array is used for a rectangular layout area. The 3-to-8 column decoder generates eight decoded outputs which control corresponding eight columns. The 2-to-4 row decoder generates control signals corresponding to the four rows. The schematic of the row and column decoders are shown in Fig. 4(a) and Fig. 4(b) respectively.

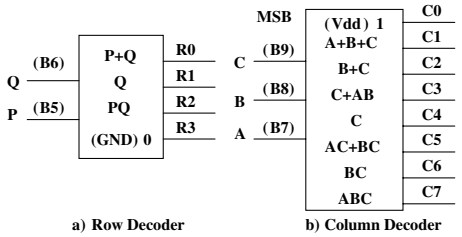

Fig. 4. Schematic of the row and column decoders

C. Design of the Local Decoder

As shown in Fig. 2, the row and column decoder outputs are again combined in the local decoder matrix to generate the final control signals for the current switches. In the proposed 10-bit DAC there are 31 number of MSB unit cells. The local decoding logic of the MSB unit cells are equivalent to an AND-OR gate function [8] as shown in Fig. 5.

D. Design of the Final Re-timing Latch

The circuit of the final re-timing latch is shown in Fig. 6 [11], [12]. As PMOS transistors are used for the design of the differential current switches, the latch is designed with PMOS drivers. Care should be taken to design the slightly overlapped switch control signals to ensure make-before-brake operation of the differential current switches. Otherwise, for any transition if both switches are off-for a small moment, the common source node of the switches will be charged up to V_{DD}. For the next transition, the node capacitance first need to be discharged to presume normal operation and thus creates large glitches and transition delay degrading the performance of the DAC. Extra NMOS transistors are used in the design of the latch to generate the overlapped differential switch control signals by modifying the rise and fall times [11].

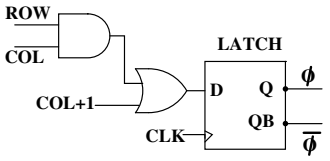

Fig. 5. Local decoder for the 31 MSB unit current cells

E. Design of the Current Sources

In CS-DAC, the INL is mainly determined by the matching of the current sources. Increasing the sizes of the current source transistors help to improve the matching of the current cells. Although, over-sizing may degrade the performance of the DAC at high signal frequencies. It is always better to design the current sources with optimum size to maintain high performances at all signal frequencies. To predict the INL within a certain boundary the INL yield is used as the percentage of the working DACs with an INL smaller than 0.5 LSB [13]. The relative standard deviation σ(I)/I, of unit current sources should satisfy the relationship given in Eq. 1, to achieve an upper bound of INL ($INL_{Upper-Bound}$) [14]. In the equation, *inv-normal* is the inverse cumulative normal distribution and *N* is the resolution of the DAC. The minimum required area of the current sources is obtained following Eq. 2 [15]:

$$\frac{\sigma^2(I)}{I^2} \leq \frac{INL_{Upper-Bound}}{inv-normal(0.5+\frac{INL_{yield}}{2}).\sqrt{2^{(N-1)}}} \quad (1)$$

$$(W \times L)_{min} = \frac{\frac{4A_{Vt}^2}{(V_{GS}-V_t)^2} + A_\beta^2}{2 \times \frac{\sigma^2(I)}{I^2}} \quad (2)$$

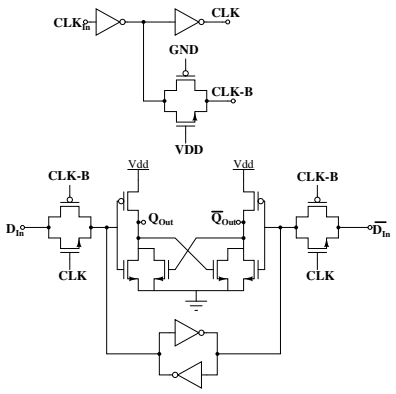

Fig. 6. Final latch circuit

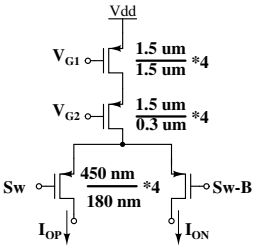

Fig. 7. 20 μA current source with differential current switches

where A_{Vt} and A_β are process mismatch parameters. V_{GS} is the MOS transistor's gate-to-source voltage and V_t is the threshold voltage. To reduce the minimum required area of the current cells, large overdrive voltage of 457 mV is used . For the LSB current of 5 μA the size the LSB cell is chosen as 1.5 μm$\times$1.5 μm, satisfying Eq. 2. The size of the cascode transistor is chosen as 1.5 μm$\times$0.3 μm. For 10 μA current the number of finger of the PMOS transistors are increased to two and for 20 μA current the number of finger is four. The finger number increases accordingly with the weight of the current sources. The schematic of the current source for 20 μA is shown in Fig. 7.

F. Design of the Current Switches

For the proposed DAC, PMOS transistors are used to design the differential current switches. The differential switch pairs are designed with minimum length. The size of the switch transistor for LSB current source is 450 nm$\times$180 nm. For current switches of 10 μA current cells the number of finger of the PMOS switch transistors are increased to two. For 20 μA current the number of finger is four as shown in Fig. 7. For the rest of the weighted current sources, the size of the switch transistors increases accordingly.

G. Design of the Current Reference Circuit

To bias the current sources a bandgap current reference circuit is designed. The schematic of the BGR is shown in Fig. 8. A two stage operational trans-conductance amplifier (OTA) has been designed for the band gap current reference.

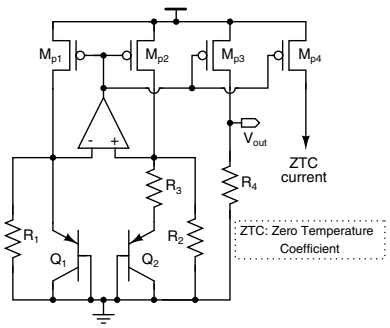

Fig. 8. Band-gap current reference circuit

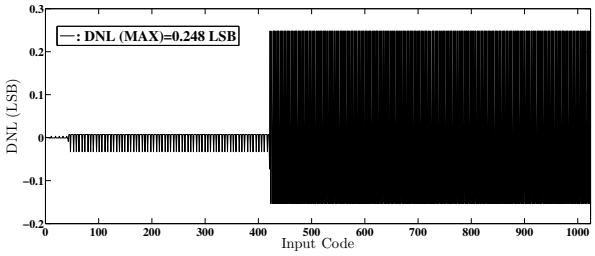

Fig. 9. Simulated DNL plot of the DAC

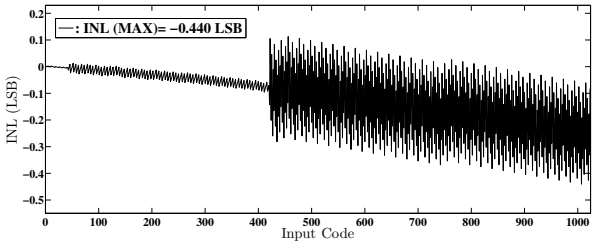

Fig. 10. Simulated INL plot of the DAC

III. Simulation Results

In Spice simulation at normal condition the segmented DAC achieves a maximum DNL of 0.248 LSB and an INL 0.440 LSB, as shown in Fig. 9 and Fig. 10 respectively. Cadence Virtuoso 6.1.4 ADE XL tool is used for the Monte Carlo-mismatch analysis of the proposed DAC. Mismatch effect is considered for the whole DAC and same mismatch seed is used for all simulations result in this paper. The DAC achieves a SFDR of 59.79 dB in mismatch environment for 5.37 MHz signal at 500 MSPS sampling rate, as shown in Fig. 11. The DAC achieves a mismatch simulated SFDR of 57.98 dB, for 15.136 MHz signal at 500 MSPS sampling rate and the output spectrum is shown in Fig. 12. The DAC shows a Nyquist SFDR of 57 dB for 249.02 MHz at 500 MSPS sampling rate and the corresponding frequency spectrum is shown in Fig. 13.

In present wireless transmitters, several multi-carrier digital modulation techniques are used and the modulated signals are directly fed into the DAC. In such case, a two-tone test gives better information about the DAC's performances for real modulated signals [11]. The DAC produces an IM3 of 50.66 dB for dual tone test with 245.60 and 247.56 MHz signals at 500 MSPS sampling rate as shown in Fig. 14. The 5+5 segmented DAC consumes 17.85 mW of power at Nyquist frequency for 500 MSPS sampling rate with 1.8 V supply.

The performance metrics of the proposed 10-bit DAC are

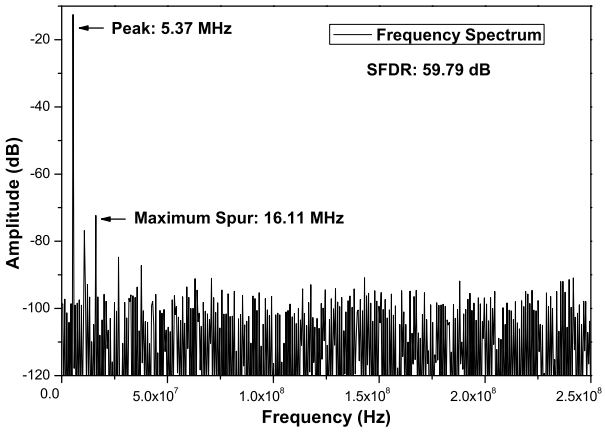

Fig. 11. Mismatch simulated output spectrum showing 59.79 dB SFDR for 5.37 MHz signal sampled at 500 MSPS

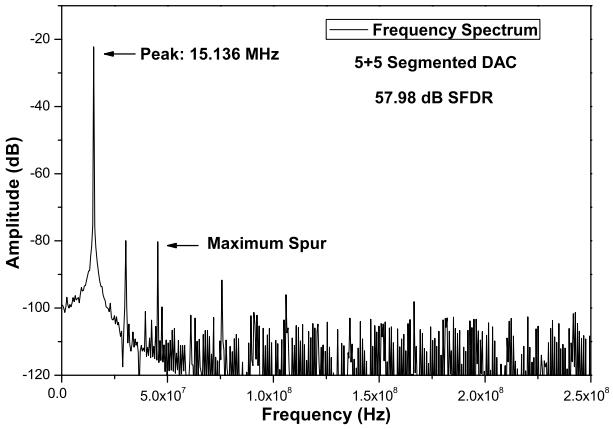

Fig. 12. Frequency spectrum showing 57.98 dB SFDR for 15.136 MHz signal, considering the effect of mismatch

summarized in Table I at the end of this section. To evaluate the overall performance of the proposed DAC, the figure of merit (FOM) described in Eq. 3 [16] is used. The proposed 10-bit DAC achieves 1.35×10^4 GHz/mW of FOM in Table I. The FOM of the DAC can be improved further by increasing the percentage of segmentation, where more number of bits will be implemented in unary architecture.

$$FOM = \frac{2^{\frac{SFDR_{dc}-1.76}{6.02}} \times 2^{\frac{SFDR_{Nyquist}-1.76}{6.02}} \times f_{clk}}{P_{total} - \frac{1}{2}{I_{load}}^2 \times R_{load}} \quad (3)$$

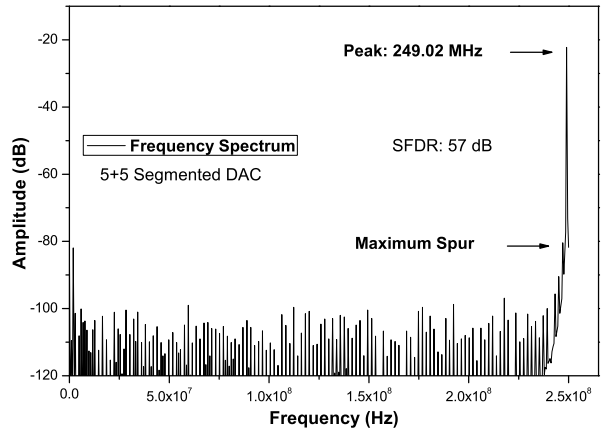

Fig. 13. Frequency spectrum of the DAC showing 57 dB of Nyquist SFDR for 500 MSPS clock rate with mismatch

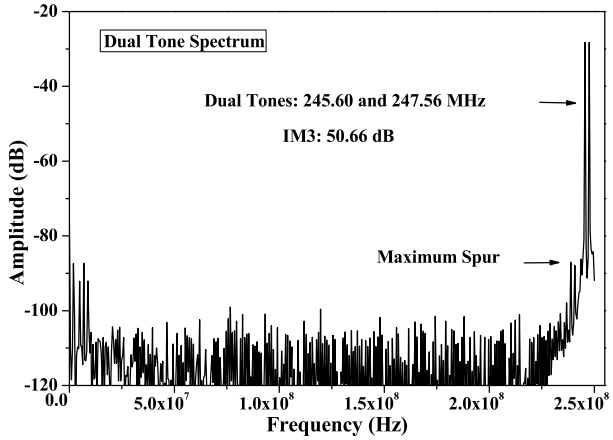

Fig. 14. Dual tone spectrum showing 50.66 dB of IM3 for 245.60 and 247.56 MHz signals, considering the mismatch effect

TABLE I
SUMMARY OF THE SIMULATION RESULTS OF THE PROPOSED 10-BIT DAC

Sampling Rate	500 MSPS
DNL (LSB)	0.248 LSB
INL (LSB)	0.440 LSB
Power Supply	1.8 V
Power Dissipation (at Nyquist Signal)	17.85 mW@500 MSPS
SFDR	59.79 dB@5.37 MHz 57 dB@249.02 MHz
IM3	50.66 dB@245.60 and 247.56 MHz
FOM	1.35×10^4 GHz/mW
Process	0.18 μm CMOS

IV. CONCLUSIONS

In this paper a 10 bit 500 MS/s segmented current steering DAC is presented. The DAC has been designed for wireless transmitters for reconfigurable multi-standard terminals. To improve matching between the unit current sources optimum transistor size is selected and an on chip bandgap current reference circuit is used for biasing the current sources. The DAC has been designed using 0.18 μm five-metal CMOS process. The DAC exhibits 10-bit intrinsic linearity. Simulation results show that the DAC achieves a maximum DNL of 0.248 LSB and an INL of 0.440 LSB. The DAC achieves an IM3 of 50.66 dB for dual tone test with 245.60 and 247.56 MHz signals at 500 MSPS sampling rate considering the effect of mismatch. The proposed DAC achieves a maximum mismatch simulated SFDR of 59.79 dB for 5.37 MHz signal at 500 MSPS sampling rate. The DAC achieves a Nyquist SFDR of 57 dB for 249.02 MHz signal at 500 MSPS sampling rate even at mismatch environment. The driving load for the DAC is considered as 50 Ω resistance. The simulated maximum power dissipation of the DAC is only 17.85 mW at Nyquist signal frequency sampled with 500 MSPS for 1.8 V DC supply. The DAC achieves moderate FOM in Table I without using any additional complex design techniques.

ACKNOWLEDGMENT

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A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect

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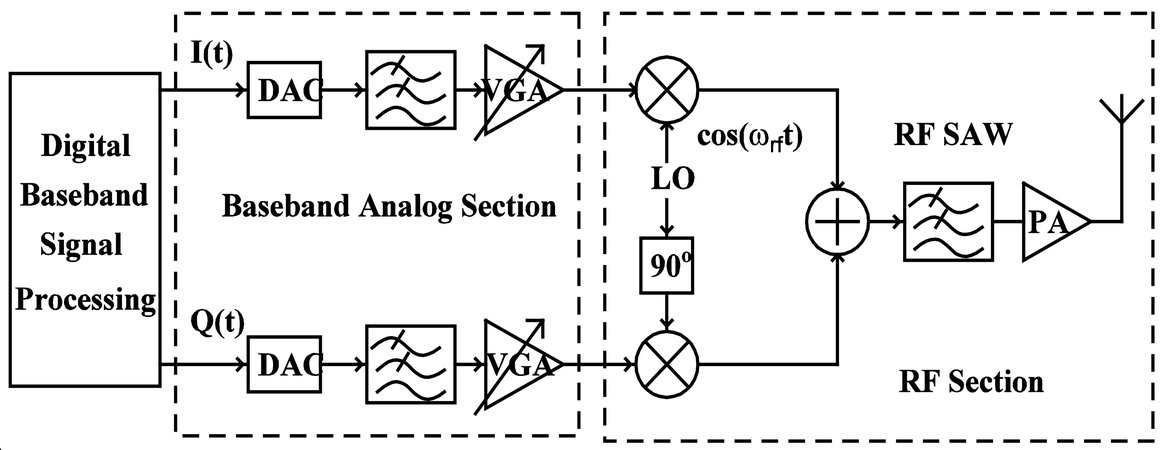
Introduction

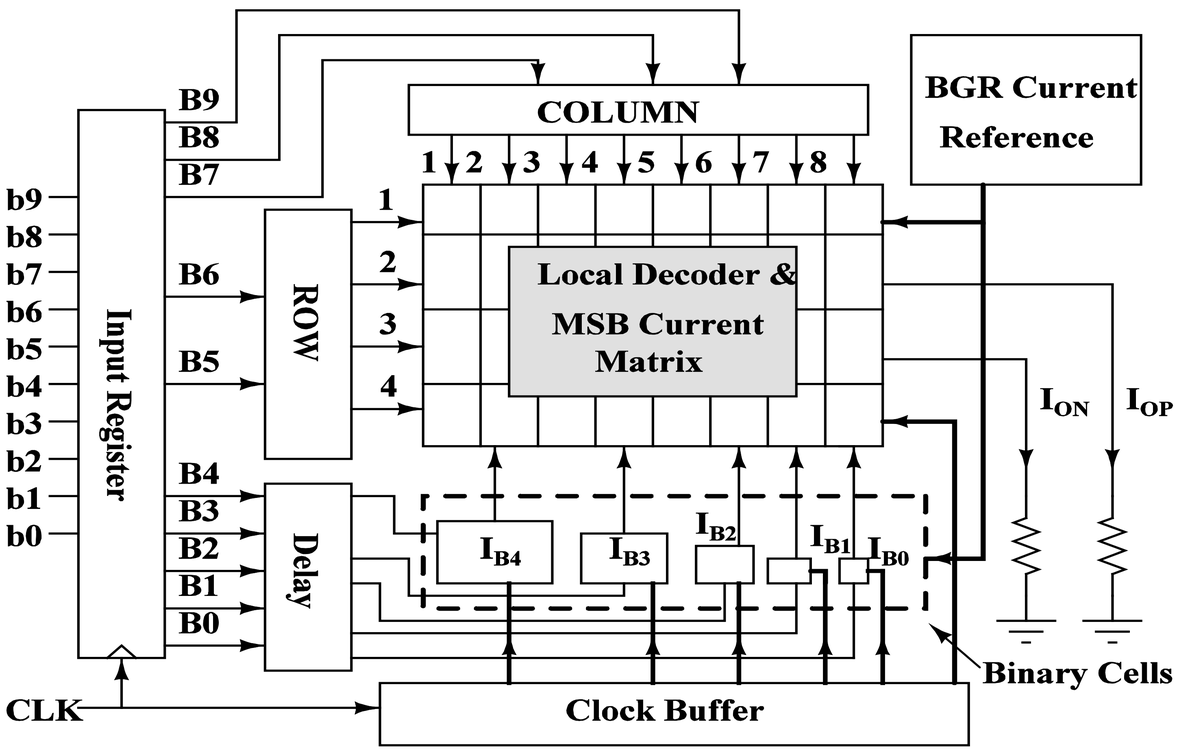
- Over the last decade the demand of low power, single chip wireless transceivers for portable terminals has increased rapidly.
  - Present transceiver systems includes several complex digital modulation techniques. The increased data rate and high signal bandwidth demands more spectral purity from the output signal.
    - As DAC is the first analog block in the signal chain of the transceiver system, it determines the overall spectral performance of the system.



- Block Diagram of the typical direct transceiver system

Motivation and Background

- The demand of high performance DAC has increased with the development of the digital transceiver systems. For high speed Current Steering (CS) Architecture is most suitable as it is inherently fast and can drive typical 50 Ω resistive load without using any voltage buffer.
  - CS Architecture can be classified into three sub-topologies namely, Unary, Binary and Segmented DACs.
    - For large resolution (> 10 bits) Segmented Architecture is most suitable to realize a high performance DAC.



- Block Diagram of the 10-bit Segmented DAC

- The 10-bit DAC has been Segmented as 5+5. The DAC has been designed in 0.18 µm n-well CMOS process.

Major Contributions

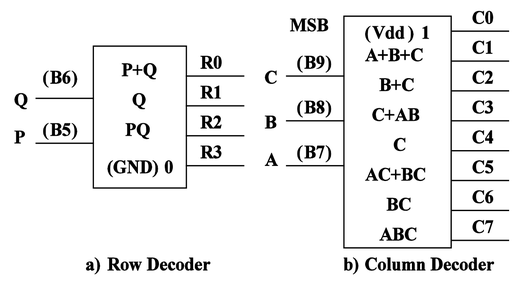
- The spectral performance of the DAC has been improved by designing optimum current sources. The simulation results show almost constant SFDR over the entire Nyquist signal frequency.
- To reduce the correlated noise of the current sources four separate bias sources are used in four different quadrant of the current source matrix.
- The proposed low power DAC consumes only 17.85 mW of power and achieves improved static as well as dynamic performances without adding any additional complex circuits.

Building Blocks

- The design of the CS-DAC includes both analog and digital blocks. The important digital blocks includes input registers, clock drivers, row and column decoders and local decoder matrix, switch driver circuits and retiming giga-latches.
- Important analog blocks includes bandgap current reference circuit, bias current cells, current source array and differential current switch array.

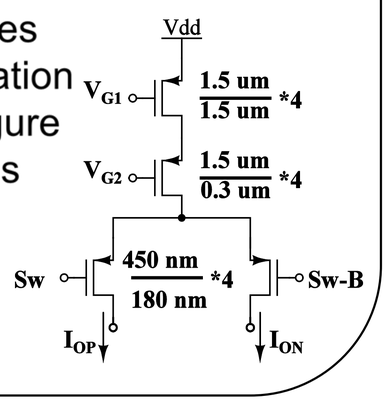
Design Algorithm

- The Row and Column decoders are realized by binary-to-thermometric decoders. The digital logic to implement the decoders are shown in the right hand side figure.



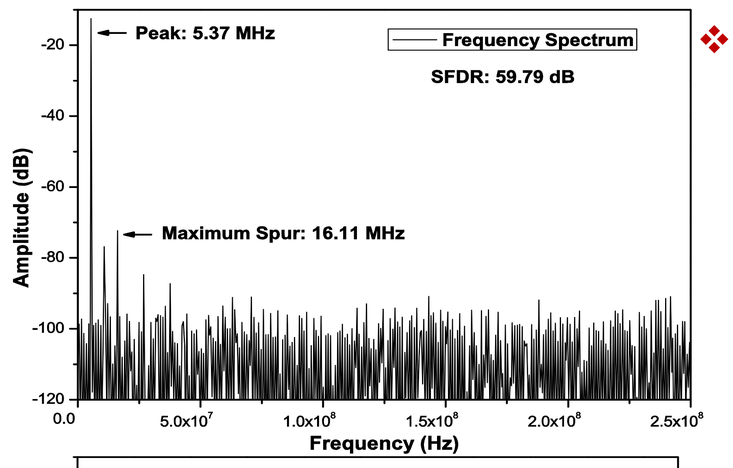
- The optimum size of the unit current sources has been derived following Pelgrom's equation [15] as listed below. The right hand side figure shows the dimension of the current sources for 20 µA current.

$$(W \times L)_{Min} = \frac{\frac{4A_{Vt}^2}{(V_{GS}-V_t)^2} + A_\beta^2}{2\left[\frac{\sigma(I)}{I}\right]^2}$$

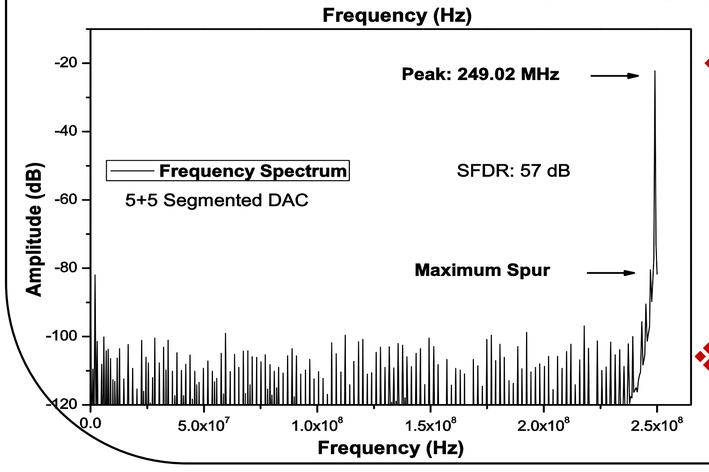


Results

- The simulated differential nonlinearity (DNL) of the10-bit DAC is 0.248 LSB, and the integral nonlinearity (INL) is 0.44 LSB.



- The DAC shows a Spurious Free Dynamic Range (SFDR) of 59.79 dB for 5.37 MHz of input signal sampled at 500 MSPS as shown in the figure left in mismatch environment.



- The DAC shows a Nyquist SFDR of 57 dB at 500 MSPS sampling rate as shown in the left hand side figure in mismatch environment.
- The SFDR variation of the DAC is negligible.

Conclusions

- The proposed work present the design methodology of a 10-bit Segmented Current Steering DAC to achieve high SFDR.
- The achieved SFDR is almost constant throughout the Nyquist signal frequency even at mismatch environment.

Future Work

- To validate the proposed design with tested results.
- The performance of the DAC can be improved further by using additional calibration circuits or dynamic element matching techniques.