Virtual Fabrication of Short-Channel Recessed-Source/Drain (Re-S/D) SOI MOSFETs

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Abstract*—This paper describes process and device simulation results of short-channel Recessed-Source/Drain (Re-S/D) SOI MOSFETs. A Re-S/D SOI MOSFET with 30nm channel length, and 10nm channel thickness, is virtually fabricated with reduced short channel effects (SCEs) and low source/drain series resistance. The processing steps, which are required to obtain the structure of the Re-S/D SOI MOSFET, are proposed and explained in detail. The electrical characteristic I_{ds} versus drain to source voltage V_{DS} is obtained for different values of V_{GS} and Re-S/D thickness (t_{rsd}). The device is virtually fabricated using 2D process simulator ATHENA, followed by electrical characterization which is done with the help of device simulator ATLAS^{TM} from SILVACO.*

Keywords— Short Channel Effects (SCEs); Recessed-Source/Drain (*Re-S/D)* thickness; electrical characteristics.

I. *INTRODUCTION*

Scaling down of MOSFET device in IC Technology offers excellent features such as packaging density and device speed of operation which increase exponentially. Simultaneously, power dissipation decreases exponentially as stated by Moore's law [1-2]. However, leakage current and short channel effects (SCEs) are to be considered when MOSFETs are scaled to the deep submicron region [3]. In order to facilitate MOSFET scaling and to follow the Moore's law, fully depleted(FD) ultra thin body (UTB) SOI MOSFET could be preferred[4]. SOI devices increase the device speed by 20 - 30% and reduces power dissipation to 50% of conventional MOSFETs [5]. Further, the FD SOI MOSFETs offer reduced short-channel effects (SCEs), smaller subthreshold swing, less mobility degradation and high on-to-off current ratio when compared with conventional MOSFET devices. Sapna *et al.* [6]. have virtually fabricated 35nm channel length fully depleted (FD) SOI MOSFET with 6nm thick SOI layer using ATHENA process simulator. The results of the study led to the conclusions that threshold voltage and subthreshold swing decrease with the decrease in SOI layer thickness. However, the on-current driving-capability of the device is limited by a demerit of large series resistance, which is associated with ultra thin body (UTB) of (FD) SOI MOSFETs [7].

Zhang *et al.* [8] fabricated self-aligned recessed-source/drain (Re-S/D) fully depleted (FD) UTB SOI MOSFET. They stated that the series resistance and the miller capacitance got reduced over UTB SOI MOSFETs when the source and drain regions are extended deeper into the buried oxide. Apart from this, slight DIBL effect is also observed. Later on Chang *et al.* [9] successfully fabricated 30nm channel length Re-S/D SOI MOSFET with 5nm thick undoped channel. They demonstrated the reduction in source/drain series resistance by extending heavily doped polysilicon source/drain regions into the buried oxide (BOX) of SOI wafer. It was found that the proposed device exhibited excellent properties in short channel immunities such as drain-induced barrier lowering (DIBL) and sub threshold slope. Svilicic *et al.[*10] have reported theoretical models for the potential distributions, short-channel threshold voltage and subthreshold swing of the Re-S/D UTB SOI MOSFETs.

In our previous work [11-13], we have analyzed the subthreshold characteristics of Re-S/D SOI MOSFETs analytically by presenting analytical subthreshold current and subthreshold swing models. We have observed that the on-current driving-capability of a Re-S/D UTB SOI MOSFETs could be further improved by adopting the dual- metal-gate (DMG) structure instead of conventional single-metal-gate structure. The present paper describes the virtual fabrication of 30nm channel length Re-S/D SOI MOSFET using ATHENA. The main objective of ATHENA process simulator [14] is to create a device structure that is used by the ATLAS device simulator [14] for further electrical characterization of the device. ATHENA provides an appropriate and suitable platform for simulating processes such as oxidation, lithography, physical etching and deposition, diffusion, ion implantation which are used in semiconductor industry. Two-dimensional (2D) process simulator ATHENA offers good features such as - fast and accurate simulation of the device; replacement of costly wafer experiments with simulations; providing advanced simulation environment

II. *VIRTUAL FABRICATION OF THE DEVICE*

Schematics of Fig.1 show the proposed process flow of Re-S/D SOI MOSFET. We consider a symmetrical MOSFET i.e. the regions from the center of the channel to source and center of the channel to the drain are identical to each other. Hence, we use a special facility from ATHENA that half of the structure (region from center of the channel to source) is fabricated first and then the other half structure (region from center of the channel to drain) is generated using the command "structure mirror". The process flow of Re-S/D SOI MOSFET commenced with defining the initial simulation grid. Specifically, the simulation grid represents the points where the model equations are solved. The number of nodes in a grid

has a direct influence on simulation time and accuracy of the device. Therefore, specification of simulation grid plays a crucial role. So, a finer grid should exist only in the critical areas of the device where ion implantation will occur, where junctions will be formed.

P-type <100> SOI wafer with 400nm thick Si substrate, 180nm thick buried oxide (BOX), 20nm thick SOI layer and background doping of 10^{14} cm^{-3} are considered as shown in Fig 1(a). The process of creating Re- S/D above the BOX is as follows: Firstly, SOI layer is etched by using geometrical etching technique and then oxide layer with thickness greater than silicon layer thickness is deposited using conformal deposition technique. After that, etching of oxide is carried out to planar structure as shown in Fig 1(b). Again, conformal deposition technique is used to deposit Si layer of thickness 20nm which is exposed to perform further processing steps as

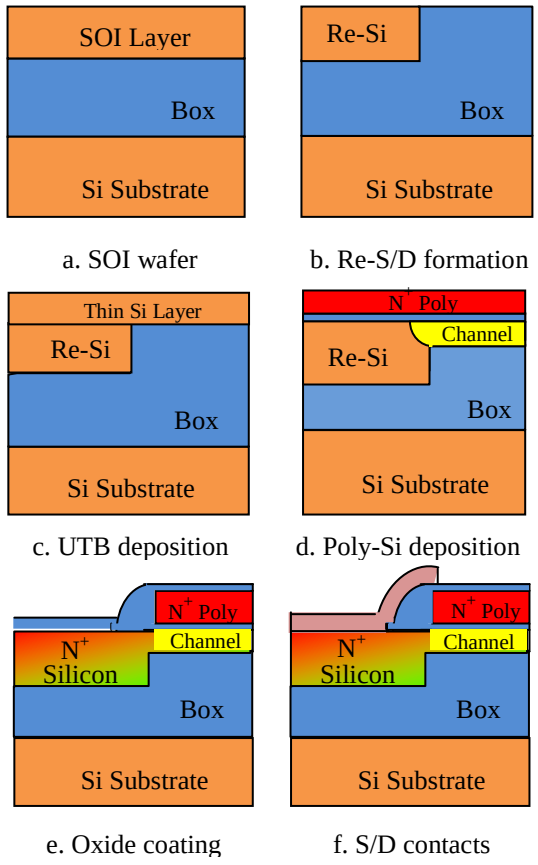

Fig. 1. Schematics showing a process flow for the proposed Re-S/D SOI MOSFET

shown in Fig 1(c). Dry oxidation is performed at 1000^0C for 30 minutes in dry O_2 at 1 atmospheric pressure with the addition of 3% HCl. Following oxide (SiO_2) growth, the oxide is etched back to a precise thickness to facilitate ion implantation that comes in the next step. Subsequently, the top Si layer is thinned to 10nm by thermal oxidation process. Further, Boron ion implantation is carried out at 7KeV of implantation energy with dosage of $3x10^{12}$ cm^{-3} in the channel region.

Furthermore, gate oxide (SiO_2) layer is developed by dry oxidation process which is performed at relatively low temperature of 850^0 C for a small time interval of 3 minutes. Heavily doped poly-silicon which is advantageous in terms of its high conductivity is utilized as gate instead of metal. Poly silicon of thickness 40nm is doped with phosphorus of concentration 10^{18} cm^{-3} and deposited with conformal deposition technique as shown in Fig 1(d). The next process is the development of source/drain (S/D) using two implantations: phosphorous and arsenic. These implantations are followed by some drive-in diffusions, which are performed at 800^0C in nitrogen for 11 minutes. If the voltage levels are not scaled simultaneously with the shrinking size of the device, there may be a rise in the electric field in the channel region resulting in hot electron current, in which electrons approach quickly, scattering into the gate oxide region.

To overcome this problem phosphorous implantation is carried out to create a lightly doped drain (LDD) region, which decreases electron energy gradually as electrons

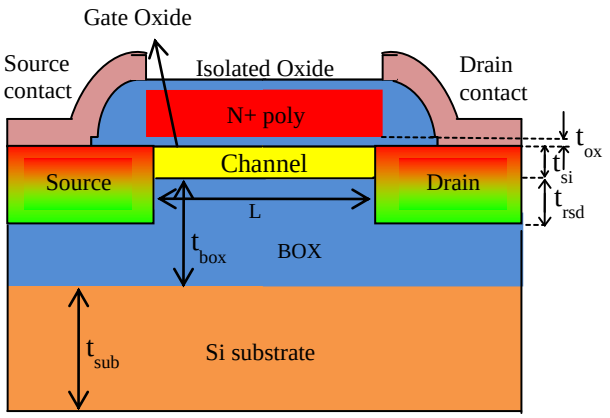

Fig. 2. Schematic showing a structure of Re-S/D SOI MOSFET

approach the drain. Arsenic implantation is carried out with high dosage of $5x10^{14}$ cm^{-3} and the implant energy is 15keV to build the low resistance in the source and drain region as shown in Fig 1(e). For providing electrical contact to the source/drain, Aluminum (Al) is deposited. Later, oxide on the left side of the device is etched for depositing Al of thickness 20nm and the contact is shaped by etching part of the aluminum on the right side as shown in Fig 1(f). This completes the virtual fabrication of half of the device. On mirror imaging the above obtained half structure the full structure of Re-S/D SOI MOSFET is formed. This completes the simulation of other half. Fig. 2 shows the schematic of complete structure of Recessed-S/D SOI MOSFET. The symbols L, t_{Si} ,$t_{ox,}$ t_{box} and t_{rsd} represent the gate length, channel thickness, gate oxide thickness buried oxide (BOX) depth and recessed source/drain (Re-S/D) thickness respectively.

III. *RESULTS AND DISCUSSION*

This section is aimed to discuss the doping and electrical characterization of device using ATLAS device simulator. The structure utilized for the simulation is generated by ATHENA process simulator. Fig. 3 shows the variation of net doping in source, channel and drain regions of 45nm channel length Re-S/D SOI MOSFET. The heavily doped n-type source/drain regions are formed by arsenic implantation with an energy of 20 keV and a dosage of $5x10^{13}$ cm^{-3} . The channel region is doped with boron impurity, with an implant energy of 7 keV and a dosage of $5x10^{13}$ cm-3. The ion beam used for both implantations is tilted by 7^0 and rotated by 30^0. The peak concentration in the source /drain regions and channel regions are observed as $5x10^{19}$ cm-3, $3x10^{18}$ cm-3 respectively.

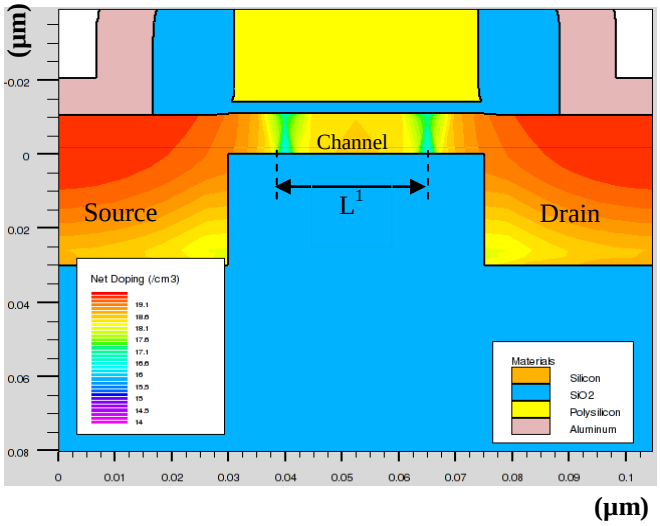

Fig. 3. Schematic diagram of net doping in source, channel and drain regions of a Re-S/D SOI MOSFET

where, tsi=10nm L=45nm L1=30nm tox=3.2nm tbox=200nm trsd=20nm

Fig. 4 shows the acceptor and donor doping profile along the cutline taken from source to drain region. The effective channel length (L1) of the device becomes 30nm due to lateral penetration of source/drain implantation

Fig. 5 shows drain current (I_{ds}) plot with respect to drain to source voltage (V_{DS}) for different gate to source voltages (V_{GS}) considering a step of 0.4V. The drain current (I_{ds}) is found to be increased with drain to source voltage (V_{DS}).

Fig. 6 shows the effect of recessed source/drain thickness (t_{rsd}) on drain current (I_{ds}) by keeping all other device parameters constant. It also depicts the I_{ds}-V_{DS} characteristics of Re-S/D SOI MOSFET where t_{rsd} varies from 0 to 30nm with step size of 10nm; when t_{rsd}=0nm, the device simply replicates conventional SOI MOSFET. From this figure it is observed that the on-current driving capability of the device increases with recessed-S/D thickness (t_{rsd}).

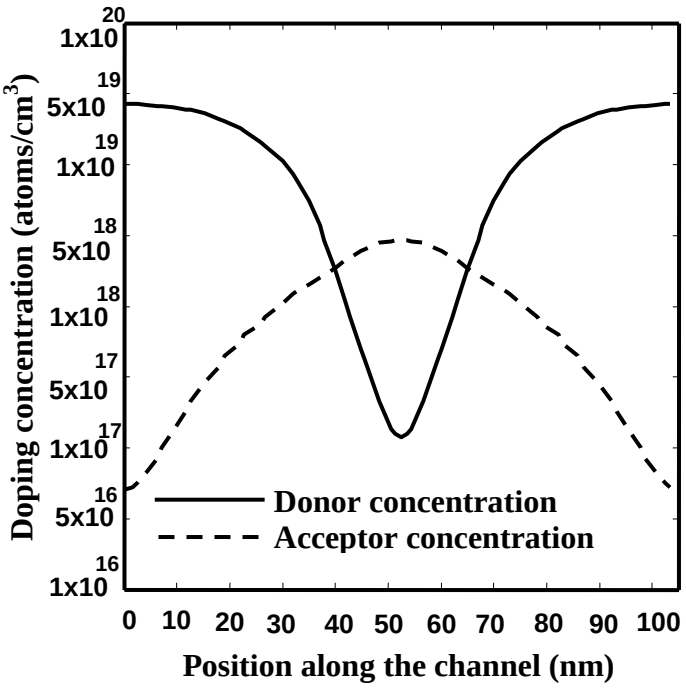

Fig. 4 Acceptor and donor doping profile along the cutline

where, tsi=10nm L=45nm L1=30nm tox=3.2nm tbox=200nm trsd=20nm

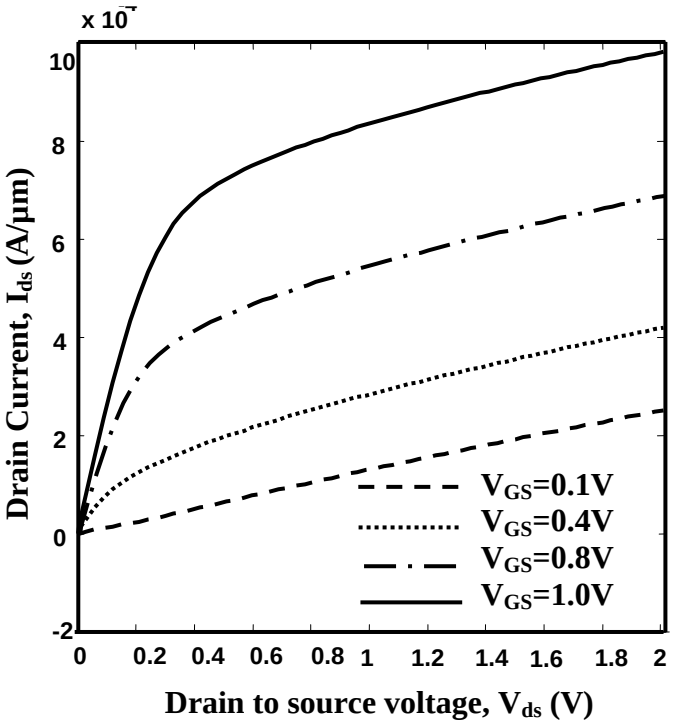

Fig. 5. Drain current versus Drain to source voltage for different Gate to source values.

where, t_{si}=10nm L=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm

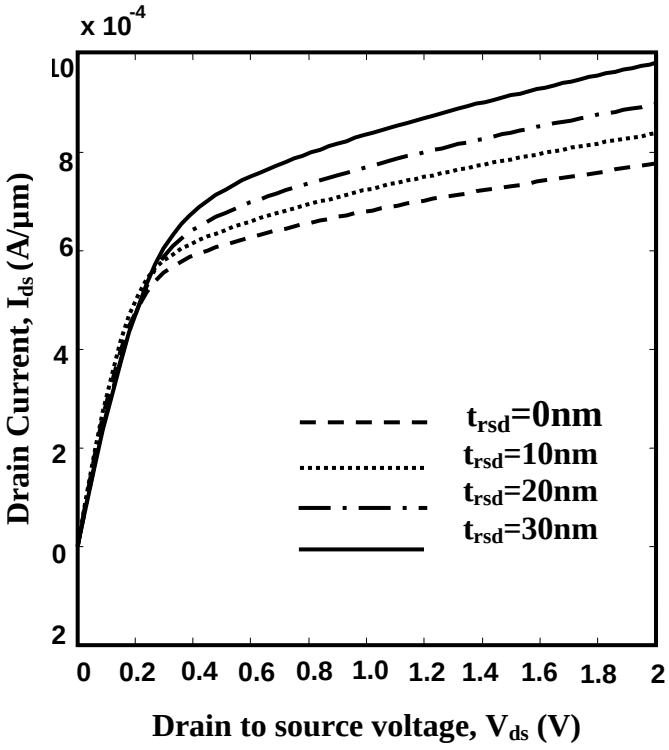

Fig. 6 Drain current versus Drain to source voltage for Recessed source/drain thickness values.

where, t_{si}=10nm L=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm V_{GS}=1V

IV. CONCLUSIONS

In this paper, the virtual fabrication of a recessed-S/D SOI MOSFET with channel length of 30nm has been done. Several processing steps such as oxidation, deposition, etching, ion implantation and lithography have been utilized in the process of device fabrication. Gate oxide thickness (t_{ox}) which is 3.2nm is extracted by process parameter extraction. The thickness of the Re-S/D (t_{rsd}) is controlled by SOI layer thickness. The electrical characteristics such as drain current (I_{ds}) versus drain to source voltage (V_{DS}) have been explored for different values of gate to source voltage (V_{GS}). Also variation of drain current (I_{ds}) with the drain to source (V_{DS}) voltage for different values of recessed S/D thickness (t_{rsd}) have been evaluated. The drain current (I_{ds}) of the device increased with increasing source/drain penetration in buried oxide(BOX).

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