Rapid Prototyping of FPGA Based Digital Controller of DSTATCOM for Load Compensation Under Distorted Utility Condition

Gokulananda Sahu,Venkata Ratnam Kolluru and Kamalakanta Mahapatra
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela, India
gokulanandasahu@gmail.com ,venkataratnamk@gmail.com and kmaha2@gmail.com

Abstract— **This paper presents rapid prototyping of FPGA based digital controller for Distribution STATic COMpensator (DSTATCOM) using Matlab/Simulink and System Generator. The MATLAB/Simulink models are optimized and converted to target-specific synthesized VHDL code for FPGA implementation. Simulation, co-simulation, system level design and verification for rapid prototyping of FPGA-based digital controller are necessary to develop prototype in a relatively short time span by avoiding time-consuming manual coding. This enables increased productivity and facilitates the development of digital controller with more complex control algorithms. This prototype controller is developed and implemented on evaluation boardXUPV5 with Virtex-5 xc5vlx110t chip. This design is verified with System Generator co-simulation platform and found total harmonic distortion of load compensation well within the allowable range of IEEE standards with unit power factor achievement.**

Keywords—Field programmable gate Array;Distribution Static Compensator;Rapid prototyping.

I. INTRODUCTION

During the last decade, there has been sudden increase in the nonlinear load (Computers, Laser printers, SMPS, Rectifier, Cyclo-converters etc.), which degrades the power quality causing a number of disturbances e.g. heating of home appliances, noise etc., in power systems [1][2] due to flow of harmonic current. The utility is also distorted due to flow of this harmonic current through line impedance. The main objective of Load compensation is harmonic elimination, load balancing and power factor correction. The DSTATCOM has proved to be a useful custom power device to eliminate harmonic components and compensate reactive power for balanced/unbalanced linear/nonlinear loads [3]. The performance of DSTATCOM largely depends on the control strategies used for reference current extraction. The author has already proposed control strategy [4] is best suitable for distorted utility condition based on instantaneous symmetrical components and active power which is implemented as all-on-chip controller on FPGA in this work.

The design of advanced power electronic circuits and systems requires knowledge from multiple discipline areas, including digital control, to develop new and custom designed products and providing solutions within short time span [5].Manual coding is tedious, time consuming and error prone. On the other hand, automatic code generation is more helpful to designers to make changes in the system level model and update HDL in short time by regenerating the HDL code. In addition, MATLAB model-based design facilitates creation of FPGA-based prototypes and automates HDL code verification by co-simulating it with Simulink and optimizes the models to meet speed-area-power objectives for the FPGA. Moreover, FPGA technology is now considered very useful in myriad fields of application due to quick implementation, confidentiality of the algorithm and architecture, capable to meet many constraints for crucial applications, and it can be adapted to any change in design by dynamic reconfiguration. It is more beneficial of using FPGA for controlling of power systems compared to counterpart DSPs and microcontrollers [6][7]. In fact, FPGA-based digital controllers have been implemented with success in many different applications, such as VSC based DSTATCOM[8][9], pulse width-modulated (PWM) inverters [10-11].

In this paper performance of proposed control strategy is investigated in **three phase three wire system** for balanced/distorted source and non-linear balanced /unbalanced Load for mitigation of harmonics and compensation of reactive power with FPGA based digital controller which is the **problem statement** for this work**.** The measures of the performance is the source current total harmonic distortion

Rest of the paper is organized as follows. In section-II system Design and in section-III brief discussion on proposed controller is presented. In section-IV FPGA implementation is presented and in section-V the performance indices used for evaluation are discussed. Simulation results are described in section-VI. Finally in section-VII, conclusion is drawn.

II. SYSTEM DESIGN

Fig.1 shows the basic block diagram of a DSTATCOM system with linear & non-linear load connected to three phase

three wire distribution system. A nonlinear load is realized by using a three phase full bridge diode rectifier whereas linear load is realized by R-L network. A three phase voltage source converter (VSC) working as a DSTATCOM is realized using six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes. At ac side, the interfacing inductors are used to filter high frequency components of compensating currents. Opto-Isolator is required to isolate power ground from logic ground.

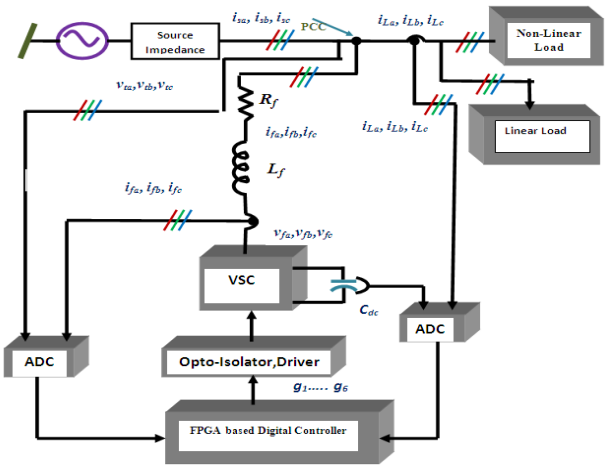

Fig.1 System design of DSTATCOM

III. PROPOSED DIGITAL CONTROLLER

This control strategy is based on instantaneous symmetrical component theory in instantaneous state. The main objective to find out active fundamental source peak current. The reference compensating current is equal to the difference between estimated source and load current.Fig.2 shows the control structure of proposed controller. The peak source current is estimated as

$$I_{sm1} = \frac{p_{3\phi}}{3V_m^+} \tag{1}$$

Prime objective is to make source current balanced.

$$i_a + i_b + i_c = 0 \tag{2}$$

Let formulate all powers in time domain. Zero sequence, positive sequence and Negative sequence complex power are denoted as s0, s+ and s- . The real power of zero sequence ,positive sequence and Negative sequence are denoted as p0,p+ and p-. The Imaginary power of zero sequence, positive sequence and Negative sequence are denoted as q0,q+ and q-.The instantaneous voltage and current of zero sequence ,positive sequence and Negative sequence are denoted as v0,v+ ,v- and i0,i+,i- respectively. Let zero sequence power is formulated as

$$\left.\begin{aligned} s_0 &= 3v_0 i_0^* = p_o + jq_0 \\ p_0 &= \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c) \\ q_0 &= 0 \end{aligned}\right\} \tag{3}$$

Let calculate the positive sequence power.

$$\left.\begin{aligned} s_+ &= 3v_+ i_+^* = p_+ + jq_+ \\ p_+ &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c)\right] \\ q_+ &= -\frac{1}{2\sqrt{3}}\left[v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b)\right] \end{aligned}\right\} \tag{4}$$

Let calculate the negative sequence power.

$$\left.\begin{aligned} s_- &= 3v_- i_-^* = p_- + jq_- \\ p_- &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c)\right] \\ q_- &= \frac{1}{2\sqrt{3}}\left[v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b)\right] \end{aligned}\right\} \tag{5}$$

Where total Instantaneous active power is defined as

$$s = (s_0 + s_+ + s_-) = (p_0 + p_+ + p_-) = p_{3\phi} = (v_a i_a + v_b i_b + v_c i_c) \tag{6}$$

In equation (4) putting $i_a+i_b+i_c=0$, We get

$$\frac{p_{3\phi}}{2} = p_+ = \frac{3V_{m1}^+}{\sqrt{2}}\frac{I_{sm1}}{\sqrt{2}} \tag{7}$$

$$I_{sm1} = I_{sm} = \frac{p_{3\phi}}{3V_{m1}^+} \tag{8}$$

So

$$\left.\begin{aligned} i_{sk}^* &= i_{skref} = I_{sm} U_{k1} \\ i_{fk}^* &= i_{fkref} = i_{Lk} - i_{skref} \end{aligned}\right\} \tag{9}$$

Where k=a, b, c and Uk1 is fundamental unit vector template.

Fig.2 shows the basic control structure of proposed controller which constitutes one PI controller, low pass filters (3xLPF1 and 1xLPF2) and arithmetic calculators. The average power plav is calculated by adding PI output (Ploss) to LPF2 output. LPF1 is used to extract the fundamental from distorted PCC (point of common coupling) voltage. Phase comp. network is used to compensate of filtered PCC terminal voltages. Hysteresis Current Controller (HCC) is used to generate gate pulses g_1-g_6 for VSC by comparing reference with actual compensating currents.

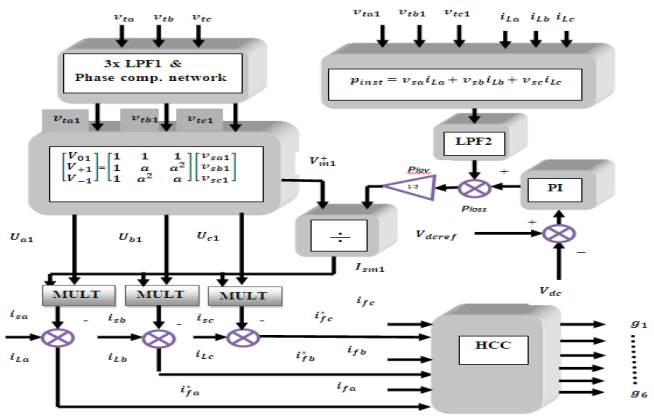

Fig.2 Control structure of proposed controller

IV. FPGA IMPLEMENTATION

A. Model based design

Fig.3 shows the model based design of FPGA based digital controller by using Xilinx fixed point block sets. This controller is designed for 3Volt to work properly in FPGA board. Sensor signals are processed through signal conditioning circuits made available within 0-3V range. The performance of the design is optimized by proper adjusting the bit precision. This model constitutes major blocks like +sequence calculator, pinst calculator for calculation of instantaneous active power, pI controller, unit vector and reference current block, HCCfpga for hysteresis current control and filters

B. Verification

1) HDL co-simulation: The System Generator generates VHDL and Verilog net-list using compilation and generate wizard for HDL simulator e.g. ISE, Cadence Incisive, Mentor Graphics ModelSim and Questa for rapid verification of generated HDL code. This streamlines the verification process and helps to fix the error bugs before hardware implementation.

2) Hardware co-simulation: It tests the design in real hardware for the generated HDL code. The programming file is loaded onto an FPGA with JTAG connection. TX/RX of data from Simulink to FPGA is via gigabit Ethernet crossover cable that co-simulate and verifies the design in real time environment. It helps to detect, isolate, identify and resolve bugs in the early stages of design process.

C. FPGA programming

The generated VHDL code is bit-true, cycle-accurate and synthesizable VHDL code which is free from bugs. System Generator offers integration with Xilinx ISE design suite that makes it easy to implement algorithm in MATLAB and Simulink to target Xilinx FPGAs. Xilinx ISE compiles and generates the bit stream file which is then loaded into the FPGA using JTAG via the USB connection by iMPACT software. Fig.6 shows the Xilinx ISE10.1 compilation report of resources utilization for digital controller implementation in Virtex-5 xc5vlx110t chip.

V. PERFORMANCE INDICES

A. Total harmonic distortion

The total harmonic distortion (THD) [12] is used to define the effect of harmonics on the power system voltage. It is used in low-voltage, medium-voltage, and high-voltage systems. It is expressed as a percent of the fundamental and is defined as

$$THD(voltage) = \frac{\sqrt{\sum_{h=2}^{50} V_h^2}}{V_1} * 100\% \quad (10)$$

$$THD(current) = \frac{\sqrt{\sum_{h=2}^{50} I_h^2}}{I_1} * 100\% \quad (11)$$

According to IEEE-519 the permissible limit for distortion in the signal is 5%.

VI. RESULTS AND DISCUSSION

To investigate the performance of the DSTATCOM for proposed control strategy, simulations are performed on matlab/simulink platform. A three phase three wire distribution system with parameters given below is considered for simulation.

A. System Parameters:

Supply voltage: 50Vrms (L-N), 50Hz, three phase balanced
Source impedance: Rs=1Ω, Ls=5mH
Nonlinear load: Three phase full bridge diode rectifier with load (L_L=10mH,R_L=10Ω)
DC storage Capacitor Cdc=2000μF
Interface inductor L_f=0.5mH , R_f=0.1Ω
DC Link voltage V_{dc}=100V
Hysteresis band=0.25A
Unbalanced Linear load: Z_a=67+j31.42Ω , Z_b=37+j18.55Ω, Z_c=28.5+j12.56Ω
PI regulator parameters: K_{pr}=0.0303,K_{ir}=6.8788
Low pass butter-worth filter LPF1and LPF2:Cut-off frequency fc1=25Hz, fc2=100Hz,Sampling frequency fs=20kHz,Order-4th(2xsecond ordersection), Structure: Direct form-II.

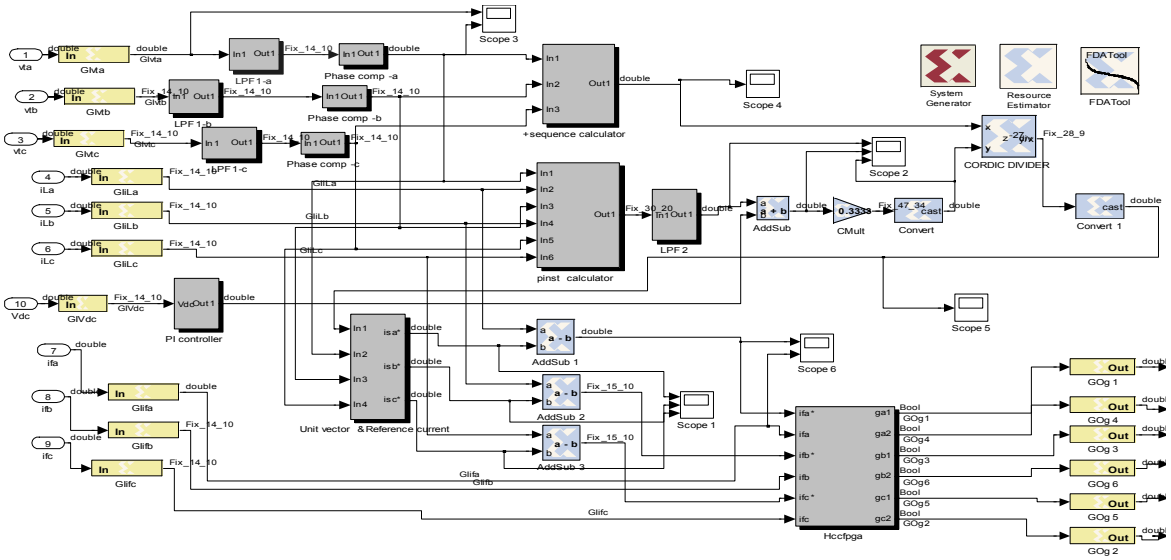

Fig.3 FPGA based digital controller

The performance of the proposed control strategy is evaluated based on balanced distorted Source and Unbalanced Non-linear load. The THD comparative analysis of the source current for all phases after and before compensation is summarized in Table1.THD% of distorted PCC voltages **are 18.50,17.16** and **17.41** for phase a,b and c respectively.

Proposed control strategy simulation

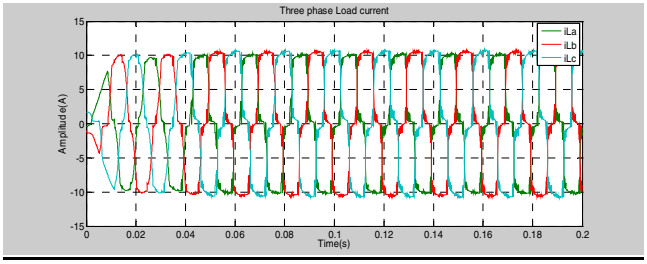

Fig.4a Three phase unbalanced Load current

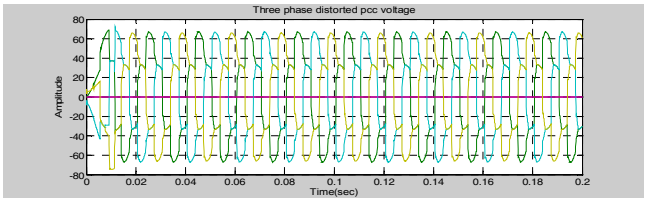

Fig.4b Three phase distorted pcc voltage

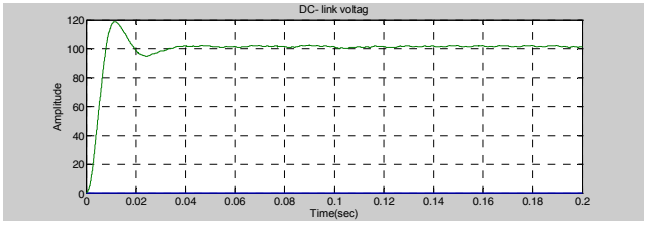

Fig.4c DC link voltage

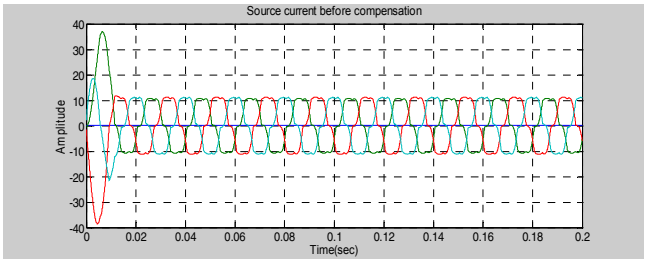

Fig.4d Three phase Source current before compensation

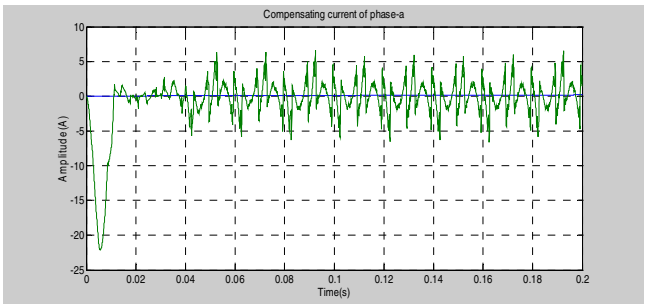

Fig.4e Compensating current of phase-a

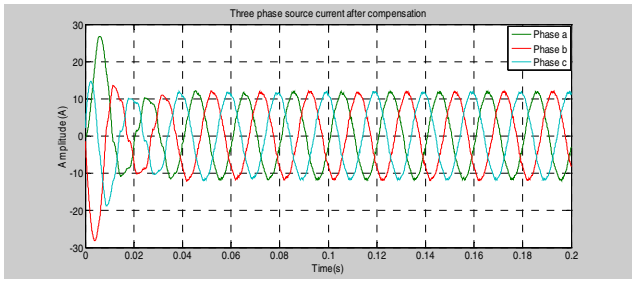

Fig.4f Three phase Source current after compensation,

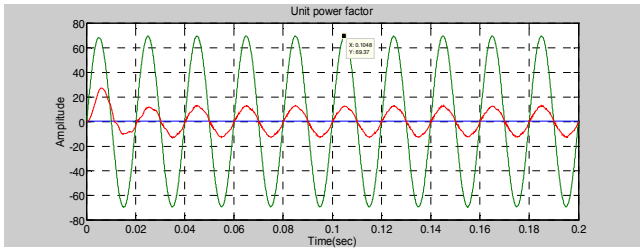

Fig.4g Unit power factor of compensated load

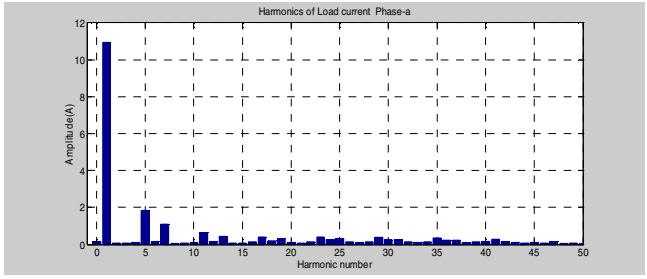

Fig.4h Harmonics of Source current before compensation

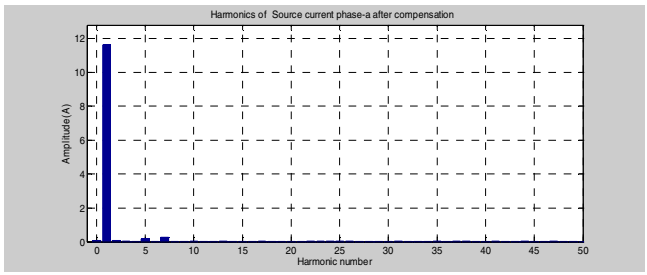

Fig.4i Harmonics of Source current after compensation

Fig.4 (a, b, c, d, e, f, g, h, i) shows the dynamic performance of the system

Table 1 Comparative Analysis of THD

Implementation	**THD(%) of Source Current with unbalanced non-linear load**					
	Before Compensation			**After Compensation**		
	a	***b***	***c***	***a***	***b***	***c***
M K Mishra et al [7](DSP)	15.5	10.5	8.5	5.2	4.8	4.7
Proposed (FPGA)	23.66	22.34	22.25	3.33	3.43	3.37

B. *Simulation of FPGA based Digital Controller*

Fig.5(a and b)show the RTL schematic and VHDL Test bench of Top module respectively. Signals prefixed with GI and GO are known as Gateway input and Gateway output signals of FPGA based controller respectively.Fig.5c shows all six gate pulses are generated from Top module in full zoom. From the test it has been found that DC link voltage Vdc remains constant to achieve proper compensation.

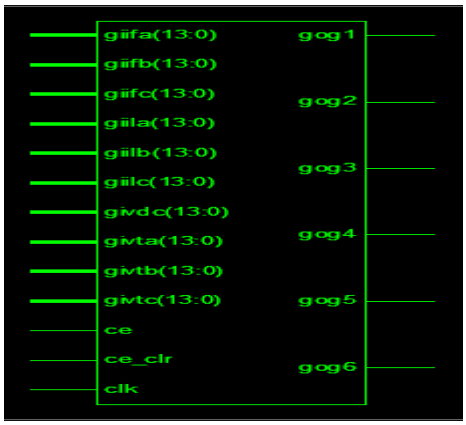

Fig.5a RTL Schematic of Top module

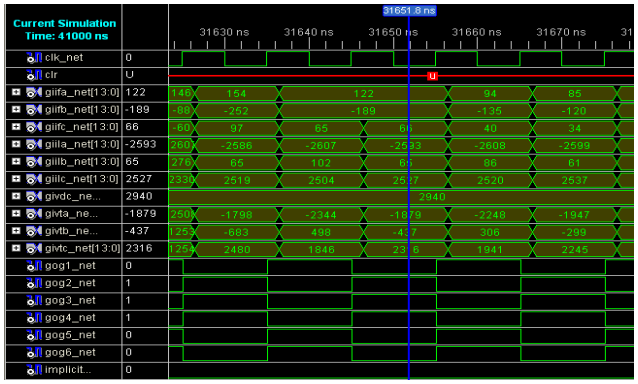

Fig.5b VHDL Test bench of Top module

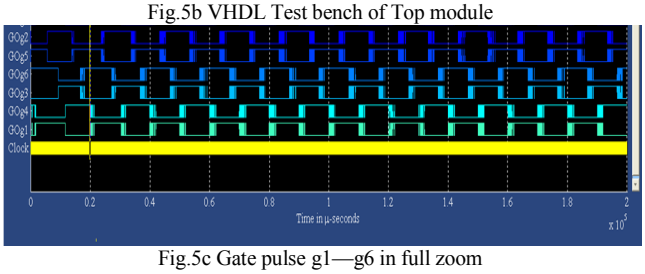

Fig.5c Gate pulse g1—g6 in full zoom

C. *Implementation Result*

The design is implemented in VHDL using ISE10.1 tool from Xilinx. Fig.6 shows the resource utilization indicates the area consumed in FPGA.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	4817	69120	6%
Number of Slice LUTs	13660	69120	19%
Number of fully used LUT-FF pairs	3589	14888	24%
Number of bonded IOBs	148	640	23%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48Es	22	64	34%

Fig.6 Device utilization summary

VII. CONCLUSION

This method has been described to facilitate the development and implementation of FPGA-based digital controller for DSTATCOM which is faster and provides a greater degree of confidence than traditional manual VHDL coding. After verification in System Generator platform it is implemented on a Xilinx Virtex-XUPV5 board successfully. Verified FPGA based digital controller resulted in 3.33, 3.43and3.37 % of total harmonic distortion for phase a,b and c respectively, well within the allowable range of IEEE standards and has improved compensation as compared to the previous implementation.

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