Non-linear Sliding mode Control with SRF based Method of UPQC for Power Quality Enhancement

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***Abstract*— This paper proposed a method of non-linear sliding(NLS) surface based control strategy for controlling the dc link voltage of unified power quality conditioner (UPQC) to compensate the current harmonics, sag/swell and voltage unbalance. The proposed non-linear sliding surface depends on controlling the DC-link capacitor voltage so that the damping ratio of the system changes from its initial low value to its final high value. The proposed algorithm allows the dc-link capacitor voltage of UPQC to obtained low overshoot and small settling time, hence better compensation can be achieved. This paper also proposed the Novel synchronous-reference frame (SRF) control technique for the reference current and voltage generation for both converters. Results have been validated using the real-time performance analysis in Opal-RT Lab. A comparison has been made with the conventional PI-controller and adequate results are considered for the verification.**

Keywords—Nonlinear sliding surface; Sag/swell; Overshoot; Settling time;SRF;Opal-RT

I. INTRODUCTION

In recent year, problem caused by power quality have great adverse economical impact on the utilities and customers due to extensive use of power electronics devices cause increasing the harmonic pollution [1].On the other side, a stable power supply has been desired for proper operation of sophisticated equipment that used in many industries and house hold purpose. Development of PWM converters has significantly mitigated the power quality (PQ) problems by the use of both shunt and series active power filter. The shunt active power filter can compensate the problem associated with current harmonics and poor power factor [2],whereas series active power filter can compensate the problem lies in supply voltage. Connection of both converters back-to-back with common DC-link capacitor and deals with both supply voltage and load current imperfections is implied as unified power quality conditioner(UPQC) [3].

The dc-link voltage of the UPQC can significantly deviate from the reference throughout a transient occasion, brought on by load connection/disconnection or/and supply side voltage sag/swell. The performance of UPQC principally relies on how rapidly and accurately reference signals are derived, a suitable DC-link voltage regulation is required for deriving the actual reference signals. In the UPQC, the shunt active power filter is generally accountable for this voltage regulation. Within the steady state, the normal dc-link voltage is maintained at a certain preset level, but throughout the transient state preset level deviates from the original value [4].Numerous methods were proposed for controlling the dc-link voltage of UPQC, like the PI, PID and fuzzy controllers have been used in [5] .These controllers fail to satisfy to the system need a fast transient response, robustness and minimum power dissipation. To improve the performance of the system the sliding mode control algorithms with time varying switching surface is proposed by many researchers in [6]- [7].These types of solutions can be used for second and higher order systems. To ensure high performance, system should settle quickly with a low overshoot.

The rapid detection of the disturbance signal with high accuracy and fast processing of the signal is the important aspect of controller based on which a power conditioner performs. The UPQC control strategy actuates the reference signals for both current and voltage and therefore determines the switching pattern of inverter switches, such that it can achieve the desired performance. performance of the power quality .The rapid detection of the disturbance signal with high accuracy and fast processing of the signal is the important aspect of controller based on which a power conditioner performs. Several control methods, algorithms and techniques are available in the literature those are easily applied to UPQC system. Other advanced control techniques have also been reported, such as state feedback controller, model predictive control, model reference adaptive controller[8], self tuning controller , sliding mode control and neural networks [9].As sliding mode controller has its natural way to control time-varying topologies, it has been widely used in power converter. The SMC is one of the robust control schemes based on the concept of changing the structure of the controller in response to the changing state of the system in order to obtain a desired response [10].

Hence, to ensure the high performance of UPQC system, this paper has proposed non-linear sliding(NLS) mode controller for controlling the dc-link voltage of UPQC instead of the traditional PI controller. The nonlinear surface changes system’s closed loop damping ratio as the output approaches the set point. At first, the nonlinear surface maintains the damping ratio to a low value to guarantee fast response and as the output approaches the set point, the system is made exceedingly damped to avoid overshoot. The nonlinear surface constantly changes the damping ratio of the system from its initial low value towards the ultimate high value. For simplicity in the synthesis of nonlinear surface, linear matrix inequalities (LMI) based algorithm is proposed for ease tuning of the parameters associated with the nonlinear surface. A new synchronous reference frame(SRF) based control strategy is used for quickly extracting the reference signal. The performance of UPQC is investigated with the assistance of real-time performance analysis in Opal-RT Lab, which affirmed the validity of the proposed control method. A comparison has been made between proposed strategy and conventional PI controller.

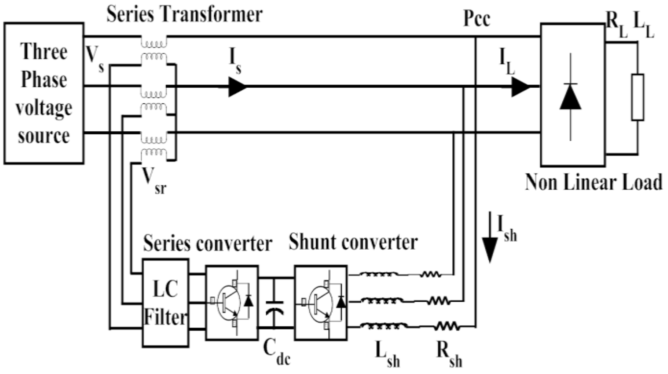


Fig.1. General block diagram representation of UPQC

II. SYSTEM DESCRIPTION

The fundamental reason of a UPQC is to compensate the load current power quality problems, such as harmonics, reactive current, unbalance and neutral current and for supply voltage power quality issues, such as sag, swell, flicker, unbalance and harmonics. Fig.1shows the block diagram representation of UPQC. It comprises of the incorporation of two converters connected back to back to a common dc-link bus. One converter is connected across the load which behaves as a shunt converter and the other, connected in series with the line behaves as series converter.

Shunt coupled inductor 1is utilized to interface the shunt converter to the system network. It additionally helps in smoothing, the current wave shape. Sometimes an isolation transformer is employed to electrically isolate the converter in the system network [10]. The LC filter that serves as a passive low-pass filter (LPF) and serves to dispense high-frequency switching ripples, that is present on converter output voltage. Series injection transformer, which is utilized to connect the series converter and power network. An appropriate turn ratio is regularly considered to reduce the current and voltage rating in the series converter. The shunt converter of UPQC plays a crucial role in achieving required performance by keeping up the dc-link voltage at a set reference value. Also the series converter of UPQC is controlled in a voltage control mode such that it generates a voltage, which is injected in series with line to accomplish a sinusoidal, free from distortion and at the specified magnitude voltage on the load terminal.

III. PROPOSED SRF-BASED CONTROL STRATEGY

The control structure of proposed nonlinear sliding with SRF-based system is depicted in fig.4. Here SRF-based control method is used for generation of reference signal for both shunt and series converter .The SRF control method is one of the best methods among the several control methods presented in the literature [11]-[14],because this method provides excellent characteristics.

Here membership functions are selected as symmetrical membership functions and the two inputs i.e. v_{dc-err} and Δv_{dc-err} are converted into each seven membership functions, five triangular and two trapezoidal membership functions as shown in Fig.5.That makes 49 rules based table . The rule base stores the linguistic variables for rule evaluation for producing the set of modified control output of linguistic variables. Membership functions and rules based are obtained by understanding the system behavior based on this. Defuzzification is designed by considering seven triangular membership functions as shown in Fig.6.The centroid method is used for its defuzzification process to get the crisp output because this method is simple and it provides high accuracy in defuzzification process. The output of the fuzzy controller estimates the magnitude of peak reference current $I_{\max}$. Control structure for series active power filter for designing trajectory of SMC is shown in Fig.7. The proposed control strategy is used to maintain the desired load voltage under specific level for compensation of both symmetric and asymmetric sag/swell on the load side. For series converter, the reference voltage generation can be used for solving the voltage power quality (PQ) problems related with sag, swell, voltage harmonics and unbalanced voltage.

The capacitor voltage control of the proposed method is obtained from FLC, that determines the maximum value of the source current for stabilizing the capacitor voltage .In this case v_{dc-err} is obtained from the difference of capacitor set value

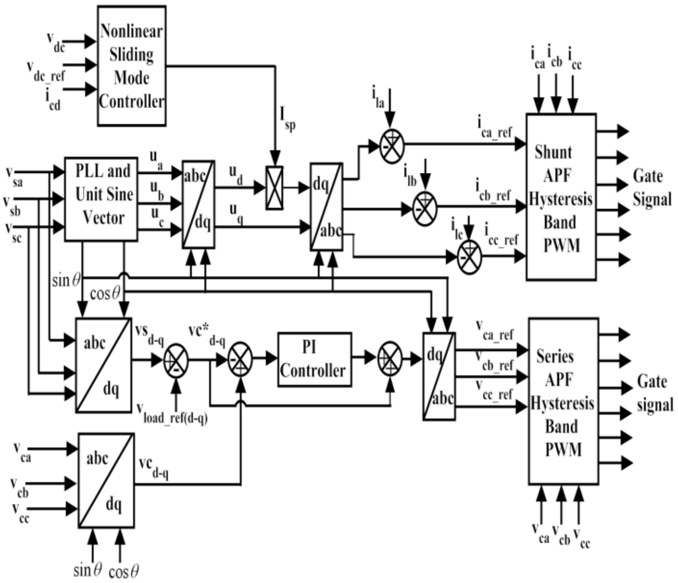


Fig.4 Proposed SRF-based control strategy for UPQC

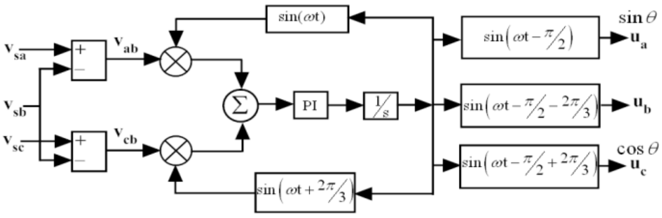


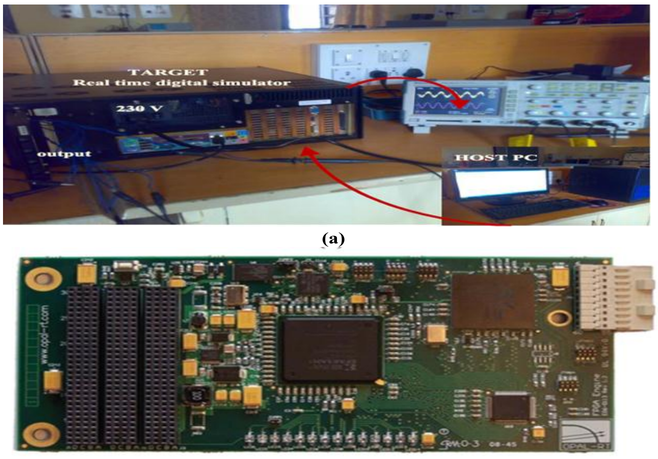
Fig.5 PLL circuit block diagram

p_{l1}^{+} is the positive sequence active power consumed by the load and p_{s1}^{+} is the positive sequence active power supplied by the source. The fundamental source currents are input to the positive sequence component detector that includes a phase-locked-loop function, where the positive sequence fundamental currents are determined by (18). The positive sequence active power, the output of the low pass filter is fed to the divider block and the output of the divider block gives rise to reference voltage V_{kref} after multiplication with unity vector generated from the positive sequence calculator block.However, it doesn't consider the voltage drop across the injection transformer and LC filter. Therefore closed loop voltage compensation vc_{d-q} is added to minimize the losses by passing the difference between the injected compensating voltage vc_{d-q}^{*} and measured compensating voltage vc_{d-q}. The error is passed through the PI controller to find out the amount of losses in injection transformer and LC filter. The losses are added to the injected compensating voltage vc_{d-q}^{*} and are getting inverse transformed to produce reference compensating voltages vc_{ref}.

The produced compensated reference voltage vc_{abc_ref} and measured compensating voltages vc_{abc} are compared in a hysteresis band voltage controller for producing IGBT switching pulses and to compensate all voltage related problems.

IV. OPAL-RT RESULT ANALYSIS

The Opal-RT Lab could be very fast, flexible and scalable real-time simulators. The diagram of Opal-RT Lab simulator set up is shown in fig.6a.The OP5142 (fig.6b) is one of the key building blocks within the standard OP5000 I/O system from opal-RT technologies. The Xilinx Spartan-3 FPGA technologies and high-speed, high-density digital I/O models are incorporated with this real-time simulator. The OP5142 can be attached to the back plane of an I/O module of either a Wanda 3U or Wanda 4U based Opal-RT simulation system. It communicates with the target PC through a PCI-Express ultra-low-latency real-time bus interface. The real-time digital simulator of Fig.6(a) was developed with the aim of meeting the transient simulation needs of the power systems. Real-time implementation of UPQC model shown in Fig.6(a) is comprised of host computers, target real-time simulator and an oscilloscope. The Simulink model compilation with RT-LAB and user interface is done in the host computer. In target real-real system, I/O and model execution process is done and results are displayed in CRO. Table I shows the system parameter used in the Opal-RT LAB.



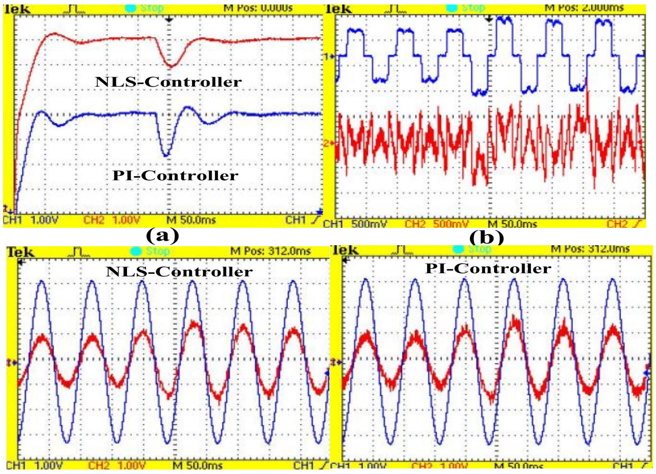
(a)

(b)

Fig.6 RTDS Hardware

TABLE I. Value of system parameter

System parameter	Notation	Value
Supply voltage and frequency	(v_s, f)	(360V p-p),50Hz)
Source impedance	(L_s, R_s)	(1mΩ,10μH)
Three phase non-linear load	(R_L, L_L)	(10Ω,1mH & 20Ω,200mH)
DC-link capacitance	(C_{dc})	6000μF
Reference dc-link voltage	(V_{dc_ref})	700V
Interface Inductor & Resistor for shunt inverter	(L_{sh}, R_{sh})	(0.1Ω .2.3mH)
AC filter inductor & capacitor for series inverter	(L_{sf}, C_{sf})	(6mH,20μF)
Injection Transformer	(IT_x)	500:100,6kVA
PI parameter for series inverter	(Kp, Ki)	(0.1,1.1)
Constant coefficient	(c_3, c_4)	(0.43,0.35)
Positive constant value	$\bar{\alpha}$	200



(a)

(b)

(c)

(d)

Fig.7 Waveform of extracted (a) dc-link voltage (b)load and compensation current of phase-a (scale:20A/div for channel 1 and 10A/div for channel 2)(c) source voltage and current of phase-a NLS--Controller(scale:120V/div for channel 1 and 20A/div for channel 2)(d)Source voltage and current of phase-a PI-Controller(scale:120v/div for channel 1and 20A/div for channel 2)

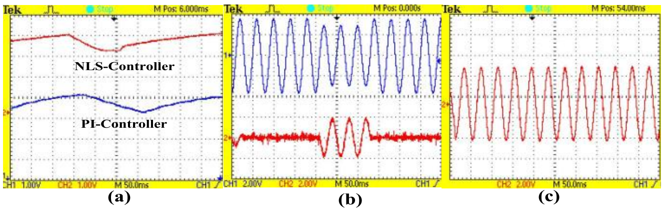


Fig.8 Waveform of extracted (a) dc-link voltage under sag condition (b)source and compensation voltage under phase-a sag condition (scale:95V/div for channel 1 and 20V/div for channel 2)(c) load voltage under phase-a sag condition(scale:95V/div)

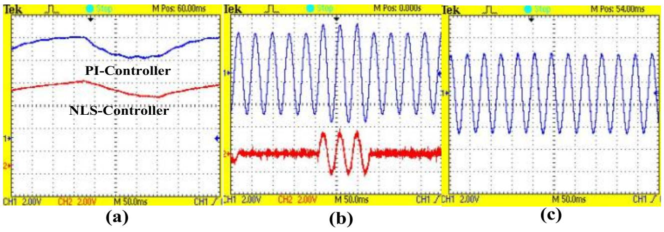


Fig.9 Waveform of extracted (a) dc-link voltage under swell condition (b)source and compensation voltage under phase-a swell condition (scale:95V/div for channel 1 and 20V/div for channel 2)(c) load voltage under phase-a swell condition(scale:95V/div)

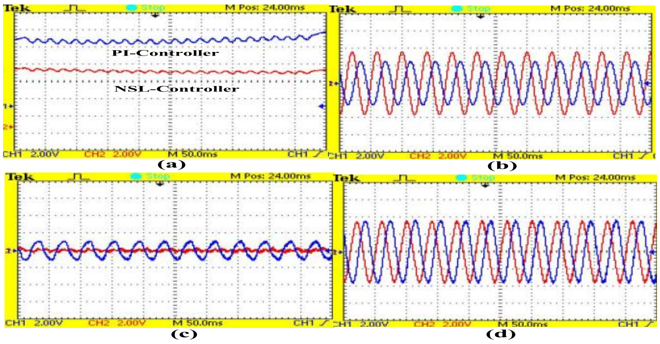


Fig.10 Waveform of extracted (a) dc-link voltage under unbalance condition (b)source voltage under phase-(a & b) unbalance condition (scale:95V/div) (c)compensation voltage under unbalance condition(scale:20V/div for channel 1 and 2)(c) load voltage under phase-(a & b) unbalance condition(scale:95V/div)

The real-time digital verification for harmonic compensation are depicted in Fig.7.The experimentation has been carried out at a switching frequency of 10kHz.The non-linear load generates harmonics and UPQC capable of compensating successfully by injecting non-sinusoidal harmonics at the point of common coupling.

Fig.7(a) provides information about the dc-link voltage of both PI-controller and proposed NLS-controller. The over-shoot and settling time is less in the dc-link voltage of the proposed NLS-controller as compared to PI-controller (when step change of load during the t=0.23s). Fig.7(b) provides the details of load current and compensating current for phase-a under the above transient condition.Fig.7(c) and (d) shows the waveform of phase-a source voltage (v_{sa}) and source current (i_{sa}) for the proposed NLS and PI-controller. It is shown that the phase-a source current becomes sinusoidal, undistorted and in phase with the source voltage.Fig.8 (a) shows the dc-link capacitor voltage of both NLS and PI controller under voltage sag condition, it is observed that both over-shoot and settling time is less in case of proposed technique in comparison to the PI-controller. Fig.8(b) shows the waveform of phase-a voltage sag with a depth of 20% and the corresponding compensating voltage. Fig.8(c) shows the phase-a sag-free load voltage.

Fig.9(a) shows the dc-link capacitor voltage during the voltage-swell condition for both NLS and PI- controller, it is found that both over-shoot and settling time are less in case of proposed NLS technique for better compensation of voltage-swell.Fig.9(b) shows the waveform of phase-a voltage swell of 16% and its compensating voltage.Fig.9(c) shows the swell-free phase-a load voltage.Fig.10(a) shows the dc-link capacitor voltage during the supply voltage unbalance, and it is observed that the dc-link voltage has less over-shoot and settling time during the voltage unbalance. This makes NSL has better compensation capability as compared to the PI-controller. Fig.10(a)-(c)shows the unbalance source voltage ,compensating voltage and load voltage. Table II shows the total harmonic distortions (THD) and real and reactive power comparison between the proposed NLS and PI-controller.Fig.11 presents the source current spectrum of both the controller after compensation.

TABLE II. THD,REAL AND REACTIVE POWER MEASUREMENT

	NLS-Controller	PI-Controller
THD(%)	3.37%	4.28%
Real Power	9.89kW	9.25kW
Reactive Power	16VAR	44VAR

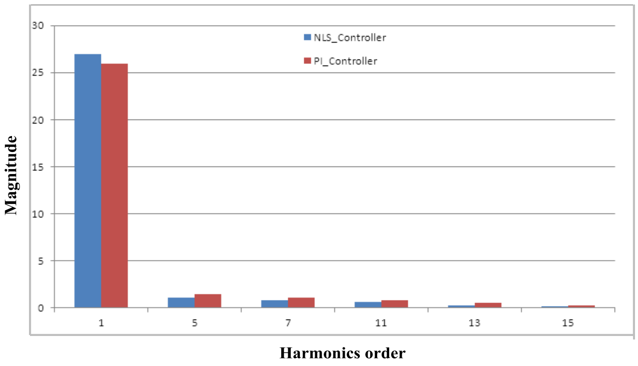


Fig.11 Source current spectrum after compensation

V. CONCLUSIONS

This paper presents a non-linear sliding mode control technique for dc-link voltage control for UPQC. The NLS strategy is more superiors than the existing strategies for controlling the dc-link voltage of UPQC, as it provides less overshoot and settling time for the dc-link capacitor voltage during the transient, voltage sag, swell and voltage unbalance. Thus, it introduces less error during the compensation process and provides adequate results.Subsequently the proposed approach for controlling the dc-link voltage of UPQC conveys high performance owing to change of damping ratio by means of the non-linear sliding surface. New functionality is added to the UPQC system for quick extraction of the reference signal from source voltage and compensating current and voltage. The Opal-RT results demonstrate that, the aforementioned control algorithm eliminates all power quality related problems and regulated the dc-link voltage with less overshoot and settling time.

REFERENCES

[1] A. G. a. G.Ledwich, *Power Quality Enhancement Using Custom Power Devices*. Bosten,M.A: Kluwer, 2002.

[2] R. K. Patjoshi and K. K. Mahapatra, "Performance comparison of direct and indirect current control techniques applied to a sliding mode based shunt active power filter," in *India Conference (INDICON)*, Mumbai, 2013.

[3] R. K. Patjoshi and K. K. Mahapatra, "New control strategy of unified power quality conditioner with sliding mode approach," in *India Conference (INDICON)*, IIT,Mumbai, 2013 .

[4] K. Karanki, G. Geddada, M. K. Mishra, and B. K. Kumar, "A Modified Three-Phase Four-Wire UPQC Topology With Reduced DC-Link Voltage Rating,", *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3563-3572, July 2014.

[5] Teke,Ahmet, Lütfü Saribulut, and Mehmet Tumay."A novel reference signal generation method for power-quality improvement of unified power-quality conditioner." *IEEE Trans.Power Del.,* vol. 26, no. 4,pp.2205-2214,Oct.2011

[6] A. Bartoszewicz and A. Nowacka-Leverton, "SMC without the reaching phase - the switching plane design for the third-order system," *Control Theory & Applications, IET* , vol. 1, no. 5, p. 1461,1470, Sept. 2007.

[7] SB Choi, CC Cheong, DW Park,"Moving switching surfaces for robust control of second-order variable structure systems," *International Journal of Control*, vol. 58, no. 1, pp. 229-245, Mar 2007.

[8] B Bandyopadhyay,D Fulwani,"High-performance tracking controller for discrete plant using nonlinear sliding surface," *IEEE Trans. Ind Electron.*, vol. 56, no. 9, pp. 3628-3637, Sept-2009.

[9] AE Khalick M, N Uchiyama, S Sano "Sliding mode contouring control design using nonlinear sliding surface for three-dimensional machining," *International Journal of Machine Tools and Manufacture*, vol. 65, no. 2, pp. 8-14, 2013.

[10] M. Kesler and E. Ozdemir, "Synchronous-Reference-Frame-Based Control Method for UPQC Under Unbalanced and Distorted Load Conditions," *IEEE Trans.Ind Electron.*, vol. 58, no. 9, pp. 3967-3975, Sept.2011.

[11] B Bandyopadhyay,D Fulwani,"Non-linear sliding surface: towards high performance robust contro," *Control Theory & Applications, IET*, vol. 6, no. 2, pp. 235-242, May.2011.

[12] M Aredes, H Akagi, EH Watanabe,"Comparisons Between the p--q and p--q--r Theories in Three-Phase Four-Wire Systems," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 924-933, Apr.2009.

[13] K. H. Kwan, Y. C. Chu, and P. L. So, "Model-Based H-infinity Control of a Unified Power Quality Conditioner," *IEEE Trans. Ind Electron.*, vol. 56, no. 7, pp. 2493-2504, Jul.2009.

[14] A. Teke, L. Saribulut, and M. Tumay, "A Novel Reference Signal Generation Method for Power-Quality Improvement of Unified Power-Quality Conditione," *IEEE Trans.Power De.l,* ,vol. 26, no. 4, pp. 2205,2214, Oct. 2011.