

A Low-Power CMOS Flip-Flop for High Performance Processors

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Abstract— A significant amount of the total power in highly synchronous systems gets dissipated over clock networks. Therefore, low-power clocking schemes would be promising approaches for high performance designs. To reduce the power consumption and delay, a new flip-flop circuit technique has been designed in CMOS domino logic. These flip-flops are a class of dynamic circuit that can be interfaced with both static and dynamic circuits. This flip-flop results in significant energy savings and operates in high speed. Based on simulation results of UMC 180 nm technology and 200 MHz frequency, we have simulated the flip-flop circuit and compared the result with the previous proposed flip-flops simulated with the same environment. The comparison results of the proposed flip-flop with the previous proposed flip-flop shows that the proposed circuit reduces 80% of power consumption and the speed increases to 70-90%.

Keywords—Flip-Flop; CMOS; Domino logic; Dynamic logic; Low power; Power-delay product; processors

I. INTRODUCTION

The clock system, which consists of the clock distribution network and timing elements like flip-flops and latches, are most power consuming components in a VLSI system [1] [2] [3] [4] [5] [6]. This system snatches the maximum portion of power in a system [7] [4]. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed.

With the continuing increase in the clock frequency and complexity of high performance VLSI chips, the resulting increase in power consumption has become the major obstacle to the realization of high-performance designs [8]. In addition to increased cooling costs, increased power consumption shortens the battery lifetime in portable applications.

Many researchers have proposed number of flip-flop circuits recently to minimize power, delay and noise of the system. In this paper, we have proposed a

new flip-flop circuit with CMOS domino logic which, reduces power and increases the speed of the circuit.

The remainder of the circuit is organised as follows. Section II contains the background work in which we have shown some recent proposed flip-flop circuits. Section III describes the low-power flip-flop logic style for high performance processors and its working process. Section IV gives the simulation results of the proposed flip-flop. Section V compares the simulation results of 1-bit of proposed flip-flop with other flip-flops. Section VI concludes the paper and shows the amount of power saving and amount of speed increased in this flip flop.

II. BACK GROUND FLIP-FLOP DESIGNS

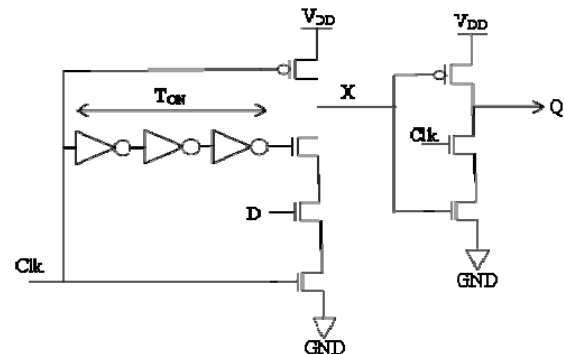


Figure 1 Basic dynamic FF

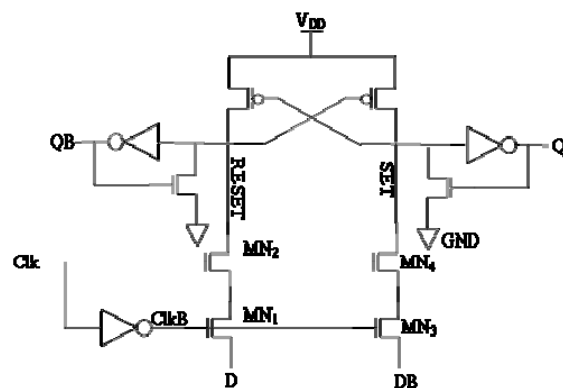


Figure 2 SDER FF

A. BASIC CMOS FLIP-FLOP

The node X is precharged to V_{DD} when $Clk = 0$. The cascaded inverter generates a very narrow pulse at every rising edge of the Clk. If $D = 1$, then node X discharge through series connected of three transistors driving Q to 1. If D remains 1, node X will be discharged at every rising edge of the Clk. This leads to larger switching power. When $D = 0$, node X remains at 1 driving Q to 0.

B. SDER FLIP-FLOP

The input data (D) and its inverted output DB applied to MN_1, MN_3 respectively. The clock signal (Clk) and its inverted output (ClkB) generates an implicit conducting pulse at every rising edge of Clk. Clk and ClkB applied to MN_2, MN_4 and MN_1, MN_3 respectively. At rising edge of CLK all these transistor starts conducting for a short duration of time determined by delay of inverter and allows D & DB to reach at RESET & SET node. Q and QB retain the old values till the next rising edge of Clk. This flip-flop is called as static because SET and RESET nodes retains the state of the flip-flop without being precharged. If the input data remains idle no internal switching occurs at SET and RESET node results in low power consumption at low data switching activity.

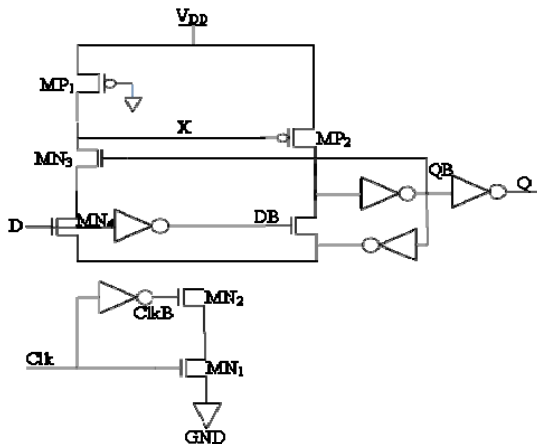


Figure 3 SCCER FF

C. SCCER FLIP-FLOP

A weak pull up transistor MP_1 is used to charge the node X to V_{DD} . The clock signals (Clk) and its inverted output (ClkB) generates an implicit conducting pulse at every rising edge of Clk allowing MN_1 & MN_2 to conduct. MN_3 controlled by QB provides a conditional discharging path for node X. Since MN_3 controlled by QB, no discharge occurs at node X as long as D remains HIGH, results in low power consumption. The worst case timing of this design occurs if $D = 1$ and node X discharges through four transistors connected in series. This requires a wider MN_1 & MN_2 for proper discharging of node X.

III. PROPOSED FLIP-FLOP

The proposed FF uses the proposed logic of this thesis. It modifies the basic FF in the way that described in this thesis. The proposed FF has a precharge PMOS M_1 , a keeper PMOS M_2 . NMOS M_3 inputs the delayed clock and NMOS M_4 inputs D. M_1 and M_5 input the Clk, where M_5 acts as the stack transistor. At the evaluation phase when the PDN is conducting, at that time M_5 stops the free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node. To compensate that M_6 makes a charge discharge path. Here M_7 again acts as a stack for the 2nd path to maintain the dynamic node. Hence circuit becomes extra noise robust and reduces the leakage power consumption. This can be increased by widening the M_2 (high W/L) to make it more conducting.

M_{10} should be grounded according to the basic circuit technique has connected to the N_FOOT in this proposed flip-flop. By doing this, the continuous switching activity of the N_FOOT does not pass to the output node. This reduces the power consumption and noise of the circuit. As the output does not switch many time, the circuit delay also becomes less and circuit gets fast.

When $Clk = 0$, the node X or the dynamic node is gets precharged to V_{DD} . The cascaded inverter, which inputs to M_3 , generates a very narrow pulse at every rising edge of the Clk.

When $D = 1$, then node X i.e. The dynamic node discharge through series connected of three transistors M_3, M_4 and M_5 driving X to 0 and output node i.e. Q to 1. If D remains 1, node X will be discharged at every rising edge of the Clk. This leads to larger switching power.

When $D = 0$, node X remains at 1 driving Q to 0. These conditions satisfy the conditions of D-FF.

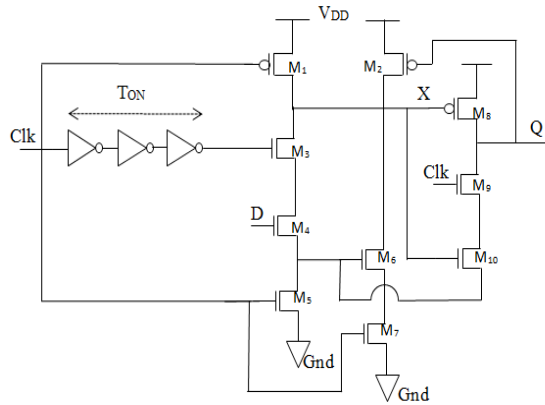


Figure 4Proposed FF

IV. SIMULATION RESULTS OF PROPOSED 1-BIT FLIP-FLOP

All the flip-flops were designed using UMC 180 nm process technology with a supply voltage of 1.8 V. The designs were optimized at a temperature of 27 degree centigrade for a clock frequency of 200 MHz. Load capacitance of 30 fF was used for all outputs. Fig. 3.41 illustrates the timing definitions for the flip-flops. Delay was measured with 50% of signal transitions. Setup time is the time from when data becomes stable to the rising transition of the clock signal. The hold time is the time from the rising transition of the clock to the earliest time that data may change after being sample. Setup and hold times are measured with reference to the 50% of rising transition of the clock. Table 1 and Figure 6 compare the power, delay and PDP of all the FFs.

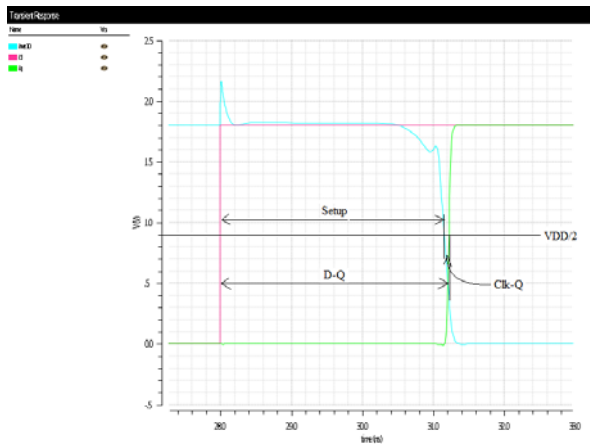
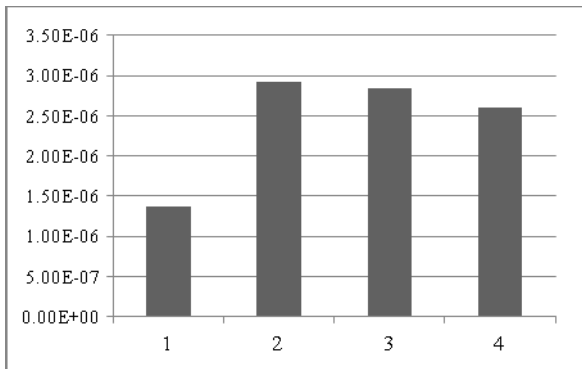
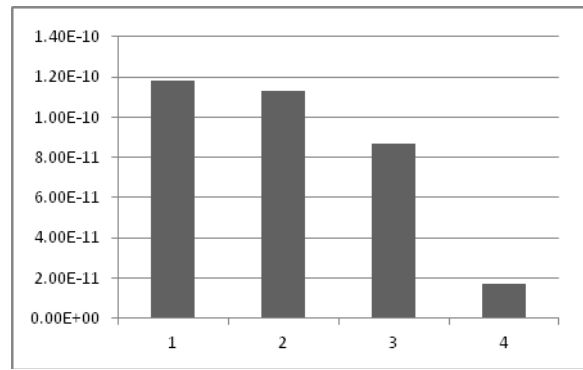


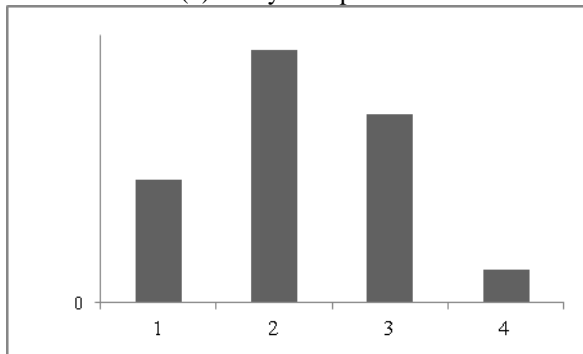
Figure 5 Proposed FF output illustrating timing definitions



(a) Power Comparison



(b) Delay Comparison



(c) PDP Comparison

1. Basic FF 2. SDER FF 3. SCCER FF 4. Proposed FF

Figure 6 Power, delay and PDP comparison of all FFs

Table 1 Power, delay and PDP comparison of all the flip-flops

PARAMETER	POWER (W)	DELAY (S)	PDP
BASIC FF	1.37E-06	1.18E-10	1.6166E-16
SDER FF	2.93E-06	1.13E-10	3.3109E-16
SCCER FF	2.84E-06	8.69E-11	2.468E-16
PROPOSED	2.60E-06	1.67E-11	4.342E-17

V. COMPARISON RESULT OF 1-BIT PROPOSED FLIP-FLOP WITH OTHER FLIP-FLOPS

The proposed flip-flop was compared with the previous proposed flip-flops. For individual flip-flop simulations, an ideal sinusoidal clock was used. Figure 7 shows clock-to-output (Clk-Q) delay versus setup time for all the flip-flops and Figure 8 shows data-to-output (D-Q) delay versus setup time for all the flip-flops. It is clearly visible that the delay outputs of the previous proposed flip-flops were much more than that of the proposed flip-flop. These outputs give a clear illustration of the behavior of the proposed flip-flop in the minimum delay region.

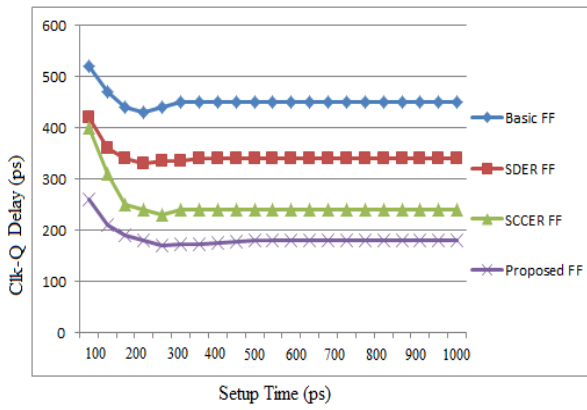


Figure 7 Clk-Q Delay Vs Setup Time

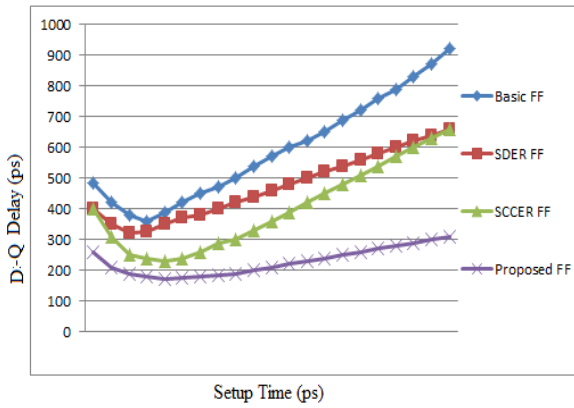


Figure 8 D-Q Delay Vs Setup Time

For any flip-flop, there is a specific setup time which results in a minimum D-Q delay. This optimum setup time is used in this paper for the comparison of setup time. As shown in the graph of Figure 9 the Clk-Q delay becomes independent of setup time for more setup times. The proposed flip-flop has lowest Clk-Q delay and D-Q delay in comparison to all the previous proposed flip-flops. Among all other flip-flops SCCER FF has lowest D-Q delay and SDER has lowest Clk-Q delay.

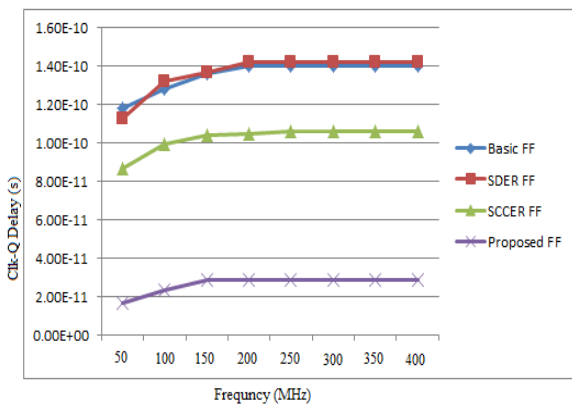


Figure 9 Clk-Q Delay versus Frequency for all FFs

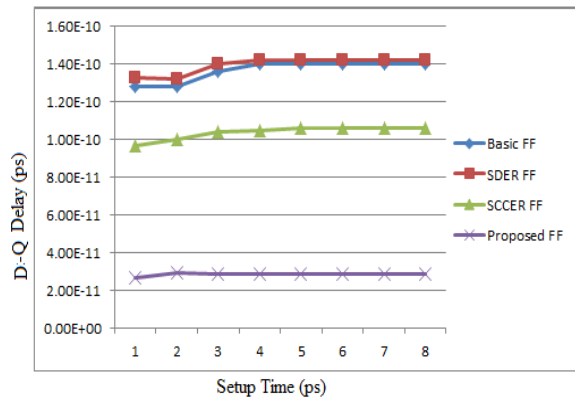


Figure 10 D-Q Delay versus Frequency for all FFs

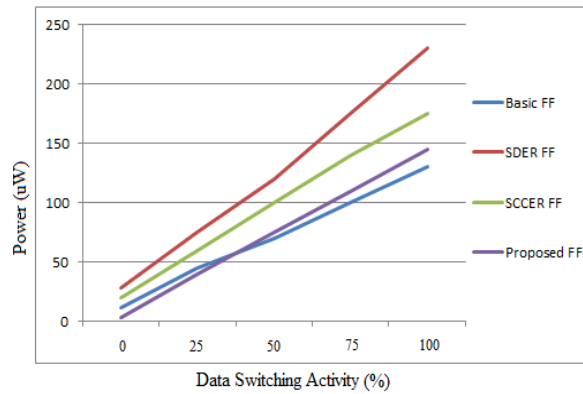


Figure 11 Power Vs Data Switching Activity at 50 MHz

Figure 9 and Figure 10 show the dependent of Clk-Q delay with frequency and D-Q delay with frequency. These flip-flops were simulated with a frequency of 50 MHz to 400 MHz or their maximum frequency of operation. The flip-flops were kept same for all the frequencies i.e. not optimized for each frequency of operation. The proposed flip-flop does not fail on a frequency above 400 MHz but other flip-flops fail on a frequency above 400 MHz. The proposed flip-flop has less dependency upon clock frequency.

Figure 10 shows the power as a function of data switching activity for all the flip-flops. Proposed FF has lowest power consumption for data switching activity less than 50%. For more than 50 % of data switching activity basic FF consumes lowest power. This is due to the fact that at higher switching activity there is a less opportunity of energy saving.

VI. CONCLUSION

In this paper, we proposed a new low power high speed flip-flop circuit designed with CMOS domino logic. All the circuits were designed and simulated with cadence spectre using 180 nm UMC process using 200 MHz clock frequency and 27⁰ C. This flip-flop resulted in significant energy savings and operates

in high speed. Based on simulation results of UMC 180 nm technology and 200 MHz frequency, we simulated the flip-flop circuit and compared the result with the previous proposed flip-flops simulated with the same environment. The comparison results of the proposed flip-flop with the previous proposed flip-flop shows that the proposed circuit reduces 80% of power consumption and the speed increases to 70-90%.

VII. REFERENCES

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