# A Two-Dimensional Subthreshold Current Model of Recessed-Source/ Drain (Re-S/D) SOI MOSFETs with High-k Dielectric

Gopi Krishna Saramekala
*Department of Electronics and Communication Engineering*, National Institute of Technology, Rourkela 769008, Orissa, India, gopi.saramekala@gmail.com.

Pramod Kumar Tiwari, *Member IEEE*
*Department of Electronics and Communication Engineering*, National Institute of Technology, Rourkela 769008, Orissa, India; Tel.:+91-0661 2462467; tiwarip@nitrkl.ac.in

***Abstract*— An analytical surface-potential based subthreshold current model for short-channel recessed-source/ drain (Re-S/D) SOI MOSFETs with high-k dielectric is presented in this paper. The two-dimensional (2D) Poisson's equation has been solved in the channel region with suitable boundary conditions in order to determine the surface potential. The diffusion component of current density is considered for the subthreshold current modeling. The impact of EOT (Effective Oxide Thickness) ( $t'_{ox}$ ), channel Length ( $L$ ), gate-dielectric constant ( $\varepsilon'_{ox}$ ) on subthreshold current has been investigated. The proposed model has been validated by comparing the analytical results with numerical simulation data obtained from ATLAS™, a two dimensional device simulator from SILVACO.**

***Keywords- recessed-source/ drain (Re-S/D); subthreshold current; mimimum surface potential, gate dielectric constant.***

## I. INTRODUCTION

The conventional MOSFET has relentlessly been scaled down in size for the past 3 decades. As the dimensions of the device are at onset of its physical limit, the trade of between switching speed and power dissipation has become extremely important [1]. Since, CMOS scaling has become very challenging as indicated by the International Technology Roadmap for Semiconductors (ITRS) [2], a number of non-conventional CMOS devices have been proposed, fabricated and tested in order to keep the MOSFET scaling on in near future. The fully-depleted (FD) recessed-source/ drain (Re-S/D) silicon-on insulator (SOI) MOSFET is supposed to be an attractive option for further scaling because of its low parasitic capacitances, reduced series resistance, high drive current, very high switching speed and compatibility with the planner CMOS technology [3-7]. A number of attempts have already been made to present analytical, experimental and numerical simulation based analysis of the Re-S/D SOI MOSFETs [3-7]. Sivilic and co-worker have presented an analytical threshold voltage model [4] and subthreshold swing model [5] for the device. Kumar et al. [5] have presented an analytical threshold voltage model for Re-S/D SOI MOSFETs considering the effect of substrate induced surface potential. Kumar *et al*. [5] claimed that the device is highly scalable and could be scaled down upto 10nm channel length. However, as per device scaling rule, a device with such a short channel length should have a very thin gate oxide in order to curb the undesirable short-channel effects. However, a thin gate oxide causes quantum mechanical tunneling through the gate and results in an unacceptable amount of gate leakage current [8, 9]. Therefore, a high-k gate dielectric material, which provides large physical thickness for a small electrical thickness, should be used in Re-S/D SOI MOSFETs fabrication. Further, as high-k dielectric material induced fringing field lines influence the channel electrostatic potential, it is very important to analyze the subthreshold characteristics of the device in presence of a high-k dielectric material. However, in the best of our knowledge, no such analysis is available in the technical literature till now.

In this paper, an analytical subthreshold current model for short-channel recessed-source/drain (Re-S/D) SOI MOSFETs with high-k dielectric is presented for the first time considering that the subthreshold current is mainly contributed by the diffusion of the charge carriers in the subthreshold regime of the device operation.

## II. DEVICE STRUCTURE

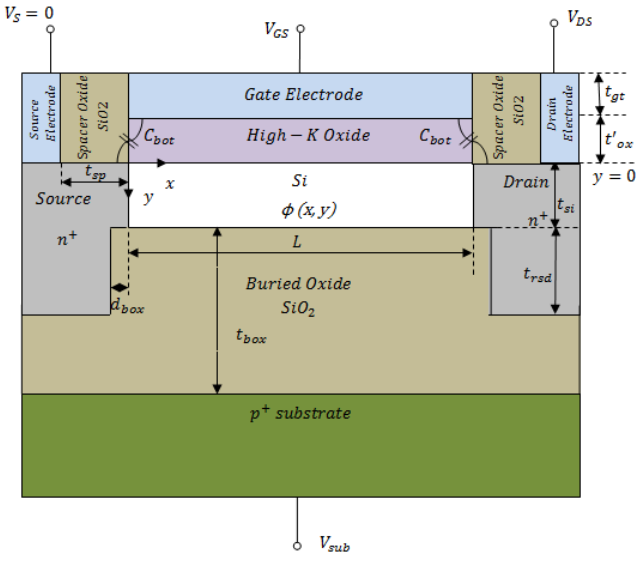


Figure 1. Cross sectional view of DMG-Re- S/D on SOI MOSFET.

The schematic structure of a Re-S/D SOI MOSFET, which is considered for our model and simulation is shown in Fig.1 where $L$ is the channel length, $t_{Si}$ , $t_{box}, t_{rsd}, t_{sp}, t_{gt}$ and $N_a$ are the channel thickness, buried oxide (BOX) thickness, recessed source drain thickness, spacer length, gate electrode thickness of the device and doping concentration in the silicon channel region respectively. It should be noted that the gate dielectric thickness shown in the figure are actually the electrical (or effective) thickness $t'_{ox}$ , where, $t'_{ox} = t_{ox}\left(\frac{\varepsilon_{Sio2}}{\varepsilon'_{ox}}\right)$ and $t_{ox}$ is physical thickness of the gate dielectric, $\varepsilon_{Sio2}$, $\varepsilon'_{ox}$ are the permittivity of silicon dioxide and gate dielectric material respectively.

The x- and y-axes are considered to be along the channel Length and channel thickness respectively, as shown in Fig.1. The high-k gate-dielectric considered for modeling and simulations is $HfO_2$ with a permittivity of 22, except for the fig.4. The device parameters of the structure used in both modeling and simulation are shown in the Table1.

TABLE I. DEVICE DIMENSIONS AND PARAMETERS USED FOR MODEL CALCULATIONS AND SIMULATIONS.

| **Parameters** | | **Values** |
|---|---|---|
| Gate work-function | $(\psi_M)$ | 4.8eV |
| Channel Doping | $(N_a)$ | $10^{16}$ cm$^{-3}$ |
| Source/Drain Doping | $(N_d)$ | $10^{20}$ cm$^{-3}$ |
| Substrate Doping | $(N_{sub})$ | $10^{15}$ cm$^{-3}$ |
| Channel Thickness | $(t_{Si})$ | 6nm |
| Front Channel Oxide Thickness | $(t'_{ox})$ | 1-2nm |
| Buried Oxide Thickness | $(t_{box})$ | 100nm |
| Recessed thickness | $(t_{rsd})$ | 20nm |
| Recessed length | $(d_{box})$ | 3nm |
| Channel Length | $(L)$ | 30-40nm |
| Gate Voltage | $(V_{GS})$ | 0.1-0.6V |
| Drain Voltage | $(V_{DS})$ | 0.1V |
| Substrate Voltage | $(V_{sub})$ | 0V |

## III. ANALYTICAL MODELING

### A. *Surface Potential Model*

The 2-D Poisson's equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}} \tag{1}$$

where, $\psi(x,y)$ is the potential distribution in the channel region.; $N_a$ is the effective body doping concentration; $q$ is the electronic charge and $\varepsilon_{Si}$ is the permittivity of Silicon, is solved in the channel region. The potential distributions in the channel region is assumed to be parabolic functions [6,7 ]

$$\psi(x,y)=\psi_f(x)+C_1(x)y+C_2(x)y^2 \tag{2}$$

The coefficients $C_1(x)$ and $C_2(x)$ are function of $x$ only. These coefficients are determined by using boundary conditions given in Ref[4, 5].

Now, substituting $C_1(x)$ and $C_2(x)$ in Eq.(2) gives the following expression of 2D channel potential $\psi(x,y)$

$$\begin{aligned}\psi(x,y)=\psi_f(x)+\frac{C_{ox}}{t_{Si}.C_{Si}}\left[\psi_f(x)-(V_G-V_{FB1})\right]y+\\ y^2\left\{\frac{C_{rsd}}{2t_{Si}^2.C_{Si}}\left[V_{DS}-2V_{FB2}-\psi_b(x)\right]\right.\\ +\frac{C_{box}}{2t_{Si}^2.C_{Si}}\left[V_{sub}+\Delta V-V_{FB3}-\psi_b(x)\right]\\ \left.+\frac{C_{ox}}{2t_{Si}^2.C_{Si}}\left[\psi_f(x)-(V_G-V_{FB1})\right]\right\}\end{aligned} \tag{3}$$

where $C_{rsd}$ is the recessed source/drain buried-oxide capacitances per unit length, $C_{box}$ is the buried oxide capacitance per unit length and $C_{Si}$ , is the silicon body capacitance per unit length, $\psi_f(x)$ and $\psi_b(x)$ are the surface potential at SiO2/channel and channel/ BOX interface, respectively. $V_{DS}$ is the drain voltage and $V_{FB1}, V_{FB2}, V_{FB3}$ are the flat band voltages for the gate, source/drain-back-gate and substrate-back-gate respectively. It is worth mentioning that all capacitances and flat band voltages have been defined in our earlier publications [5, 7]

Now, using Eq.(3) in Eq.(1) gives the partial differential equation of front and back surface potential. Further, the solution of those partial differential equations with suitable boundary conditions gives the following expressions for the front and back surface potential

$$\psi_{f,b}=A_{f,b}.e^{\sqrt{\alpha_{f,b}}x}+B_{f,b}.e^{\sqrt{\alpha_{f,b}}x}-\frac{\beta_{f,b}}{\alpha_{f,b}} \tag{4}$$

where ,

$$A_{f,b}=\frac{\left\{\beta_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L}-1\right)+\alpha_{f,b}\left[V_{bi}\left(e^{\sqrt{\alpha_{f,b}}L}-1\right)+V_{DS}e^{\sqrt{\alpha_{f,b}}L}\right]\right\}}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L}-1\right)} \quad (5)$$

$$B_{f,b}=\frac{e^{\sqrt{\alpha_{f,b}}L}\left\{\beta_{f,b}\left(e^{\sqrt{\alpha_{f,b}}L}-1\right)-\alpha_{f,b}\left[V_{bi}\left(1-e^{\sqrt{\alpha_{f,b}}L}\right)+V_{DS}\right]\right\}}{\alpha_{f,b}\left(e^{2\sqrt{\alpha_{f,b}}L}-1\right)} \quad (6)$$

where, $\alpha_{f,b}$, $\beta_{f,b}$ are constants which are determined from boundary conditions[4], $V_{bi}$ is the built-in voltage at the source/drain and Si given by $V_{bi}=\frac{kT}{q}\ln\left(\frac{N_aN_d}{n_i^2}\right)$, $N_d$ is the doping concentration, $n_i$ is the intrinsic carrier concentration in the silicon,

The positions $(x_{min})_{f,b}$ of the front and back channel minimum surface potentials can be obtained by solving $\left.\frac{d\psi_{f,b}(x)}{dx}\right|_{(x_{\min})_{f,b}}=0$ and are determined as

$$(x_{\min})_{f,b}=\frac{1}{2}\frac{\ln\left(\frac{B_{f,b}}{A_{f,b}}\right)}{\sqrt{\alpha_{f,b}}} \quad (7)$$

Further, the minimum value of the front-surface/back-surface potential $\psi_{f,b\,min}$ is obtained by substituting $(x_{\min})_{f,b}$ of Eq.(7) into Eq.(3)

$$\psi_{f,b\min}=2\sqrt{A_{f,b}B_{f,b}}-\sigma_{f,b} \quad (8)$$

where, $A_{f,b}$, $B_{f,b}$ are the device dependent constants.

### *B. Effect of high-k dielectric induced fringing field lines on the surface potential*

It is worth mentioning that the fringing field lines that emerge from the bottom of gate electrode terminate either at the source or the drain terminals. Thus, the additional charges are induced in the source and drain region due to the fringing field lines. The potential at a distance *x* from the source and drain due to the induced charges could be given as[10]

$$V(x,\sigma_i)=\frac{\sigma_i}{8\pi\varepsilon_{Si}}\left[\left(x+t_{sp}\right)\ln\left\{\frac{\sqrt{\left(x+t_{sp}\right)^2+\left(\frac{W^2}{4}\right)}+\left(\frac{W}{2}\right)}{\sqrt{\left(x+t_{sp}\right)^2+\left(\frac{W^2}{4}\right)}-\left(\frac{W}{2}\right)}\right\}-x.\ln\left\{\frac{\sqrt{\left(x+t_{sp}\right)^2+\left(\frac{W^2}{4}\right)}+\left(\frac{W}{2}\right)}{\sqrt{\left(x+t_{sp}\right)^2+\left(\frac{W^2}{4}\right)}-\left(\frac{W}{2}\right)}\right\}+W.\ln\left\{\frac{\sqrt{\left(x+t_{sp}\right)^2+\left(\frac{W^2}{4}\right)}+t_{sp}+\sqrt{x^2+{t_{sp}}^2+2t_{sp}\sqrt{x^2+\left(\frac{W^2}{4}\right)}}}{\sqrt{x^2+\left(\frac{W^2}{4}\right)}+x}\right\}\right] \quad (9)$$

where, $\sigma_i=\left(\frac{(C_{bot})V_{pi}}{W.t_{sp}}\right)$ for $i=1,2$, $V_{p1}=V_{bi}-V_{GS}+V_{FB2}$ and $V_{p2}=V_{bi}+V_{DS}-V_{GS}+V_{FB2}$ are the source and drain region potential respectively, $C_{bot}=\frac{(0.3)\varepsilon_{eff}W}{\pi}$ is the parasitic internal fringe capacitances associated with bottom edge of gate electrode ,

$\varepsilon_{eff}=\frac{\varepsilon_k\varepsilon_{sp}^{'}}{\varepsilon_k-\varepsilon_{sp}^{'}}\ln\left(\frac{\varepsilon_k}{\varepsilon_{sp}^{'}}\right)$ , $\varepsilon_{sp}^{'}=\left(1+\frac{t_{ox}^{\prime}}{L}\right)\varepsilon_{sp}$ is the effective permittivity of spacer material,. $W$ is width of gate and $t_{sp}$ is spacer thickness between gate sidewall and source/drain contacts. $\varepsilon_k$ and $\varepsilon_{sp}^{\prime}$ are the permittivity of gate dielectric and spacer material respectively.

Now, in order to include the effect of high-k induced fringing field lines, two additional potential terms, $V(x)|_{source}$ and $V(L_g-x)_{drain}$ are added in the minimum of the surface potential of Eq. (14). Thus, the modified equations for minimum of the surface potential are

$$\psi^{\prime}_{\min f,b}=2\sqrt{A_{f,b}B_{f,b}}-\frac{\beta_{f,b}}{\alpha_{f,b}}+\left(V(x)|_{source}+V\left(L_g-x\right)_{drain}\right)\Big|_{x=x_{\min}} \quad (10)$$

Further, $\psi(x,y)$ of Eq.(3) can be represented either as a function of $\psi_f(x)$ or $\psi_b(x)$ using Eq.(2) in (3). Subsequently, $\psi_f(x)$ or $\psi_b(x)$ of $\psi(x,y)$ could be replaced by $\psi^{\prime}_{\min f}$ or $\psi^{\prime}_{\min b}$, respectively, in order to

obtain the following equations of the virtual cathode potential $\psi_{vc}(y)$

$$\psi_{vc}(y) = \psi'_{\min f}\left[1+\frac{C_{ox}}{C_{si}t_{Si}}y-\frac{C_{ox}}{C_{si}t_{Si}^{\,2}}y^2 - \left(2C_{si}+C_{ox}\right)z_1y^2\right] + (V_{GS}-V_{FB1})\left[-\frac{C_{ox}}{C_{si}t_{Si}}y+\frac{C_{ox}}{2C_{si}t_{Si}^{\,2}}y^2-(C_{ox})z_1y^2\right] + (V_{DS}-2V_{FB2})\left[\frac{C_{rsd}}{2C_{si}t_{Si}^{\,2}}y^2+(C_{rsd})z_1y^2\right] + (V_{sub}-V_{FB3})\left[\frac{C_{box}}{2C_{si}t_{Si}^{\,2}}y^2+(C_{box})z_1y^2\right] \quad (11)$$

where

$$z_1 = \left(\frac{2C_{rsd}+C_{box}}{2C_{si}t_{Si}^{\,2}\left(2C_{si}+2C_{rsd}+C_{box}\right)}\right) \quad (12)$$

$$\psi_{vc}(y) = \psi'_{\min b}\left[\left(\frac{2C_{si}+2C_{rsd}+C_{box}}{2C_{si}+C_{ox}}\right)z_2 - \left(\frac{C_{rsd}}{C_{si}t_{Si}^{\,2}}+\frac{C_{box}}{2C_{si}t_{Si}^{\,2}}\right)y^2\right] + (V_{GS}-V_{FB1})\left[-\frac{C_{ox}}{C_{si}t_{Si}}y+\frac{C_{ox}}{C_{si}t_{Si}^{\,2}}y^2+\left(\frac{C_{ox}}{2C_{si}+C_{ox}}\right)z_2\right] + (V_{DS}-2V_{FB2})\left[\frac{C_{rsd}}{C_{si}t_{Si}^{\,2}}y^2-\left(\frac{C_{rsd}}{2C_{si}+C_{ox}}\right)z_2\right] + (V_{sub}-V_{FB3})\left[\frac{C_{box}}{C_{si}t_{Si}^{\,2}}y^2-\left(\frac{C_{box}}{2C_{si}+C_{ox}}\right)z_2\right] \quad (13)$$

where, $z_2 = \left(1+\frac{C_{ox1}}{C_{si1}t_{Si}}y-\frac{C_{ox1}}{2C_{si1}t_{Si}^{\,2}}y^2\right)$ (14)

Thus, two equations of virtual cathode potential have been derived and any one of them could be used for subthreshold current modeling.

### *C. Subthreshold CurrentModel*

Assuming that the diffusion is the dominant current flow mechanism in the subthreshold regime, we have modified the drift diffusion equation as

$$J_n(y) = \frac{qD_n n_{\min}(y)}{L_e}\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (15)$$

where, $D_n$ is the coefficient of diffusion, $L_e$ is the effective channel length [11], $V_T$ is the thermal voltage. The electron density at the virtual cathode, $n_{\min}(y)$ can be expressed as [11]

$$n_{\min}(y) = \frac{n_i^{\,2}}{N_a}\exp\left(\frac{\psi_{vc}(y)}{V_T}\right) \quad (16)$$

Now, the integration of $J_n(y)$ for $y$=0 to $t_{Si}$ gives the following subthreshold current equation

$$I_{sub} = \int_0^{t_{Si}} J_n(y)dy \quad (17)$$

Now, by following the method of Refs.[7, 11], the above eqn.(17) has been solved to obtain the following subthreshold current equation

$$I_{sub} = KV_T\left[\frac{\exp\left(\frac{\psi_{vc}(y=0)}{V_T}\right)-\exp\left(\frac{\psi_{vc}(y=y_m)}{V_T}\right)}{(\psi_{vc}(y=0)-\psi_{vc}(y=y_m))/y_m} + \frac{\exp\left(\frac{\psi_{vc}(y=y_m)}{V_T}\right)-\exp\left(\frac{\psi_{vc}(y=t_{Si})}{V_T}\right)}{(\psi_{vc}(y=y_m)-\psi_{vc}(y=t_{Si}))/(t_{Si}-y_m)}\right] \quad (18)$$

where, $y_m$ is the position where the virtual cathode has the lowest potential value; and

$$K = \frac{qD_nV_Tn_i^{\,2}}{L_eN_a}\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (19)$$

## IV. VALIDATION OF MODEL

In this Section, we have presented model results and the same have been compared with numerical simulation results. The simulations have been carried out using a 2-D numerical device simulator (ATLAS$^{TM}$)[12]. The simulations are performed using the drift-diffusion model for carrier transportation, SRH model for recombination, Fermi Dirac carrier statistics for carrier distribution and CVT mobility model for doping and parallel field dependence.

Fig. 2 plots the subthreshold current against the gate-to-source voltage for the device channel lengths of 30 and 40nm keeping other device parameters constant. $HFO_2$ is considered to be the dielectric material in the device with physical thickness of 5.8nm. The higher value of subthreshold current at shorter channel length for a fixed gate voltage may be attributed to the excess short channel effects in the device.

The effect of gate oxide thickness on the subthreshold current is examined in Fig. 3. The subthreshold current characteristics are plotted with gate-to-source voltages for

two different effective oxide thicknesses whereas the channel length is 40nm. It is worth noting that the thinner gate oxide renders lower subthreshold current because gate remains in a position to control the channel charges effectively.

In Fig.4, subthreshold current has been plotted against gate to source whereas gate-dielectric constant is a variable parameter. The device with a higher gate-dielectric constant is found to be having lesser subthreshold leakage current.

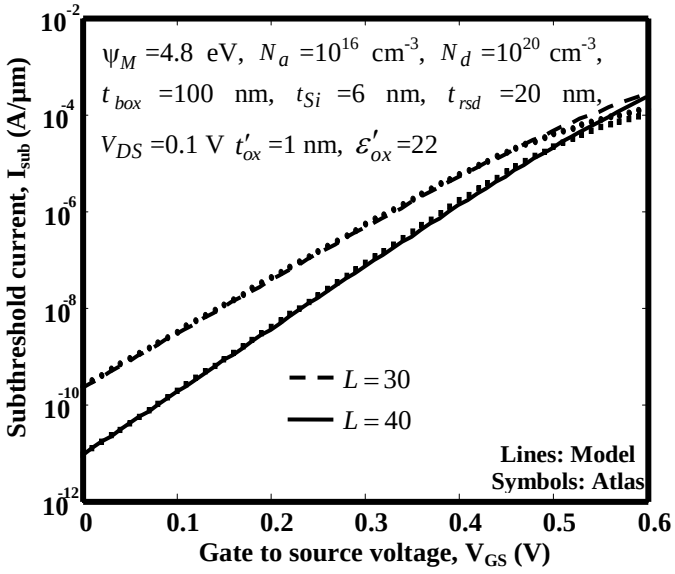


Figure 2. Subthreshold current versus gate to source voltage for different channel Length.

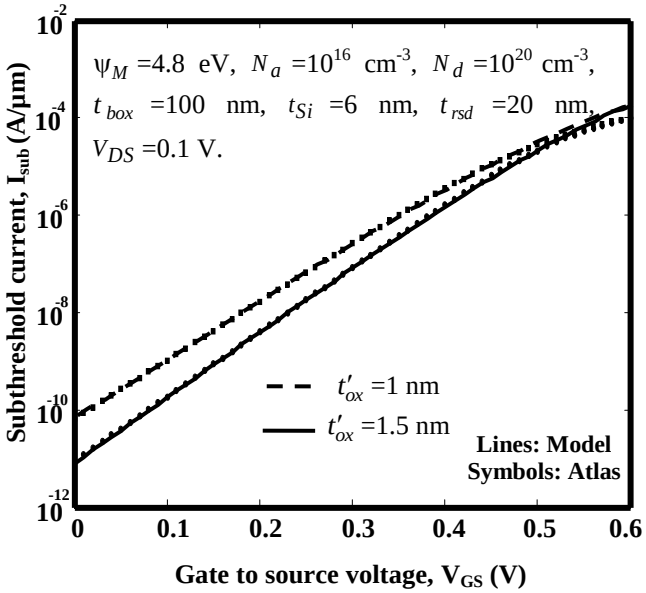


Figure 3. Subthreshold current versus gate to source voltage for different oxide thickness.

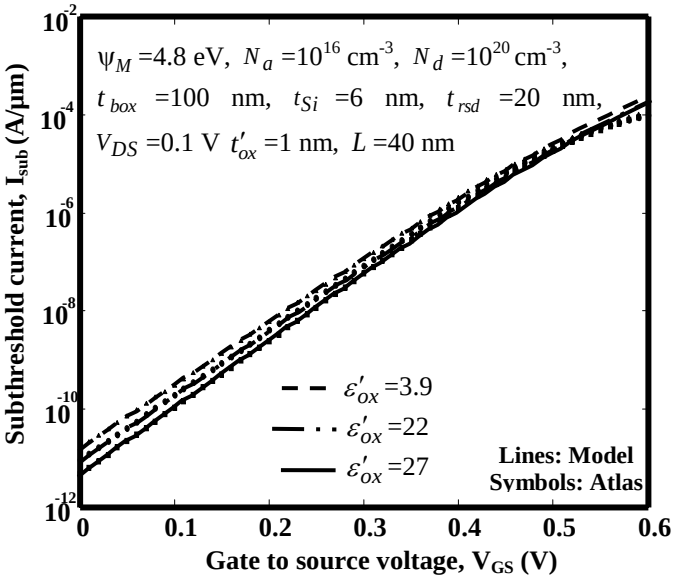


Figure 4. Subthreshold current versus gate to source voltage for gate dielectric constant.

## V. CONCLUSION

A subthreshold current model for short-channel recessed-source/ drain (Re-S/D) SOI MOSFETs with high k dielectric has been presented in this paper. The virtual cathode potential has been used to formulate the subthreshold current model. It is found that the proposed model is valid for a wide variations in the device parameters. Further, the authenticity of the model is verified by comparing the model results with the simulation results which are obtained from the ATLAS™, a two dimensional device simulator from SILVACO.

## ACKNOWLEDGMENT

One of the authors, Dr. Pramod Kumar Tiwari acknowledges financial support from Science and Engineering Research Board (SERB), Department of Science and Technology (DST), Govt. of India, under the fast track scheme for young scientists. The grant number is SB/FTP/ETA-415/2012.

## REFERENCES

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", Proc. IEEE, Mar. 2001, vol. 89, pp.259 - 288 doi:10.1109/5.915374

[2] International Technology Roadmap for Semiconductors (2012).

[3] W. Ke, X. Han X, D. Li, X. Wang, T. Zhang, R. Han, S. Zhang, "Recessed source/drain for sub-50nm UTB SOI MOSFET", Semicond Sci. Technol. vol. 22, Apr. 2007, pp. 577-583.

[4] B. Svilic˘ic, V. Jovanovic´, T. Suligoj, "Analytical models of front- and back-gate potential distribution and threshold voltage for recessed source/drain UTB SOI MOSFETs". Solid-State Electronics, vol. 53, May 2009, pp. 540-547 .

[5] A. Kumar, P. K. Tiwari, "A threshold voltage model of short-channel fully-depleted recessed-source/drain (Re-S/D) UTB SOI MOSFETs including substrate induced surface potential effects", Solid-State Electronics, vol. 95, May 2014, pp. 52-60.

[6] B. Svilicic, V. Jovanovic, T. Suligoj, "Analysis of subthreshold conduction in short channel recessed source/drain UTB SOI MOSFETs", Solid-State Electronics, vol. 54, May 2010, pp. 545-551.

[7] G. K. Saramekala, A. Santra, M. Kumar, S. Dubey, S. Jit, P. K. Tiwari, "Analytical subthreshold current and subthreshold swing models of short-channel dual-metal-gate (DMG) fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs", J. comput. Electron. vol. 13, Feb. 2014, pp. 467-476.

[8] E. Suzuki, K. Ishii, S. Kanemaru, T. Maeda, T. Tsutsumi, T. Sekigawa, K. Nagai and H. Hiroshima, "Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs", IEEE Trans. Electron. Devices, vol. 47, Feb. 2000, pp. 354-359.

[9] G. D. Wilk, R. M. Wallace, J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations", Applied Phys. vol. 89, May 2001, pp. 5243-5275.

[10] M. J. Kumar , S. K. Gupta, V. Venkataraman, "Compact modeling of the effects of parasitic internal fringe capacitance on the threshold voltage of high- k gate-dielectric nanoscale SOI MOSFET", IEEE Trans. Electron Devices, vol. 53, Apr. 2006, pp. 706 -711.

[11] A. Dey, A. Chakravorty, N. DasGupta, A. DasGupta, "Analytical Model of Subthreshold Current and Slope for Asymmetric 4-T and 3-T Double- Gate MOSFETs". IEEE Trans. Electron Devices vol. 55, Dec. 2008, pp. 3442-3449.

[12] ATLAS manual: Silvaco Int. Santa Clara (2008)