Design of High Speed Sense Amplifier for SRAM

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***Abstract*— 1kb static random access memory (SRAM) is designed and tested for correct read and write operation. Novel Sense Amplifier (SA) circuit for 1kb SRAM are presented and analysed in this paper. Sense amplifier using decoupled latch with current controlled architecture is proposed and compared with Current controlled latch SA using 90nm CMOS technology. Delay and power dissipation in proposed SA is 21.5% and 18.5% less than that of current controlled SA. The maximum operating frequency of the SRAM is found as 1.25GHz**.

Index Terms– Sense Amplifier, SRAM architecture, current controlled SA, Cache memory.

I. Introduction

SRAM is used as Cache memory which is very fast and used to speed up the task of processor and memory interface. With the recent advances in VLSI technology, processor clock rates have increased intensely. To be able to take advantage of these high clock rates, the processor must be provided with instructions and data with little or no delay. A very large bandwidth is therefore necessary for both instructions and data. However, while the speed of the logic gates has increased substantially with improvements in VLSI technology, memory access times have not improved proportionally since memory densities have also increased simultaneously. Therefore, SRAM memories have become very important in realizing high-speed computers.

Larger sized on-chip caches are required for future high-performance microprocessors and for system-on-chip (SoC) implementations. These large sizes are made up by the small SRAM memory blocks which respond to very high frequency. Sense amplifier is essential element in all SRAM memory block which respond to very high frequency. Access time and power consumption of memories is largely determined by sense amplifier design.

The sense amplifier (SA) is one of the most important peripheral circuits in memory devices. Although many types of SAs have been developed, the latch-type SA is the most popular because of its high sensing speed and low power consumption [5]. Many sense amplifiers are activated in the on chip memories to achieve a wide internal data bus. The on chip memories and interface circuits consume a large portion of the total power. Therefore, low-power sense amplifiers are necessary in high-performance VLSI's [1] [3]. To respond high frequency, SRAM peripheral circuit needs to be very fast, high performance sense amplifier is a key to achieve a high-speed SRAM [2]. Comparative Study of Various Latch-Type Sense Amplifiers [4] gives comparison in voltage mode and current mode sense amplifiers also.

This paper will describe the design of high speed low power sense amplifier design using decoupled latch and current controlled architecture and simulation results for the same and comparison with existing sense amplifier. The remainder of this paper is organized as follows. Section II, design of high speed low power sense amplifier. Application of proposed sense amplifier to 1kb 1.25 GHz SRAM memory in section III. In Section IV, Simulation results for sense amplifier obtained from Cadence tool are presented using 90nm CMOS technology. The conclusion will be in Section V.

II. Sense Amplifier Design

Sense amplifier (SA) is an important component in memory design. The design and choice of a sense amplifier outlines the robustness of bit line sensing, impacting the read speed and power. The primary function of a SA in SRAMs is to amplify a small differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. A SA allows the SRAM cells to be small, as each individual cell does not required to fully discharge the bit line, hence array area is less. The minimal bit line differential which is input to SA is called as SA margin, is a factor in defining the total read access time and thus, the speed of an SRAM. On the other hand, the subsequent better tolerance to the process and environmental fluctuations comes at the cost of the extra read access time and the power spent on the discharging and precharging of the bit lines.

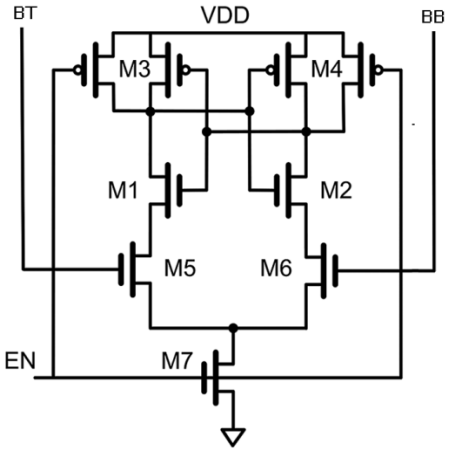

Fig.1. Current-controlled latch sense amplifier [1]

The power problem is one of the most serious limitations in high-performance VLSI's and battery backed-up systems. Power dissipation of high-performance VLSI's has been increasing in proportion to the operation speed. The on chip memories and interface circuits consume a large portion of the total power. Therefore, low-power sense amplifiers and interface circuits are necessary in high-performance VLSI's. To realize a low-power and an automatic power-saving scheme, the current-controlled latch sense amplifier is developed [1] (Fig. 1). In a read cycle, the data of a memory cell appear as a small difference on the data lines (BT and BB). The gates of two NMOSFET's (M5 and M6) are connected to BT and BB. The current flow of M5 and M6 controls the serially connected latch circuit. A small difference between the current through M5 and M6 converts to a large output voltage.

Sense enable EN starts the sense operation by turning on M7. After EN is activated, the operation current flows during the transition of output nodes. The current flows only during switching of inverters that compose the latch sense amplifier. Therefore, the current flow stops automatically in the sense amplifier, and this sense amplifier does not dissipate static power in a read operation. Moreover, the current flow of the latch circuits is small, because the latches of this current controlled latch sense amplifier do not directly drive BT and BB with a large load capacitance.

To further improve the performance and power dissipation, we have proposed a current controlled latch SA with decoupled transistors as shown in Fig. 2. Decoupled transistors connect Bit lines to latch when EN signal is deactivated [2]. When EN signal is low, the logic on BT and BB develops on the latch output i.e. differential voltage but it is not get amplified as the transistor M7 is off and therefore same logic retains still EN goes high. Here line having low voltage goes to discharge to ground when EN signal goes high. When EN signal is high decoupled transistors disconnect the BT and BB signals from latch circuit and it act as a current controlled latch as in [1]. Low voltage path is going to discharge after EN goes high therefore it is quicker than current controlled SA to give output and is having less power dissipation. The comparative study of proposed with current controlled latch SA [1] and CMOS current sense amplifier [6] shows the performance and power dissipation improvement of proposed over them.

Fig.5 and Fig.6 shows the Delay comparison of proposed SA with current controlled latch SA [1] and CMOS current sense amplifier [6], it demonstrations that delay in CMOS current sense amplifier [6] is very high for bit line capacitance of 1fF and that's why is not giving output. CMOS current sense amplifier [6] is having very high power dissipation more than 165uW and that's why is not given in comparison of proposed SA with current concrolled latch SA [1] as in Fig.7. Thus the delay and power dissipation for proposed sense amplifier is less than that of latch SA [1] and CMOS current sense amplifier [6]. Delay and power dissipation in proposed SA is 21.5% and 18.5% less than that of current controlled latch SA.

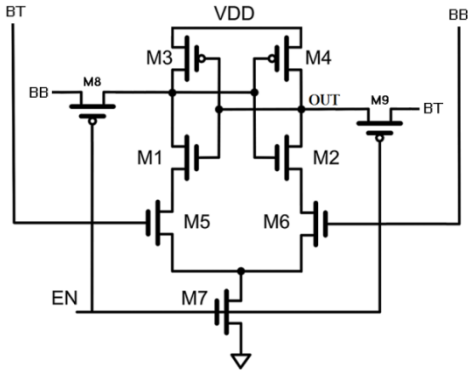

Fig.2. Proposed Sense amplifier with current controlled and decoupled latch

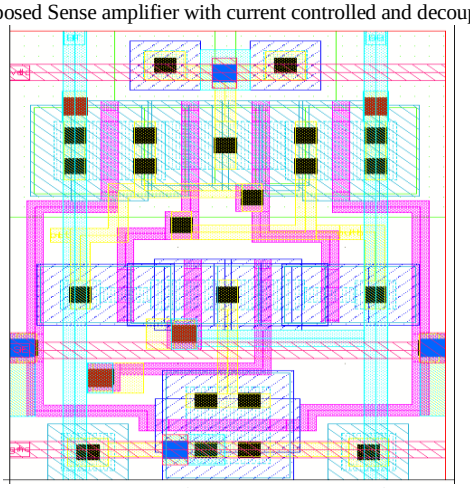

Fig.3. Layout of proposed Sense amplifier

III. Application to 1kb SRAM

Fig. 4 shows the 1-kb SRAM block diagram which includes decoder, sense amplifier, write driver, column mux, precharge circuitry, address latch and read and write control and Input output buffer as the peripheral circuit to the SRAM cell array. The memory core trades performance and reliability for reduction area, memory design relies exceedingly on the peripheral circuitry to recover speed and electrical integrity.

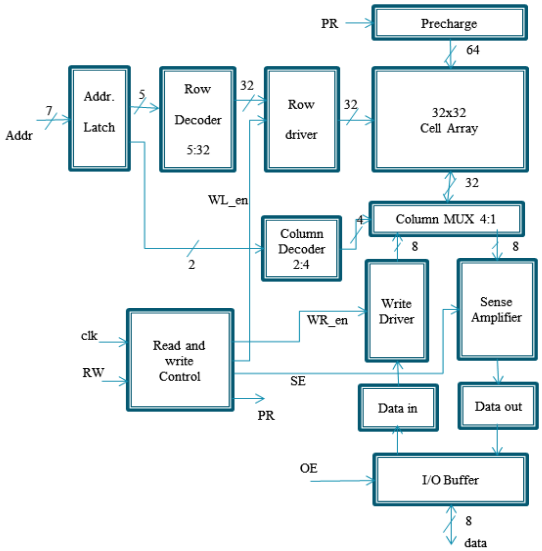

Fig.4. 1-kb SRAM block diagram

We have used proposed sense amplifier for design of 1kb SRAM. During read cycle after word line goes high, bit line or bit line bar starts discharging through selected memory cell and it creates difference on bit and bit line bar, sense amplifier senses that difference and give output as logic 0 or 1. We have used Proposed Sense amplifier with current controlled and decoupled latch which is described in section II for 1-kb SRAM. We have simulated the complete memory with proposed sense amplifier and simulation results are given in section IV for the same.

IV. Simulation Results

Sense Amplifier:

Fig.5 and Fig.6 shows the Delay comparison of proposed SA with current controlled latch SA [1] and CMOS current sense amplifier [6]. It shows the proposed sense amplifier is having less delay and power dissipation compared to current controlled latch SA [1] and CMOS current sense amplifier [6]. Fig.5 shows delay comparison of proposed SA with current SA [6] and current controlled latch SA [1] for different SA margin and bit line capacitance of 1pF, here for every SA margin proposed SA have smallest delay compared to others, similarly in Fig.6 delay comparison of proposed SA with current SA [6] and current controlled latch SA [1] for different bit line cap and SA margin of 100mV is given where proposed have smallest delay.

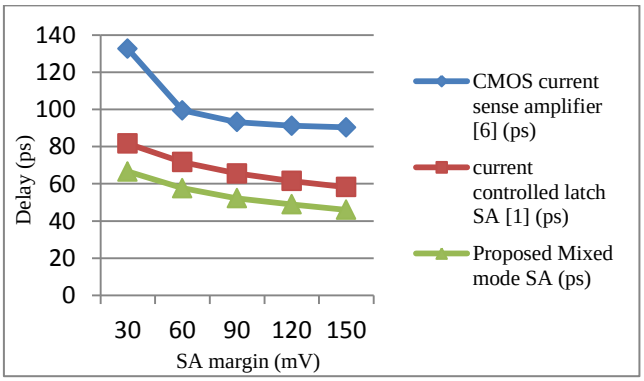

Fig.5. Delay comparison of proposed SA with current SA [6] and current controlled latch SA [1] for different SA margin and BL cap = 1pF.

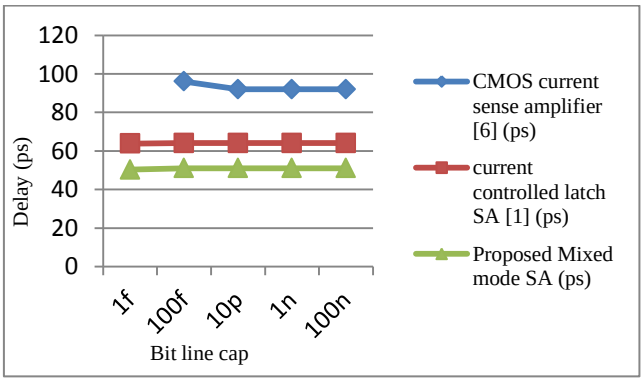

Fig.6. Delay comparison of proposed SA with current SA [6] and current controlled latch SA [1] for different bit line cap and SA margin = 100mV.

Fig.7 gives the power consumption comparison of proposed SA with current controlled latch SA [1] for different SA margin and bit line capacitance of 1pF, here proposed SA is having less power dissipation for every sense amplifier margin from 30mV to 150mV.

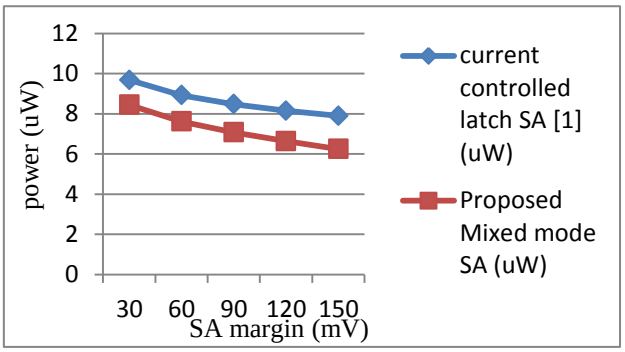

Fig.7. Power consumption comparison of proposed SA with current controlled latch SA [1] for different SA margin and BL cap = 1pF.

Table I gives the results for corner analysis where the largest delay is found out for SS case and it is 75.81ps whereas the smallest is for FF case and it is 38.06ps.

TABLE I
CORNER ANALYSIS

	Delay (ps)
NN	51.08
SS	75.81
SF	73.71
FS	38.70
FF	38.06

Monte Carlo Analysis:

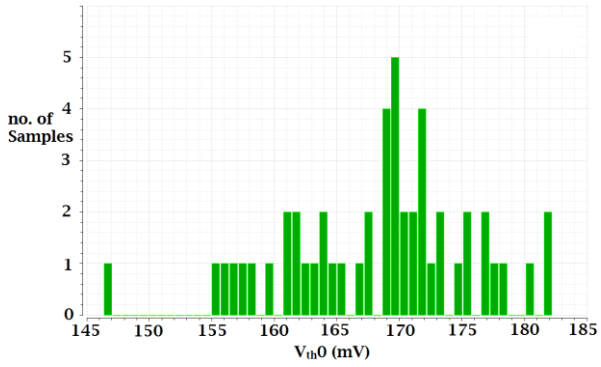

Fig.8. V_{th} Variation for Monte Carlo simulation

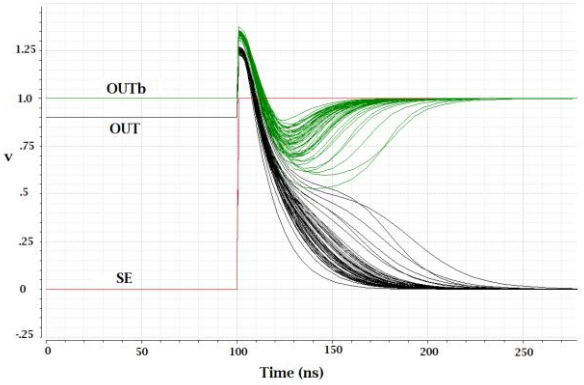

Fig.9. Monte Carlo simulation output for proposed sense amplifier with sense amplifier margin of 100mV.

Monte Carlo simulation is carried out for 50 steps with threshold voltage variation as shown in Fig.8 and the output of sense amplifier is given in Fig.9, output shows that for every case sense amplifier is giving correct output with maximum delay of 93ps.

1kb SRAM

Fig.10 shows the read cycle, here SA margin is 100mV, time to make SA margin on bit and bit bar line is 41ps, after world line goes active, after 41ps sense enable signal go high and sense amplifier takes 57ps to give output. Read cycle takes 730ps to complete read operation from address latching to output available. Fig. 11 shows write operation, after WL goes high, point of cross section of logic change occur after 70ps and complete logic change after 170ps. Write cycle takes 800ps to complete write operation. The maximum access time is 800ps. Therefore the frequency on which SRAM can work comfortably is 1.25 GHz.

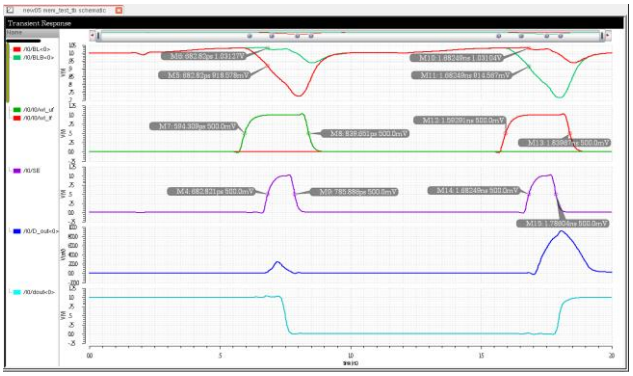

Fig.10. 32x32 SRAM Read cycle

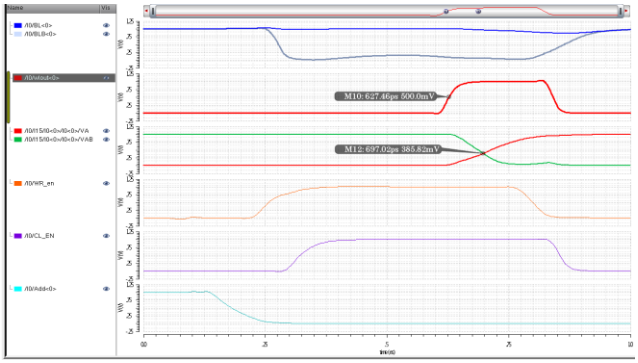

Fig.11. 32x32 SRAM Write cycle

V. Conclusion

Static random access memory (SRAM) is designed with its peripheral blocks to achieve operation of frequency 1.25 GHz. Sense amplifiers with decoupled latch and current controlled logic is designed. As the voltage available and need be discharge to ground is less than supply voltage ,it is having improvement over current controlled latch sense amplifier in terms of power dissipation and performance.

Sense amplifier is the essential components in fast SRAM. Proposed sense amplifier is used to develop a 1-kb 8-bit 1.25-GHz SRAM Memory.

References

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