# FPGA Implementation of Digital PI Controller on Control Strategy of DSTATCOM for Power Quality Improvement

Gokulananda Sahu
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela, India
gokulanandasahu@gmail.com

Kamalakanta Mahapatra
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela, India
kmaha2@gmail.com

*Abstract*—**The proliferation of power electronics-based industrial and domestic equipment which has degraded the power quality in power distribution networks due to non-linear load impedance. The Distribution STATic COMpensator (DSTAT-COM) has proved to be a useful custom power device to eliminate harmonic components and to compensate reactive power for balanced/unbalanced linear/nonlinear loads. This paper presents a novel control strategy to calculate the reference compensation current of three phase DSTATCOM under distorted utility condition at instantaneous state. In this proposed approach a digital PI controller has been implemented on FPGA to make the process faster and enable the design to be independent of process technology. The performance of the system simulated in Matlab Platform and evaluated considering the source current total harmonic distortion. The VHDL design has been implemented using ISE10.1 tool from Xilinx. This is tested on a board with hardware configuration such as FPGA - XC2VP4 with on chip PowerPC-405 Processor, ADC AD9240-14 bit 10MSPS analog input channel, DAC AD7541-12-bit of conversion time–100ns with System clock 40 MHz.**

***Keywords—Field programmable gate Array;Distribution Static Compensator;proportional integral controller.***

## I. INTRODUCTION

During the last decade, there has been sudden increase in the nonlinear load (Computers, Laser printers, SMPS, Rectifier, Cyclo-converters etc.), which degrades the power quality causing a number of disturbances e.g. heating of home appliances, noise etc., in power systems[1][2] due to harmonics.

To compensate the harmonics due to nonlinear load, a custom power device DSTATCOM is used [3]. The performance of DSTATCOM largely depends on the control strategies used for reference current extraction. The control strategy used conventionally, were based on active and reactive power are found unsuitable for unbalanced and distorted utility conditions. Significant contribution for development of control algorithm was made by Budeanu and Fryze[5]. They provide power definition in frequency and time domain and set the pathways for development universal set power definitions which led to the development of p-q theory by Akagi [5][6].

Implementation of digital PI controller has gone through several stages of evolution, from the early mechanical and pneumatic designs to the microprocessor based systems but these systems have the drawback of demanding control requirements of modern power conditioning systems which will overload most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms. Recently, Field Programmable Gate Arrays (FPGA) has becoming alternative solution for the realization of digital control systems. The FPGA based controllers offer advantages such as high speed computation, complex functionality, real time processing capabilities and low power consumption [9][10]. In this paper we consider discrete time PI controller and is implemented in a dedicated FPGA. Following the standard digital design practices, the controller functionality is described in Very High Speed Integrated Circuit Hardware Description Language (VHDL). Using synthesis tool, the design is then targeted to the FPGA board.

In this paper performance of proposed control strategy is investigated in **three phase three wire system** for balanced/distorted source and non-linear balanced /unbalanced Load for mitigation of harmonics and compensation of reactive power with digital PI controller which defines the **problem statement.** The measures of the performance is the source current total harmonic distortion

Rest of the paper is organized as follows. In section II system configuration and in section III brief discussion on proposed control strategy is presented. In section IV general structure & FSMD architecture of digital PI controller are presented and in section V the performance indices used for evaluation are discussed. Simulation results are described in section VI. Finally in section VII, conclusion is drawn.

## II. SYSTEM CONFIGURATION

Fig.1 shows the basic circuit diagram of a DSTATCOM [3][7][8] system with non-linear and linear load connected to three phase three wire distribution system. A nonlinear load is realized by using a three phase full bridge diode rectifier. A three phase voltage source converter (VSC) working as a DSTATCOM is realized using six insulated gate bipolar

transistors (IGBTs) with anti-parallel diodes. At ac side, the interfacing inductors are used to filter high frequency components of compensating currents.

The first harmonic load currents of positive sequence are transformed to DC quantities. The first harmonic load currents of negative sequence and all the harmonics are transformed to non-DC quantities and undergo a frequency shift in the spectrum.

The voltage regulator in the converter DC side is performed by a proportional–integral (P-I) controller. Its input is the capacitor voltage error ($v_{dcref}$-$v_{dc}$) and it regulates the first harmonic active current of positive sequence. It is possible to control the active power flow in the VSC and thus the capacitor voltage $V_{dc}$ remains constant.

The dynamics of each VSC are modeled by solving differential equations governing two-level inverter. The switching of the inverter is done by monitoring the reference and actual currents and comparison of error with the hysteresis band of hysteresis controller (HCC) which is most suitable for all the applications due to its unconditioned stability, fast response, good accuracy and easy implementation with minimum hardware. The VSC model is based on discrete switching variables $g_a$, $g_b$, $g_c$ [4].

$$\begin{bmatrix} v_{fa} \\ v_{fb} \\ v_{fc} \end{bmatrix} = \frac{V_{dc}}{\sqrt{3}} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} g_a \\ g_b \\ g_c \end{bmatrix} \quad (1)$$

The *R–L* network on the ac side of the converter is represented by three differential equations.

$$\left.\begin{aligned} L_f \frac{di_{fa}}{dt} &= -i_{fa}.R_f + v_{sa} - v_{fa} \\ L_f \frac{di_{fb}}{dt} &= -i_{fb}.R_f + v_{sb} - v_{fb} \\ L_f \frac{di_{fc}}{dt} &= -i_{fc}.R_f + v_{sc} - v_{fc} \end{aligned}\right\} \quad (2)$$

The dc side equations are defined as

$$i_{dc} = g_a.if_a + g_b.if_b + g_c.if_c \quad (3)$$

$$-C_{dc}.\frac{dv_{dc}}{dt} = i_{dc} \quad (4)$$

The equation for discrete PI controller is defined as

$$u(n) = u(n-1) + k_p\{e(n) - e(n-1)\} + k_i e(n) \quad (5)$$

Where u(n)= PI controller output, e(n)=$V_{dcref}$-$V_{dc}$ , $K_p$ = Proportional gain constant and $K_i$= Integral constant of PI Controller. The equation of HCC is defined as

If $i_{fk} < (i^*_{fk} - hb)$

$g_k$=1

end

If $i_{fk} > (i^*_{fk} + hb)$ (6)

$g_k$=0

end

Where k= phase a, b and c.

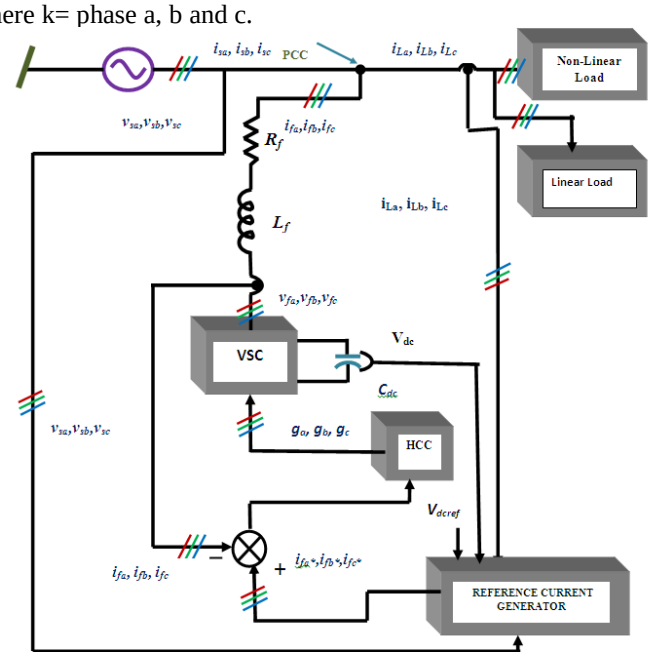


Fig.1 system configuration of DSTATCOM

## III. PROPOSED CONTROL STRATEGY

This control strategy is best suitable for distorted utility condition. It is based on instantaneous symmetrical component theory in instantaneous state. The main objective to find out active fundamental source peak current.

The reference compensating current is equal to the difference between estimated source and load current.Fig.2 shows the control structure of proposed controller. The peak source current is estimated as

$$I_{sm1} = \frac{p_{3\phi}}{3V_m^+} \quad (7)$$

Prime objective is to make source current balanced.

$$i_a + i_b + i_c = 0 \quad (8)$$

Let formulate all powers in time domain. Zero sequence, positive sequence and Negative sequence complex power are denoted as $s_0$, $s_+$ and $s_-$ . The real power of zero sequence ,positive sequence and negative sequence are denoted as $p_0$,$p_+$ and $p_-$. The imaginary power of zero sequence, positive sequence and negative sequence are denoted as $q_0$,$q_+$ and $q_-$ .The instantaneous voltage and current of zero sequence ,positive sequence and negative sequence are denoted as $v_0$,$v_+$ ,$v_-$ and $i_0$,$i_+$,$i_-$ respectively. Let zero sequence power is formulated as

$$\left.\begin{aligned} s_0 &= 3v_0 i_0^* = p_o + jq_0 \\ p_0 &= \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c) \\ q_0 &= 0 \end{aligned}\right\} \quad (9)$$

Let calculate the positive sequence power.

$$\left.\begin{aligned} s_+ &= 3v_+ i_+^* = p_+ + jq_+ \\ p_+ &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c)\right] \\ q_+ &= -\frac{1}{2\sqrt{3}}\ v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b) \end{aligned}\right\} \quad (10)$$

Let calculate the negative sequence power.

$$\left.\begin{aligned} s_- &= 3v_- i_-^* = p_- + jq_- \\ p_- &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c)\right] \\ q_- &= \frac{1}{2\sqrt{3}}\ v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b) \end{aligned}\right\} \quad (11)$$

Where total Instantaneous active power is defined as

$$s = (s_0 + s_+ + s_-) = (p_0 + p_+ + p_-) = p_{3\phi} = (v_a i_a + v_b i_b + v_c i_c) \quad (12)$$

In equation (12) putting $i_a+i_b+i_c=0$ , We get

$$\frac{p_{3\phi}}{2} = p_+ = \frac{3V_{m1}^+}{\sqrt{2}}\frac{I_{sm1}^+}{\sqrt{2}} \quad (13)$$

$$I_{sm1}^+ = I_{sm} = \frac{p_{3\phi}}{3V_{m1}^+} \quad (14)$$

So

$$\left.\begin{aligned} i_{sk}^* &= i_{skref} = I_{sm} U_{k1} \\ i_{fk}^* &= i_{fkref} = i_{Lk} - i_{skref} \end{aligned}\right\} \quad (15)$$

Where k=a, b, c and Uck1 is fundamental unit vector template.

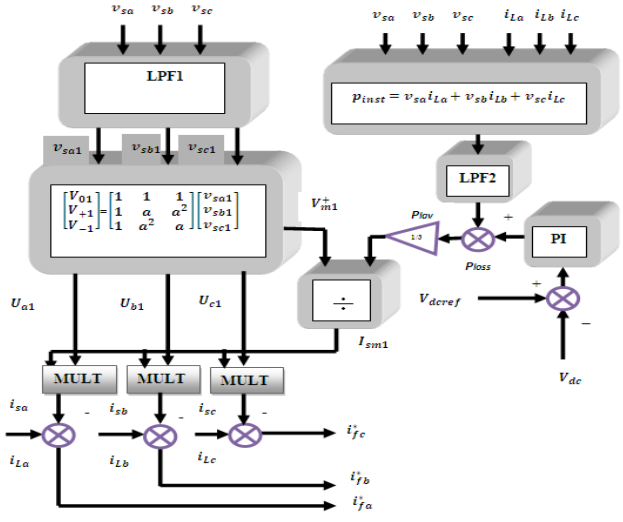


Fig.2 Control structure of proposed algorithm

Fig.2 shows the basic control structure of proposed algorithm which constitutes one PI controller; low pass filters (LPF1 and LPF2) and arithmetic calculators. The average power $p_{lav}$ is calculated by adding PI output ($P_{loss}$) to LPF2 output. LPF1 is used to extract the fundamental from distorted PCC (point of common coupling) voltage.

## IV. DIGITAL PI CONTROLLER

### A. *General Structure*

The PI controller is derived from the generic PID controller equation. The PID(proportional-integral-derivative) controller is expressed as:

$$u(t) = k_p\left[e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{d}{dt}e(t)\right] \quad (16)$$

$K_p$=proportional gain, $T_i$=integral time constant, $T_d$=derivative time constant. The above equation is described for small sampling time T to be implemented by digital system.The differential equation is given by:

$$u(n) = k_p\left[e(n) + \frac{T}{T_i}\sum_{j=0}^{n} e(j) + \frac{T_d}{T}[e(n) - e(n-1)]\right] \quad (17)$$

Where $K_i=k_pT/T_i$ inttegral coefficient, $K_d=k_pT_d/T$ derivative coefficient. To derive the recursive algorithm first calculate u(n-1).

$$u(n-1) = k_p e(n-1) + k_i\sum_{j=0}^{n-1} e(j) + k_d[e(n-1) - e(n-2)] \quad (18)$$

Then calculating the correction term as:

$$\Delta u(n) = u(n) - u(n-1) \quad (19)$$

$$(\Delta u(n) = k_0 e(n) + k_1 e(n) + k_2 e(n-2) \quad (20)$$

Where

$$\left.\begin{aligned} k_0 &= k_p + k_i + k_d \\ k_1 &= -k_p - 2k_d \\ k2 &= k_d \end{aligned}\right\} \quad (21)$$

The control output is calculated as:

$$u(n) = u(n-1) + \Delta u(n) \quad (22)$$

$$u(n) = u(n-1) + k_0 e(n) + k_1 e(n-1) + k_2 e(n-2) \quad (23)$$

For PI controller $k_d=k_2=0$, Putting the value of $k_0$, $k_1$, $k_2$in equation (22) we get:

$$u(n) = u(n-1) + (k_p + k_i)e(n) + (-k_p)e(n-1) \quad (24)$$

$$u(n) = u(n-1) + C_1 e(n) + C_2 e(n-1) \quad (25)$$

Where $C_1=k_p+k_i$ and $C_2=-k_p$.

$$u(n) = u(n-1) + k_p\{e(n) - e(n-1)\} + k_i e(n) \quad (26)$$

*B. FSMD architecture of PI Controller*

FSMD architecture implements the FSMD model by combining a controller with a data path which is depicted in Fig.3.

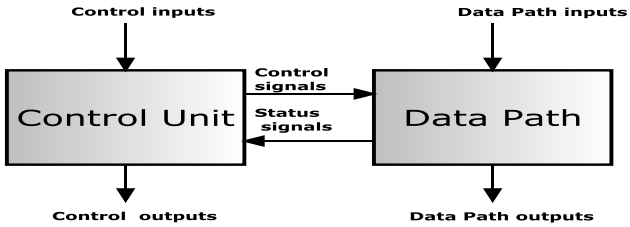


Fig.3 FSMD high level block diagram

The behavior of the PI Controller is deduced in data flow graph (DFG) which is illustrated in Fig.4. Thus, we have chosen to work on 14 bit signed integer coding and thousandth order of precision.

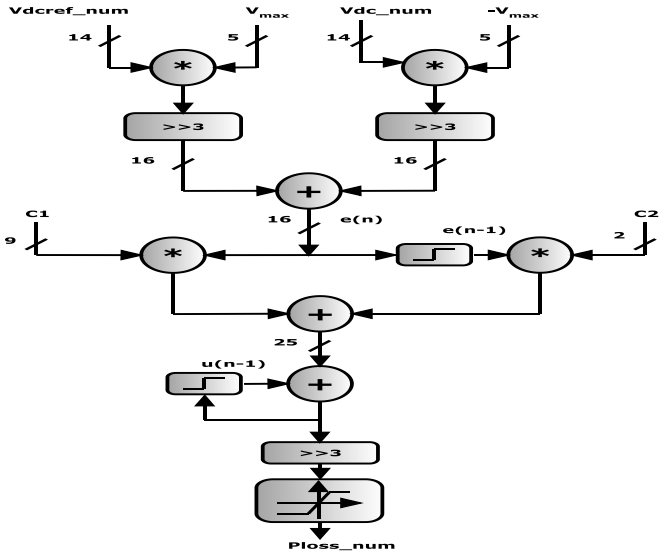


Fig.4 DFG of PI controller

For the given system, there are several FSMD architectures that are different by their implementation results. In our application case, we have developed space optimized FSMD architecture. The command computing is carried out in a sequential way and the operators are implemented in the data path with multiple operator structure.

Fig.5 shows data path unit structure adapted for a PI controller. According to the control signals, this unit allows restoring external data inputs and outputs results, to generate command value and to keep it at output.

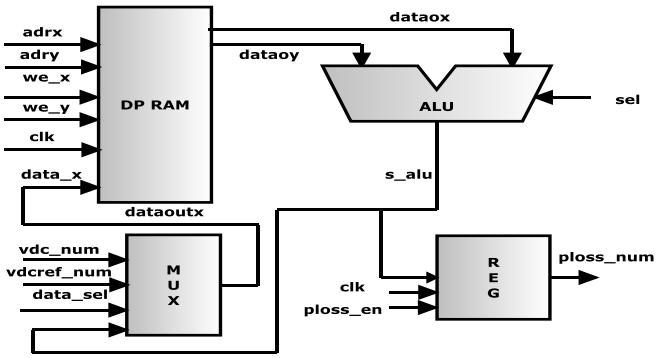


Fig.5 Data path structure

The Fig.6 depicts the control unit with states. In this figure the FSMC (Finite State Machine controller) provides control signals to the data path and data path provides status signals to the FSMC. The data path consists of RAM, ALU, MUX and RESISTER which accepts the input signals. The FSM controller operates on 28 states for calculating the ploss_num. The computations of the following stages are carried out.

Acquisition:

.$V_{dcref}$ and $V_{dc}$ are loaded from the corresponding registers for write operation.

Calculation:

For each calculation one state is used to read operands and select operators. Then one other state is used to save the result in DP RAM. At the end of this stage ploss_num is loaded on the register REG.

Update:

State transition has been occurred at the edge of FSMC clock signal. Initial state INIT from which the machine can be turned on when it is on rest (start='0') or on reset (reset='1').For normal operation it has to carry $S_o$ to $S_{27}$

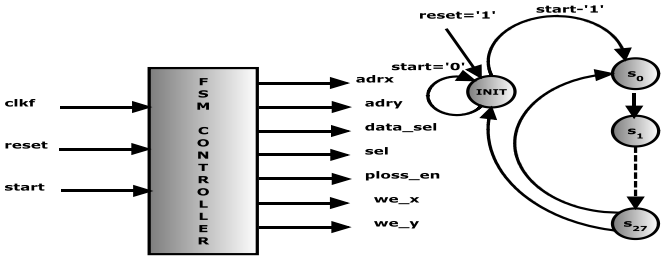


Fig.6 Control Unit with States

## V. PERFORMANCE INDICES

*A. Total harmonic distortion*

The total harmonic distortion (THD) [11] is used to define the effect of harmonics on the power system voltage. It is used in low-voltage, medium-voltage, and high-voltage systems. It is expressed as a percent of the fundamental and is defined as

$$THD(voltage) = \frac{\sqrt{\sum_{h=2}^{50} V_h^2}}{V_1} * 100\% \quad (26)$$

$$THD(current) = \frac{\sqrt{\sum_{h=2}^{50} I_h^2}}{I_1} * 100\% \quad (27)$$

According to IEEE-519 the permissible limit for distortion in the signal is 5%.

## VI. RESULTS AND DISCUSSION

To investigate the performance of the DSTATCOM for proposed control strategy, simulations are performed on matlab platform. A three phase three wire distribution system with parameters given below is considered for simulation.

### *A. System Parameters:*

Supply voltage: 50Vrms (L-N), 50Hz, three phase balanced
Source impedance: Rs=0.1Ω, Ls=0.5mH
Nonlinear load: Three phase full bridge diode rectifier with load ( L=10mH,$R_L$=3.7Ω)
DC storage Capacitor $C_{dc}$=2000μF
Interface inductor $L_f$=5mH , $R_f$=0.1Ω
DC Link voltage $V_{dc}$=100V
Hysteresis band hb=0.25A
Unbalanced Linear load: $Z_a$=67+j31.42Ω , $Z_b$=37+j18.55Ω, $Z_c$=28.5+j12.56Ω

### *B. Design specification of Digital PI Controller:*

Controller sample time: 0.05ms
Input data length: 14 bits
Output data length: 12 bits
PI regulator parameters: $K_{pr}$=1.0259,$K_{ir}$=227.9288
Arithmetic: fixed point
The performance of the proposed control strategy is evaluated based on three different cases.
Case1- Balanced Source and balanced Non-Linear load
Case2- Balanced Source and Unbalanced Non-linear load.
Case3- Balanced distorted Source and Unbalanced Non-linear load.

In **case 1** the source is assumed to be sinusoidal and balanced whereas the load is considered as non-sinusoidal and balanced with load as six pulse diode full bridge rectifier. Before compensation the THD of load current is found to be **23.2361%.** After compensation the THD for proposed control strategy is listed in the T**able1.** In **case 2** the source is balanced and sinusoidal but the load is unbalanced non – sinusoidal (load current harmonic is found to be **22.2914%)** .The THD of the load current for phase **a** after compensation is summarized in **Table1.**The results demonstrated here are considered for phase-a only. In **case 3** the source is balanced and distorted (**distorted** voltage source harmonic is **13.7477%)** but the load is unbalanced non sinusoidal (load current harmonic is found to be **22.2914%)** . The THD of the load current for phase **a** after compensation is summarized in **Table 1.**The results demonstrated here are considered for phase a only.

### *C. Case 3 Proposed control strategy simulation*

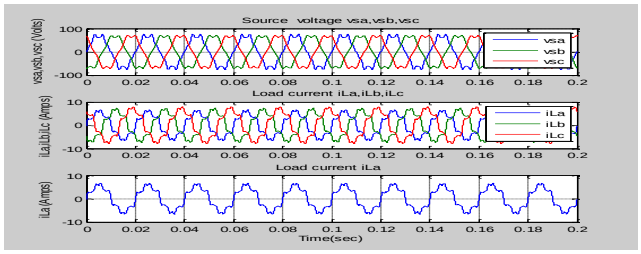


Fig.7a Balanced distorted source voltage,Unbalanced Load current, Phase a Load current

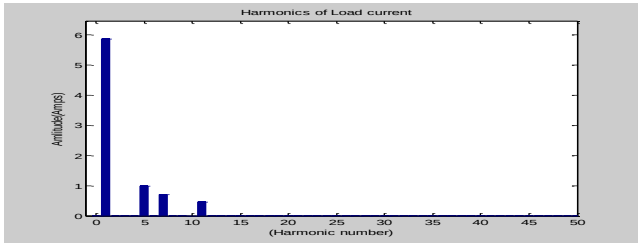


Fig.7b Harmonics of Load current of Phase a

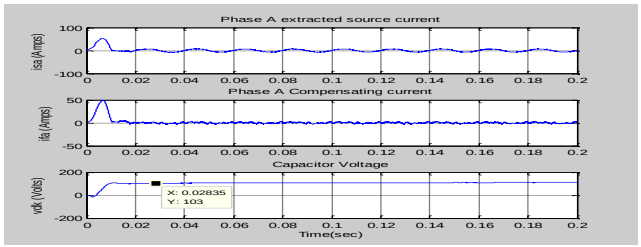


Fig.7c Phase A extracted Source current, Compensating Current and DC link Capacitor Voltage

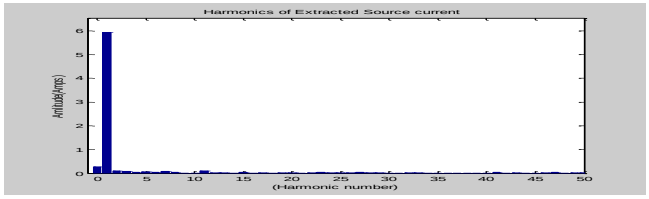


Fig.7d Harmonics of extracted Source current

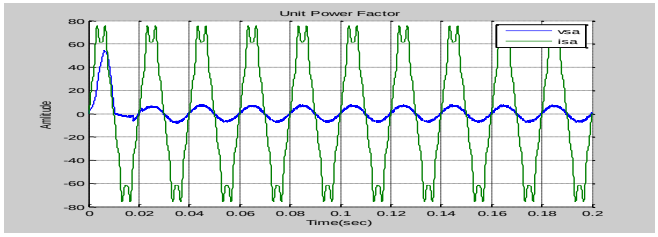


Fig.7e Unit power factor of compensated load

Fig.7 (a, b, c, d, e ) shows the dynamic performance of the system.

Table 1. THD% of extracted source current

| **Control strategy** | **THD(%) of Extracted source current** | | |
|---|---|---|---|
| | CASE-1 | CASE-2 | CASE-3 |
| PROPOSED | 3.6914 | 4.2566 | **4.7217** |

### D. *Simulation of Digital PI Controller*

Fig.8a shows the RTL schematic of digital PI controller which works as per the DFG. The capacitor voltage vdc_num (data(13:0)) is the output of ADC fed to data path unit and stored in DPRAM at state $s_0$.After execution of all 28 states the ploss_num is obtained and fed to the DAC. Fig.8b shows the internal structure of TOP module which includes REG, RAM, MUX,ALU, FSMC interface with ADC module.Fig.8c shows the output of FSM controller.

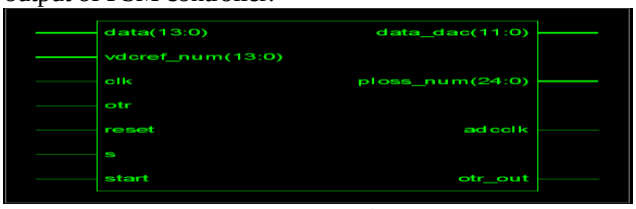


Fig.8a RTL Schematic of Top module

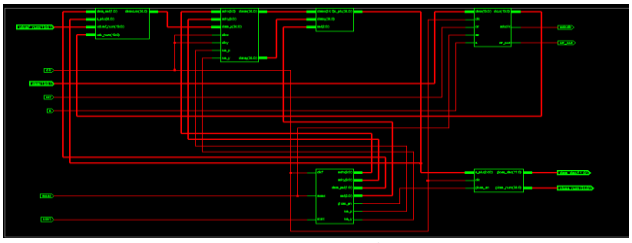

Fig.8b Internal structure of Top module

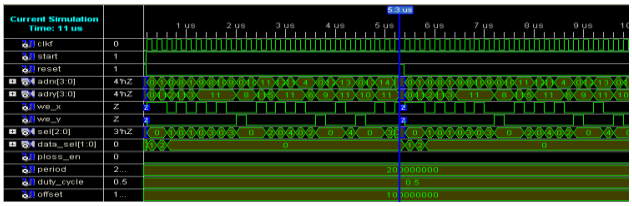


Fig.8c FSM controller output

### E. *Implementation Result*

The design is implemented in VHDL using ISE10.1 tool from Xilinx. The testing board has hardware configuration such as FPGA - XC2VP4 with on chip PowerPC-405 Processor, ADC - 14 bit, 10MSPS analog input channel is available using AD9240, DAC - One channel, using 12-bit DAC, AD7541of conversion time – 100ns with System clock 40 MHz, DSO and Signal Generator. Fig.9 shows the resource utilization indicates the area consumed in FPGA.

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slices | 194 | 3008 | 6% |
| Number of Slice Flip Flops | 160 | 6016 | 2% |
| Number of 4 input LUTs | 365 | 6016 | 6% |
| Number of bonded IOBs | 72 | 348 | 20% |
| Number of MULT18X18s | 2 | 28 | 7% |
| Number of GCLKs | 3 | 16 | 18% |

Fig.9 Device utilization summary

## VII. CONCLUSION

In all cases it is observed that proposed control strategy is working fine and able to compensate the nonlinear unbalanced load successfully. The THD obtained here are within the limit of 5% prescribed by IEEE 519. The digital PI controller has been implemented successfully on FPGA

## REFERENCES


[1] Rose, Francisco C. De La, "*Harmonics and Power Systems*," New York, Taylor & Francis Group, LLC, 2006.

[2] S.B. Karanki,N. Geddada,M.K. Mishra,B.K. Kumar.,"A DSTATCOM Topology With Reduced DC-Link Voltage Rating for Load Compensation With Non stiff Source" *IEEE Trans.Power Electronics*, vol. 27, no. 3, pp. 1201–1211,2012.

[3] A. Moreno-Munoz,"*Power Quality: Mitigation Technologies in a Distributed Environment"*. London, U. K.: Springer-Verlag, 2007.

[4] Rahmani, S., Al-Haddad, K., Fnaiech, F. (2002). A New PWM Control Technique Applied to Three-Phase Shunt Hybrid Power Filter. Proceedings of International Conference on Industrial Electronics IECON'02, Seville Spain, Vol. 1, pp. 727–732,2002.

[5] H. Akagi, E. H. Watanabe, and M. Aredes," *Instantaneous Power Theory and Applications to Power Conditioning"*, Hoboken, NJ: Wiley, 2007.

[6] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensator comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.* , vol. IA-20, no. 3, pp. 625-630,Mar. 1984.

*[7]* Gokulananda Sahu, Kamalakanta Mahapatra,"Comparison of control strategies of DSTATCOM for non-linear load compensation."*ACEEE conf. CIIT-2013,pp.27-35,2013.*

*[8]* G. Sahu,K. Mahapatra ,"Real time implementation of digital filter on control strategy of DSTATCOM for load compensation under distorted utility condition."*IEEE Conf. PrimeAsia, pp.164-169,2013.*

[9] Y.F. Chan, M. Moallem, W. Wang, "Efficient Implementation of PID Algorithm Using FPGA Technology" *Proc. Of 43rd EEE Conference on Decision and Control,*, Atlantis, pp. 4885-4890, 2004.

[10] D.D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, and S. Zhao,"*SpecC: Specification language and methodology*," Kluwer Academic Publishers, CECS, 2001.

[11] IEEE Recommended Practices and Requirements /or Harmonic Control in Electrical Power Systems, *IEEE Standard 519*, 1992.


**Gokulananda Sahu** received Bachelor of Engineering in Electronics from Marathawada Universiy,Aurangabad, Maharashtra in 1993 & M.Tech in VLSI Design and Embedded system in 2010 from National Institue of Technology ,Rourkela Odisha.He has 17 years of teaching and research experience. He has been serving as a research Scholar in the Department of Electronics and Communication Engineering, NIT Rourkela since 2012. His research interests include Power Quality, Power Electronics ,VLSI design, Embedded System, FPGA based System design and wireless Communication.

**Kamalakanta Mahapatra** received B.Tech degree with Honours in 1985 from University of Calicut, Master's in 1989 from Sambalpur University and Ph.D from Indian Institute of Technology, Kanpur in the year 2000 in Electrical Engineering .Currently, he is a Professor in the Electronics and Communication Engineering Department of National Institute of Technology Rourkela; he assumed this position since February 2004. He is a Fellow of the Institution of Engineers (India), His research interest includes Power Electronics, Embedded Systems, Electronic Circuits, FPGA based System design and VLSI Design.