# Process Corner Variation Aware Design of Low Power Current Starved VCO


Prakash Kumar Rout[1]
Dept. Electronics and Communication Engineering
Silicon Institute of Technology
Bhubaneswar, India
[1]Prakashrout05@gmail.com

D.P.Acharya[2]
Dept. Electronics and Communication Engineering
National Institute of Technology
Rourkela, India
[2]d_p_acharya@rediffmail.com

Ganapati Panda[3]
Dept. Electronics and Communication Engineering
Indian Institute of Technology
Bhubaneswar, India
[3]ganapati.panda@gmail.com

Debasish Nayak[4]
Dept. Electronics and Communication Engineering
National Institute of Technology
Rourkela, India
[4]nayak.debasish84@gmail.com



***Abstract*— Conventionally the integrated circuit designer first carries out the design to achieve the required performance specifications and observes the worst case performance through simulations. If the worst case performance falls well inside the acceptable range then that design is designated as a process variation tolerant design. In such case the design is not truly robust against actual process variations. The randomness of process variations is hardly included in the design phase to minimize their effects on the performance of the fabricated chips. In the present work a novel approach is proposed in which minimizes the process corner performance variation (PCPV) so that the performances of the extreme corner case chips are very close the nominal fabrication case. The nominal case design is also subjected to performance optimization along with the process corner variability. Evolutionary algorithm is suitably employed for simultaneous optimization of all the objectives. The proposed design technique is applied to a CSVCO circuit as a case study and the performance improvement results of Cadence simulation are reported.**



***Index Terms*–** Process Corner Performance Variation (PCPV), Low Power Analog Integrated Circuits, Current Starved Voltage Controlled Oscillator, Infeasibility Driven Evolutionary Algorithm (IDEA).


## I. INTRODUCTION

The random fluctuation of the parameters of the semiconductor fabrication process influences strongly the performance of integrated circuits. In traditional techniques the designers carry out a performance driven design and subject it to worst case process variations. In this method circuit tolerance to the variation in process are estimated using simulation analysis and the design is said to be process variation tolerant when the performances are found within the acceptable range. This worst case modeling is highly unrealistic in many of the high performance integrated circuits whose performance acceptability range is very narrow. Moreover if in a specified design, the worst case performance does not fall in the acceptable range then the designer has no control over it even if the design offers good performance in nominal process. In such a case designer has to reject that design option. In [1] the worst case modeling is made more realistic by assigning probability to the process corners. A more practical approach to maximize the yield is to minimize the performance variations due to process and environmental fluctuations. The worst case value of the circuit performance variability is minimized and specifications on the nominal value of the performance measures are handled simultaneously in [2]. In the worst case variability minimization technique the standard deviation of the performance is estimated from the Monte Carlo sampling of the noise parameters and the performance optimization is done by gradient techniques like Simplex method and Quadratic Programming method. One novel practical approach of performance optimization of integrated circuits is proposed in this work. It is well known that the probability of having chip being manufactured under normal process environment is higher than the other corner process environments since it follows a Gaussian distribution. In our proposed approach we minimize the process corner performance variability (PCPV) simultaneously with performance optimization. In PCPV the statistical performance deviations of the corner cases from the nominal case is minimized by considering the actual SPICE parameters of different process corners for evaluation of performances. The design proposed here is made **true process corner variation** robust by optimizing the circuit performance in the nominal case and minimizing the difference between chip performances in normal and worst case corner environments.

Optimization methods have been developed [3] for process dependent fluctuation in different circuit performance parameters. In [3] fuzzy set theory is used to construct a single objective function for a weighted combination of different objectives and applied gradient based technique. The choice of weights for competing objectives makes the formulation of such an objective function somewhat ambiguous. In [2] it was single objective gradient based optimization and in [3] though there is a mention regarding multiple objective optimizations but effectively the problem has been solved in a single objective gradient approach. Considering the spirit of [3] and our proposed formulation, a more appropriate way is to use the multiobjective multicriteria optimization techniques. Besides this the use of gradient based optimization approach is inefficient in handling multimodal objective functions for which evolutionary approaches are suitable. In this paper a multiobjective evolutionary technique is used for the optimization of multiple statistically formulated performance process variability objective functions along with the nominal performance objectives simultaneously.

The remaining part of the paper is organized as follows. In Section II we present the proposed robust design methodology along with the formulation of the optimization objectives. The performance analysis of the proposed design technique for a demonstrative example is carried out in Section III. Concluding remarks and suggestions for future research work are provided in Section IV.

## II. Fabrication Process Variation Tolerant Design Technique

### A. Overview of the Technique

The design methodology proposed here makes the integrated circuit robust due to (i) the optimization of the performance measures like power consumption and frequency oscillation under the nominal fabrication conditions and (ii) minimization of the random variability of extreme process performances from the nominal case. The above processes are carried out simultaneously using a multiobjective evolutionary technique. Circuit performance parameters of the nominal (NN) process are subjected to optimization using multiobjective evolutionary algorithm by integrating the SPICE model parameters of the process in the optimization engine. The performance measures like frequency and power of other process corners FF, SF, FS and SS, are computed using respective SPICE model parameters. Their statistical deviations from the NN process circuit model as obtained above form another set of objectives are injected into the same multiobjective evolutionary algorithm in an iterative manner. After the statistical deviations are minimized to meet the specified tolerance limits, the robustified optimal circuit design parameters are extracted for final design. These final design parameters are used for design and verification of the circuit performances in the circuit level. The extensive simulations are carried out using ADE GXL and Assura tools from Cadence.

### B. Objective Functions for Current Starved VCO

In the performance optimization, the objective functions are precisely the performance indices of current starve VCO whose schematic is shown in figure 1. The performance measures are the, power consumption and target frequency precision.

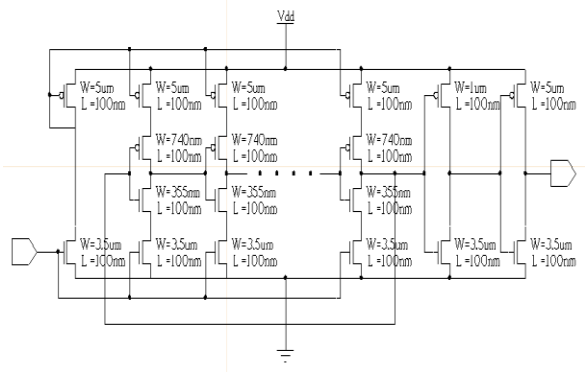


Fig. 1. Circuit Schematic of CSVCO

The frequency of oscillation of an N stage CSVCO [5] is given by

$$f_{osc} = \frac{I_d}{N\, V_{dd}\, C_{tot}} \tag{1}$$

where $C_{tot}$ is the total effective parasitic capacitance which is estimated using the design and SPICE parameters.

The current starved circuit dissipates a power [5] which can be expressed as

$$P = P_{avg} + P_{SC} \tag{2}$$

Where $P_{avg}$ is the average power dissipated by the CSVCO and $P_{SC}$ is the short circuit power dissipation [6].

Mathematically for convenience we can have a representation for NN, FF, FS, SF and SS as j=0,1,2,3 and 4 respectively. In the nominal case for optimal performance the CSVCO objectives are

$$F_1 = P = P(0) \tag{3}$$

$$F_2 = \left|\hat{f}_{osc}(0) - f_{osc}\right| \tag{4}$$

Where $f_{osc}$ is the target frequency and $\hat{f}_{osc}(0)$ estimated frequency for the nominal case.

The second part of optimization is for process corner performance variability (PCPV). The proposed work formulates the objectives in such a manner that the effective performance variation of corner cases from the nominal case is subjected to minimization. This concept is depicted in figure 2 where the optimization engine is trained to orient the design such that the worst case corners are pushed towards the nominal case.

Since there are three performance measures for the CSVCO circuit under consideration there are two variability objectives. The power consumption and frequency of oscillation variability objectives can be formulated as

$$F_3 = \sqrt{\left\{\sum_{j=1}^{4} |\hat{P}(0) - \hat{P}(j))|^2\right\}} \tag{5}$$

$$F_4 = \sqrt{\left\{\sum_{j=1}^{4} \left|\hat{f}_{osc}(j) - f_{osc}\right|^2\right\}} \tag{6}$$

### C. The Multiobjective Optimization

The optimization problem can be stated as

$$Minimize\ \{F_1, F_2, F_3, \dots, F_5\}$$

$$Subject\ to \quad \left.\begin{array}{c} f_{osc} = 2\ GHz \\ W_{min} < W < W_{max} \\ L_{min} < L < L_{max} \end{array}\right\} \tag{7}$$

$$where\ F_j = F_j(W, L, V_t, t_{ox}, V_{dd,} T)$$

In the above expression $W_{min}$, $L_{min}$, $W_{max}$ and $L_{max}$ are lower and upper bounds of width and length respectively.

W is the width of the transistor, L is the length, $V_t$ is threshold voltage, $V_{dd,}$ supply voltage, $t_{ox}$ oxide thickness and T is the absolute temperature.

One of the most efficient and recently developed evolutionary algorithms, Infeasibility Driven Evolutionary Algorithm (IDEA), [4] is deployed here for multiobjective optimization due to its reported superior performance. A brief outline of IDEA is as follows.

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Infeasibility Driven Evolutionary Algorithm (IDEA) for Robust IC Design

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Set: $N$ {Population Size}
Set: $N_G > 1$ {Number of Generations}
Set: $0 < \alpha < 1$ {Proportion of infeasible solutions}
1: $N_{inf} = \alpha * N$
2: $N_f = N - N_{inf}$
3: *while* $Parameter\ Constraints\ C = [W_{min} < W < W_{max}, L_{min} < L < L_{max}]$ *do*
4: pop1 = Initialize () *subject to C*
5: Evaluate $[F_j(pop1), \forall j \in \{1, \ldots, 6\}]$
6: for $i = 2$ to $N_G$ do
7: $childpop_{i-1}$ = Evolve ($pop_{i-1}$)
8: Evaluate $[F_j(childpop_{i-1}), \forall j \in \{1, \ldots, 6\}]$
9: $Compute\ D = |f_{osc} - f_{target}|$
10: $if\ D \leq \epsilon\ then\ S_f$
else $S_{inf}$
$end\ if$
11: ($S_f, S_{inf}$) = Split ($pop_{i-1} + childpop_{i-1}$)
12: Rank($S_f$)
13: Rank($S_{inf}$)
14: $pop_i = S_{inf}(1 : N_{inf}) + S_f(1 : N_f)$
15: end for
16: *end while*

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In the above pseudo code Evolve is the procedure of crossover, mutation and non-dominated sorting. $S_f$ and $S_{inf}$ represent the feasible and infeasible sets of solutions and $N_f$ *and* $N_{inf}$ are their modulus respectively.

## III. Performance Analysis of the Proposed Methodology

The robust design targets the performance objectives target frequency precision, power consumption as described earlier through equations (4), (5) and (6). The design targets to achieve a frequency of 2 GHz. The five design parameters (Wn, Wp, Wncs, Wpcs, L) obtained from the proposed IDEA based robust methodology are used to design the CSVCO in the Cadence Analog Virtuoso Design environment [10]. The circuit is simulated at schematic level and then in the physical layout level which is depicted in figure 3. Simulation is carried out 90nm CMOS Salicide 1.2V/2.5V 1P 9M technology with a supply voltage of 1.2V at room temperature. The BSIM model library [11] is used in the process. The robust circuit is subjected to process corner variations. The frequency of oscillations and power consumption performances are estimated at different process corners. Their values for a conventional optimized design and robust design are summarized in Table I.

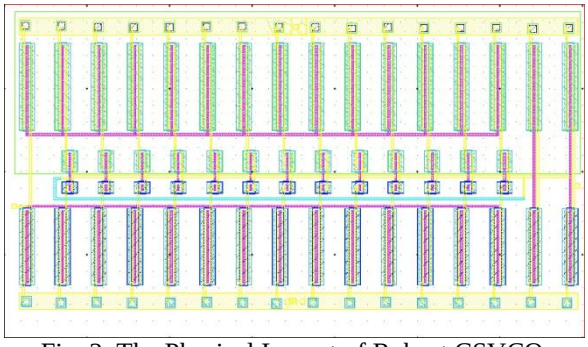

Fig. 2. The Physical Layout of Robust CSVCO

TABLE I

Design Parameter of Optimized Nano-CMOS CSVCO

| Process Corners | Oscillation Frequency in GHz | | Power in mW | |
|---|---|---|---|---|
| | Conventional Design | Robust Design | Conventional Design | Robust Design |
| NN | 2.305 | 2.048 | 1.589 | 1.0625 |
| FF | 3.15 | 2.596 | 2.226 | 1.875 |
| FS | 2.14 | 2.114 | 1.745 | 1.275 |
| SF | 2.11 | 1.997 | 0.8 | 0.7842 |
| SS | 1.4 | 1.972 | 0.575 | 0.7453 |

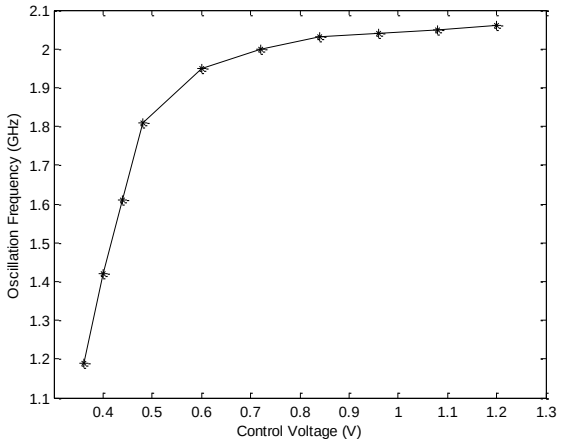


Fig. 3. The Tuning range plot of Robust CSVCO

Figure 3 depicts the tuning range plot of the robust CSVCO circuit. The estimated tuning range is about 22 MHz which is 11 % of the center frequency.

Figure 4 shows the comparative plot of the frequency of oscillations obtained using the robust design and that using the conventional one. In each corner case the proposed robust design achieves frequency which is more close to the target frequency. In the FF case of the robust design there is more deviation from the target value which is very much expected. However in other corner cases the observed frequency shows a better trend of matching with the expected frequency. In the nominal case there is 13% change in frequency in the expected dimension.

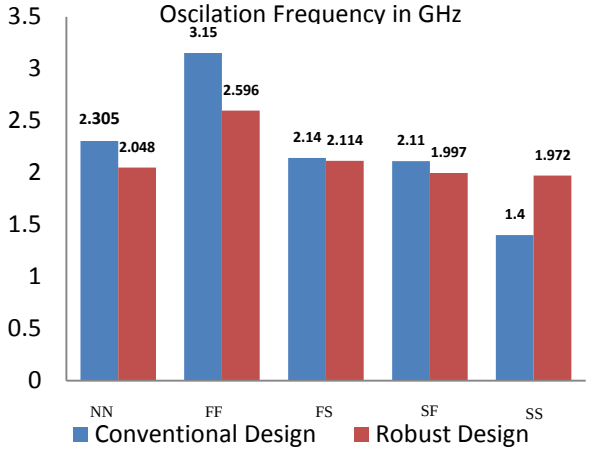


Fig. 4. Oscillation Frequency of CSVCO for Conventional and Robust Designs

It is clear from the histogram shown in figure 5 that in general the average power consumption of the robust CSVCO is less than the conventional one. The robust design achieves a 33% power reduction as compared to the conventional case. In robust NN case there is a considerable power reduction as compared to the reduction in other corner cases except SS case where there is a very little increase in power.

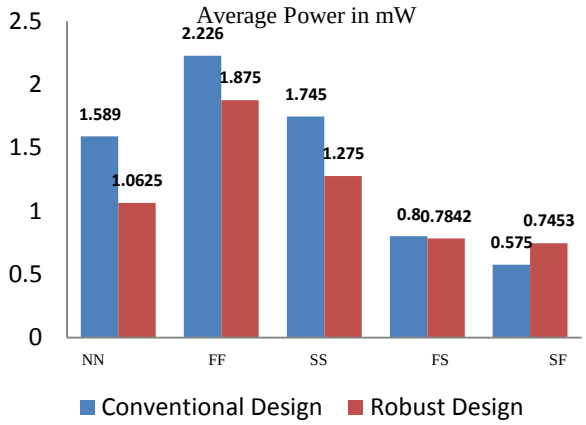


Fig.5. Average Power Consumption of CSVCO for Conventional and Robust Designs

## IV. Conclusion and Scope for Future Work

A novel design methodology for a robust current starve VCO is proposed. The technique optimizes the performance of the VCO circuit in nominal case and also guides the design in such a way that the other corner cases tend to behave closer to the nominal case. The power consumption along with frequency of oscillation for CSVCO is considered here. This method of design helps in maximizing the yield of integrated circuits. This work can be extended to include other process corners and performance indices like phase noise and area.

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