ATLAS™ based simulation study of the electrical characteristics of dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs

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***Abstract*—Recessed-Source/Drain (Re-S/D) SOI (Silicon on Insulator) MOSFETs (Metal-Oxide-Semiconductor Field-Effect-Transistors) offer higher drain current compare to conventional SOI MOSFETs which may be attributed to large source and drain area in recessed S/D devices. The concept of dual-metal-gate has already been incorporated in the recessed S/D SOI MOSFETs by our group and the devices have been named as Re-S/D fully-depleted (FD) SOI MOSFETs. In this work, 2D numerical simulations have been carried out to study the electrical characteristics like surface potential, threshold voltage and drain current of Re-S/D FD SOI MOSFETs. Device parameters like the depth of S/D in the buried oxide and gate length ratio are varied to access their impact on the surface potential, threshold voltage and drain current. All these numerical simulation results are obtained from ATLAS™, a 2-D numerical device simulator from SILVACO Inc.**

Keywords—Short Channel Effects, DMG FD SOI MOSFETs, recessed-source/drain (Re-S/D).

I. INTRODUCTION

In recent years the ultra-thin-body (UTB) silicon on insulator (SOI) MOSFETs device structures have been considered as one of the best alternative to the conventional MOSFETs in VLSI technology [1,2]. One of the reasons behind this consideration is the ultra-scalability of UTB SOI MOSFETs which may be attributed to reduce short channel effects due to presence of the ultra-thin-body (UTB) and the thick buried oxide [3]. However, due to the ultra-thin source and drain regions, fully-depleted (FD) SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device, despite having excellent short-channel characteristics. To overcome this large series resistance problem Zhang et al. proposed a new recessed source/drain (Re-S/D) fully-depleted (FD) UTB SOI MOSFET structure [4]. Later Svilicic et al. developed, a physics-based threshold voltage model for short channel (sub-100 nm) Re-S/D UTB SOI MOSFETs [5]. Long *et al.* have proposed the dual-metal-gate (DMG) structure and concluded that the current drive capability is better for the DMG MOSFETs than the conventional MOSFETs [6]. In this work, the concept of DMG is adopted in order to include its implicit advantages in the Re-S/D UTB SOI MOSFET structure. Further, the electrical characteristics like surface potential, threshold voltage and drain current of the device are obtained by carrying out numerical simulations.

To study the performance of dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs, the obtained electrical characteristics have also been compared with the electrical characteristics of a fully-depleted (FD) SOI MOSFET and fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFET. ATLAS™, the 2-D numerical device simulator from SILVACO Inc. was used to carry out numerical simulations of the considered device structures.

II. DEVICE STRUCTURE

The cross-sectional diagram of a dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET structure used for simulation is shown in Fig.1. The position along the channel length is represented by the x- axis whereas the channel depth is represented by the y- axis as shown in the

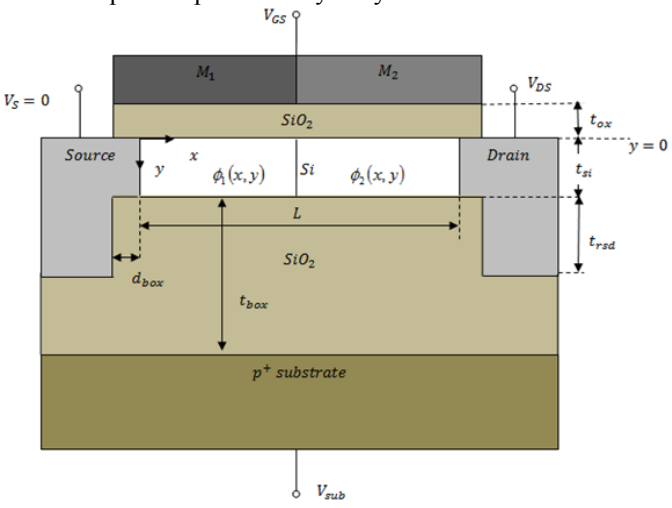

Fig. 1: Cross sectional view of DMG-Re-S/D on SOI MOSFET.

figure. Two metals of different work functions are deposited over gate oxide in a non-overlapping way to construct the gate of the device. The metal (M_1) with high work function of Length (L_1) is deposited toward the source side while metal (M_2) with work function of Length (L_2) is deposited toward the drain side. In this way total channel length of the devices becomes ($L = L_1 + L_2$). The gate with higher work function is called as the control gate (M_1) which is responsible in determining the threshold voltage of the device and the gate with lower work function is called the screen gate (M_2) which screens the effect of drain bias on the channel region. The metals (M_1 and M_2) divide the entire channel into two different virtual regions named as region I and region II respectively. The device is assumed to be doped uniformly having source/drain and body regions with doping densities of N_d and N_a respectively. The symbols t_{Si}, t_{ox}, t_{box} and t_{rsd} represent the thicknesses of the silicon, gate oxide, buried oxide and the source and the drain regions penetrate in to the buried oxide respectively.As shown in the Fig.1, d_{box} is the length of the source/drain overlap over the buried-oxide. The source/drain to channel junction is assumed to be abrupt. The MOSFET is biased by gate voltage of V_{GS}, drain voltage of V_{DS} and substrate voltage V_{sub} keeping the source voltage $V_S = 0$. Notations and values used for device parameters have been tabulated in Table I.

TABLE I. DEVICE PARAMETERS USED FOR SIMULATIONS

Parameters	**Values**
Control Gate work-function (ϕ_{M1})	4.8eV
Screen Gate work-function (ϕ_{M2})	4.6eV
Channel Doping (N_a)	10^{16} cm^{-3}
Source/Drain Doping (N_d)	10^{20} cm^{-3}
Substrate Doping (N_{sub})	10^{15} cm^{-3}
Silicon Thickness (t_{Si})	8nm
Gate Oxide Thickness (t_{ox})	2nm
Buried Oxide Thickness (t_{box})	200nm
The depth of S/D in the buried oxide (t_{rsd})	30nm
Recessed Length (d_{box})	3nm
Channel Length (L)	30nm to 300nm
Gate Voltage (V_{GS})	0.1V to 1V
Drain Voltage (V_{DS})	0.1V to 2V
Substrate Voltage (V_{Sub})	0V

III. RESULTS AND DISCUSSION

The numerical simulations have been carried out by a two-dimensional (2D) device simulator ATLAS™ from Silvaco Int. [7] for obtaining surface potential profile, threshold voltage and drain current. The models used during simulations are: the drift-diffusion model, FLDMOB mobility model, CVT mobility model and FERMI carrier statistical model, Shockley-Read-Hall (SRH) model. The threshold voltage of the device is determined from drain-current gate-voltage curve by assuming the value of gate voltage for drain current, $I_d = \frac{W}{L}10^{-7}$ A/μm (where W and L are the width and channel Length respectively) [8]. The metal work-function of the control gate is taken as 4.8eV (Au: Gold) and for screen gate as the 4.6eV (Mo: Molybdenum). To avoid the quantum tunneling effects, we considered channel thickness more than its limitation i.e. 5nm. The depth of S/D in the buried oxide (t_{rsd}) is considered as 30nm from Fig. 2 to Fig. 5. In this work we consider six types of devices namely 'Device 1' (conventional SOI MOSFET), 'Device 2' (recessed-source/drain (Re-S/D) SOI MOSFET), 'Device 3' (dual-metal-gate (DMG) SOI MOSFET), 'Device 4' (dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET with control-to-screen gate length ratio L=1:1), 'Device 5' (dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET with control-to-screen gate length ratio L=1:2), 'Device 6' (dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET with control-to-screen gate length ratio L=2:1)

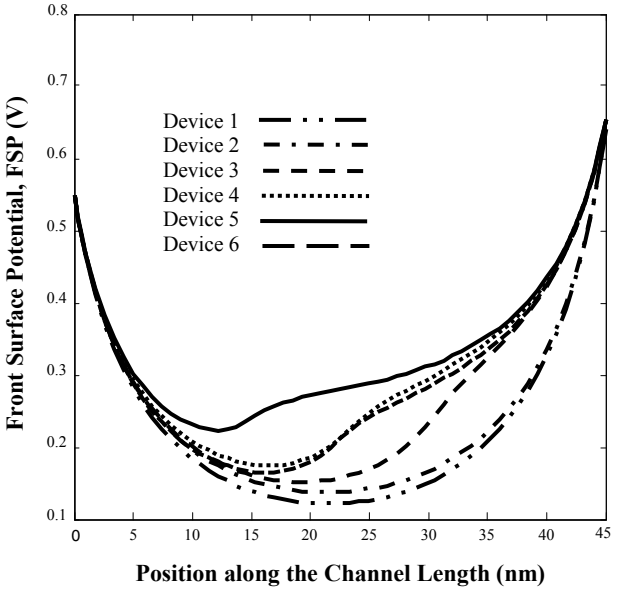

Fig.2 Surface Potential along the channel length at front gate where φ_{M1} =4.8eV, φ_{M2} =4.6eV, N_a =10^{16} cm^{-3}, N_d =10^{20} cm^{-3}, t_{si} =8nm, t_{ox}=2nm, V_{GS} =0.1V, V_{DS} =0.1V.

Fig. 2 shows various front surface potential curves plotted against the position along the channel length for devices under consideration. It is noticed from Fig. 2 that devices with dual-metal-gate structure i.e. Device 3 to Device 6 have a sudden rise in their surface potential profile at interface of metals (M_1 and M_2). The step profile at the junction of two gate metal electrodes (M_1 and M_2) screens channel region from the variations in the drain voltage. It is observed that the device with a higher length of screen gate is having the higher minimum front surface potential and lower source-channel barrier height. In addition to that, the minimum front surface potential moves towards the source end having an upward shift while decreasing the control gate length. Here it is worth to mention that high value of minimum surface potential results in lower threshold voltage and hence expected order of threshold voltage for these devices are (V_{th} of Device 1> V_{th} of Device 2 > V_{th} of Device 6 > V_{th} of Device 3 > V_{th} of Device 4 > V_{th} of Device 5).

Fig. 3 contains back surface potential curves along the channel length direction of devices under consideration. It is found that an increase in the control gate length leads to decrease in the minimum surface potential like the front surface potential. From Fig. 2 and Fig. 3, it is concluded that minimum back surface potential is higher than the minimum front surface potential for Devices 4, 5 and 6 and hence the back surface is responsible for the threshold voltage (V_{th}).The figure also shows that the minimum back surface potential is higher for the Device 4 than the Device 3. Fig. 4 deals with the threshold voltage (V_{th}) variation against channel length for the devices under consideration.

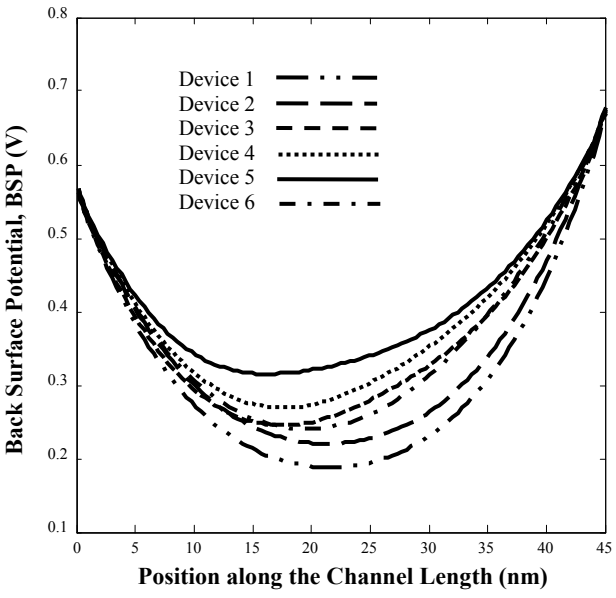

Fig.3 Surface Potential along the channel length at back gate where φ_{M1} =4.8eV, φ_{M2} =4.6eV, N_a =10^{16} cm^{-3}, N_d =10^{20} cm^{-3}, t_{si} =8nm, t_{ox} =2nm, V_{GS} =0.1V, V_{DS} =0.1V.

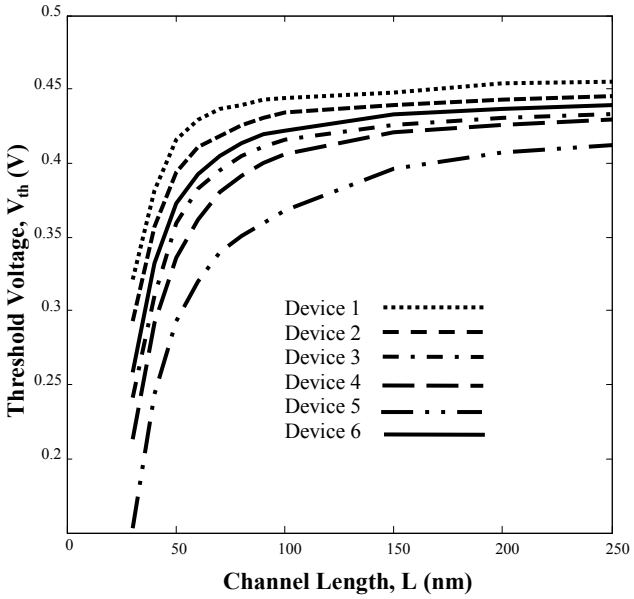

Fig. 4 Threshold Voltage along the channel length where φ_{M1} =4.8eV, φ_{M2} =4.6eV, N_a =10^{16} cm^{-3}, N_d =10^{20} cm^{-3}, t_{si} =8nm, t_{ox} =2nm, t_{box} =200nm, V_{DS} =0.1V.

It is observed that, the threshold voltage of Device 5 is lower than the Device4 and Device 6. In addition, the threshold voltage of Device 4 is observed to be less than Device 3. It may be attributed to the fact that the channel region of the recessed S/D devices are under the control of S/D which results in more short channel effects in recessed S/D devices.

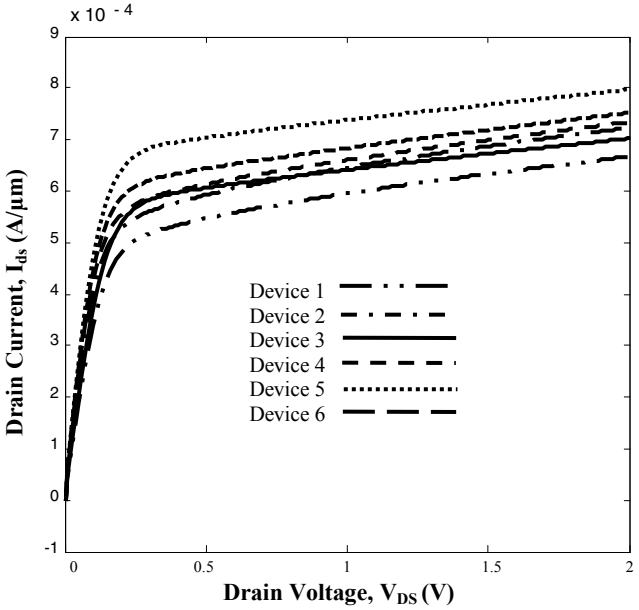

Fig. 5 Drain Current along the Drain Voltage, V_{DS} (V) where φ_{M1} =4.8eV, φ_{M2} =4.6eV, N_a =10^{16} cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} =8nm, t_{ox} =2nm, t_{box} =200nm, V_{GS} =0.1V.

Fig. 5 depicts the variation in the drain current (I_{ds}) with the change in applied drain voltage, (V_{DS}) for all the considered devices. It is noticed that a normal SOI MOSFET (Device 1) offers minimum drain current. Incorporation of recessed S/D structure in SOI MOSFETs (Device 2) improves the drain current capability. Moreover, incorporation of a DMG Structure in a recessed S/D (SOI MOSFETs (Device 4, 5, and 6) further improves drain current capability of the device. Comparing current levels of Devices 4, 5 and 6 it may be concluded that recessed S/D SOI MOSFETs with small length of control gate offer the highest drain current. The variation of the drain current (I_{ds}) with respect to drain voltage, (V_{DS}) for different combinations of t_{rsd} for a DMG-Re-S/D SOI MOSFET is demonstrated in Fig. 6. In Fig. 6 the control-to-screen gate length ratio is considered as L=1:1. It can be observed that the drain current (I_{ds}) is increased with increasing the depth of S/D in the buried oxide (t_{rsd}) till 30nm.

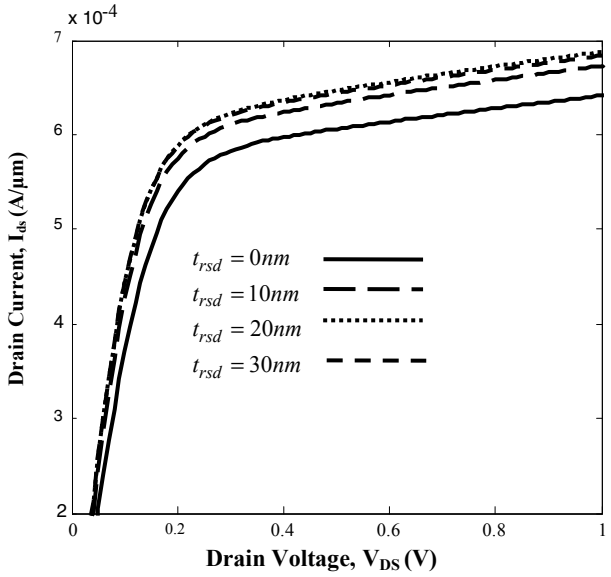

Fig. 6 Drain Current along the Drain Voltage, V_{DS} (V) for varying source/drain penetration in BOX.
where φ_{M1} =4.8eV, φ_{M2} =4.6eV, N_a =10^{16} cm^{-3}, N_d =10^{20} cm^{-3}, t_{si} =8nm, t_{ox} =2nm, t_{box} =200nm, V_{GS} =0.1V.

IV. CONCLUSION

Atlas based simulation study of various electrical characteristics such as the surface potential, threshold voltage and drain current have been explored and studied for dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs. It has been shown that the reduction in threshold voltage happened for dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs with increasing the source/drain penetration in BOX and also by increasing the length of control gate for the given channel length. The drain current (I_{ds}) is increased with increasing the source/drain penetration in BOX. It is also concluded that drain current drive capability of a Re-S/D MOSFETs can be further improved by incorporating the concept of dual metal gate structure in the device

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