Real Time Implementation of Digital Filter on Control strategy of DSTATCOM for Load Compensation under Distorted Utility Condition

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Abstract—**The Distribution STATic COMpensator (DSTAT-COM) has proved to be a useful custom power device to eliminate harmonic components and to compensate reactive power for balanced /unbalanced linear/nonlinear loads. This paper presents a novel control strategy to calculate the reference compensation current of three phase DSTATCOM under distorted utility condition at instantaneous state. In this proposed approach digital FIR filters with cut off frequency 25,100 Hz of direct form structure have been implemented on FPGA to make the process faster. The performance of the system simulated in Matlab Platform and evaluated considering the source current total harmonic distortion. The VHDL design has been implemented using ISE10.1 tool from Xilinx. This is tested on a board with hardware configuration such as FPGA - XC2VP4 with on chip PowerPC-405 Processor, ADC AD9240-14 bit 10MSPS analog input channel, DAC AD7541-12-bit of conversion time–100ns with System clock 40 MHz.**

Keywords—*Field programmable gate Array; Constant Coefficient; Distribution Static Compensator; Finite Impulse Response.*

I. INTRODUCTION

During the last decade, there has been sudden increase in the nonlinear load (Computers, Laser printers, SMPS, Rectifier etc.), which degrades the power quality causing a number of disturbances e.g. heating of home appliances, noise etc., in power systems[1], [2] due to harmonics.

To compensate the harmonics due to nonlinear load, a DSTATCOM is used [3]. The performance of DSTATCOM largely depends on the control strategies used for reference current extraction. The control strategy used conventionally, were based on active and reactive power are found unsuitable for unbalanced and distorted utility conditions. Significant contribution for development of control algorithm was made by Budeanu and Fryze[5]. They provide power definition in frequency and time domain and set the pathways for development universal set power definitions which led to the development of p-q theory by Akagi [5][6].

A variety of approaches to custom implementation of FIR filters have been pursued [7][8][9]. In order to attain high performance, low cost multiplier less implementation strategies such as constant co-efficient design [10] method has been applied. The paper [11] describes FPGA is more advantageous as compare to advanced microcontroller for implementation.

In this paper performance of proposed control strategy is investigated in **three phase three wire system** for balanced/distorted source and non-linear balanced /unbalanced Load for mitigation of harmonics and compensation of reactive power with digital filter which is defined as **problem statement**. The measures of the performance is the source current total harmonic distortion

Rest of the paper is organized as follows. In section II system configuration and in section III brief discussion on proposed control strategy is presented. In section IV constant coefficients design on Digital FIR filter direct form architecture and in section V the performance indices used for evaluation are discussed. Simulation results are described in section VI. Finally in section VII, conclusion is drawn.

II. SYSTEM CONFIGURATION

Fig.1 shows the basic circuit diagram of a DSTATCOM [3] system with non-linear load connected to three phase three wire distribution system. A nonlinear load is realized by using a three phase full bridge diode rectifier. A three phase voltage source converter (VSC) working as a DSTATCOM is realized using six insulated gate bipolar transistors (IGBTs) with anti-parallel diodes. At ac side, the interfacing inductors are used to filter high frequency components of compensating currents.

The first harmonic load currents of positive sequence are transformed to DC quantities. The first harmonic load currents of negative sequence and all the harmonics are transformed to non-DC quantities and undergo a frequency shift in the spectrum.

The voltage regulator in the converter DC side is performed by a proportional–integral (P-I) controller. Its input is the capacitor voltage error (v_{dcref}-v_{dc}) and it regulates the first harmonic active current of positive sequence. It is possible to control the active power flow in the VSC and thus the capacitor voltage V_{dc} remains constant.

The dynamics of each VSC are modeled by solving differential equations governing two-level inverter. The switching of the inverter is done by monitoring the reference and actual currents and comparison of error with the hysteresis band.

The VSC model is based on discrete switching variables g_a, g_b, g_c [4].

$$\begin{bmatrix} v_{fa} \\ v_{fb} \\ v_{fc} \end{bmatrix} = \frac{V_{dc}}{\sqrt{3}} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} g_a \\ g_b \\ g_c \end{bmatrix} \tag{1}$$

The $R–L$ network on the ac side of the converter is represented by three differential equations.

$$\left. \begin{aligned} L_f \frac{di_{fa}}{dt} &= -i_{fa}.R_f + v_{sa} - v_{fa} \\ L_f \frac{di_{fb}}{dt} &= -i_{fb}.R_f + v_{sb} - v_{fb} \\ L_f \frac{di_{fc}}{dt} &= -i_{fc}.R_f + v_{sc} - v_{fc} \end{aligned} \right\} \tag{2}$$

The dc side equations are defined as

$$i_{dc} = g_a.if_a + g_b.if_b + g_c.if_c \tag{3}$$

$$-C_{dc}.\frac{dv_{dc}}{dt} = i_{dc} \tag{4}$$

The equation for discrete **PI controller** is defined as

$$u(n) = u(n-1) + k_p\{e(n) - e(n-1)\} + k_i e(n) \tag{5}$$

Where u(n)= PI controller output, e(n)=V_{dcref}-V_{dc} , K_p = Proportional gain constant and K_i= Integral constant of PI controller.
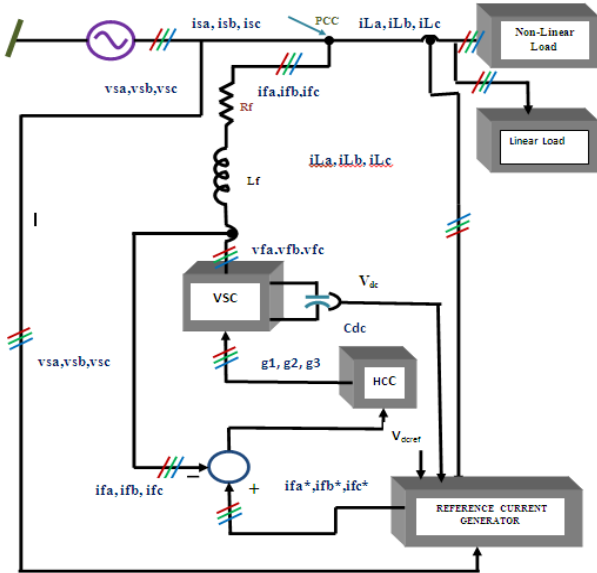

Fig.1 system configuration of DSTATCOM

III. PROPOSED CONTROL STRATEGY

This control strategy is best suitable for distorted utility condition. It is based on instantaneous symmetrical component theory in instantaneous state. The main objective to find out active fundamental source peak current.

The reference compensating current is equal to the difference between estimated source and load current.Fig.2 shows the control structure of proposed controller. The peak source current is estimated as

$$I_{sm1} = \frac{p_{3\phi}}{3V_m^+} \tag{6}$$

Prime objective is to make source current balanced.

$$i_a + i_b + i_c = 0 \tag{7}$$

Let formulate all powers in time domain. Zero sequence, positive sequence and Negative sequence complex power are denoted as s_0, s_+ and s_- . The real power of zero sequence ,positive sequence and Negative sequence are denoted as p_0,p_+ and p_-. The Imaginary power of zero sequence, positive sequence and Negative sequence are denoted as q_0,q_+ and q_- .The instantaneous voltage and current of zero sequence ,positive sequence and Negative sequence are denoted as v_0,v_+ ,v_- and i_0,i_+,i_- respectively. Let zero sequence power is formulated as

$$\left. \begin{aligned} s_0 &= 3v_0 * i_0^* = p_o + jq_0 \\ p_0 &= \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c) \\ q_0 &= 0 \end{aligned} \right\} \tag{8}$$

Let calculate the positive sequence power.

$$\left. \begin{aligned} s_+ &= 3v_+ i_+^* = p_+ + jq_+ \\ p_+ &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c) \right] \\ q_+ &= -\frac{1}{2\sqrt{3}} \; v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b) \end{aligned} \right\} \tag{9}$$

Let calculate the negative sequence power.

$$\left. \begin{aligned} s_- &= 3v_- i_-^* = p_- + jq_- \\ p_- &= \frac{1}{2}\left[(v_a i_a + v_b i_b + v_c i_c) - \frac{1}{3}(v_a + v_b + v_c)(i_a + i_b + i_c) \right] \\ q_- &= \frac{1}{2\sqrt{3}} \; v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b) \end{aligned} \right\} \tag{10}$$

Where total Instantaneous active power is defined as

$$s = (s_0 + s_+ + s_-) = (p_0 + p_+ + p_-) = p_{3\phi} = (v_a i_a + v_b i_b + v_c i_c) \tag{11}$$

In equation (11) putting $i_a + i_b + i_c = 0$, We get

$$\frac{p_{3\phi}}{2} = p_+ = \frac{3V_m^+}{\sqrt{2}} \frac{I_{sm}^+}{\sqrt{2}} \qquad (12)$$

$$I_{sm}^+ = I_{sm} = \frac{p_{3\phi}}{3V_m^+} \qquad (13)$$

So
$$\left.\begin{array}{l} i_{sk}^* = i_{skref} = I_{sm}U_{ck1} \\ i_{fk}^* = i_{fkref} = i_{Lk} - i_{skref} \end{array}\right\} \qquad (14)$$

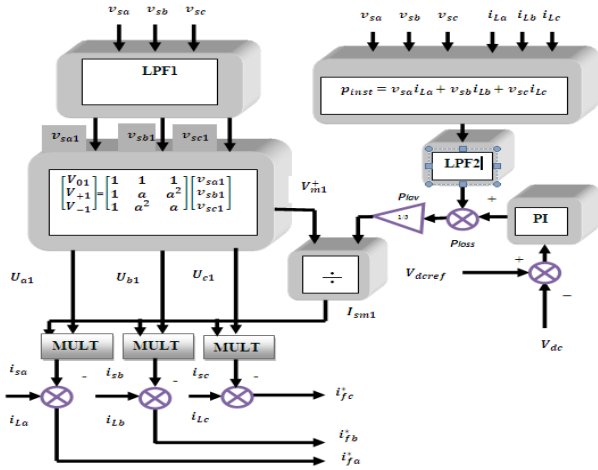Where k=a, b, c and Uck1 is fundamental unit vector template.

Fig.2 Control structure of proposed algorithm

Fig.2 shows the basic control structure of proposed algorithm which constitute one PI controller, low pass filters (LPF1 and LPF2) and arithmetic calculators. The average power p_{lav} is calculated by adding PI output (P_{loss}) to LPF2 output. LPF1 is used to extract the fundamental from distorted PCC (point of common coupling) voltage.

IV. DIGITAL FILTER

Digital filters are typically used to modify or alter the attributes of a signal in the time or frequency domain. The most common digital filter is the linear time invariant (LTI) filter. An LTI interacts with its input signal through a process called linear convolution, denoted by y= h*x where h is the filter's impulse response, x is the input signal, and y is the convolved output. The linear convolution process is formally defined by;

$$y[n] = \sum_k x[k]h[n-k] \qquad (15)$$

LTI digital filters are generally classified as being finite impulse response (FIR) ,or infinite impulse response (IIR). As the name, an FIR filter consists of a finite number of sample values, reducing the above convolution sum to a finite sum per output sample instant. An IIR filter however, requires that an infinite sum be performed.

The motivation for studying digital filters is found in their growing popularity as a primary dsp operation. Digital filters are rapidly replacing classic analog filters, which were implemented using RLC components and operational amplifiers. Analog filters were mathematically modeled using ordinary differential equations of Laplace transforms. Analog prototypes are now only used in IIR design, while FIR is typically designed using direct computer specifications and algorithms.

An FIR with constant coefficient s is an LTI digital filter. The output of an FIR filter of order or length N, to an input time series x[n], is given by a finite version of the convolution sum given in (15) namely;

$$y[n] = x[n] * h[n] = \sum_{k=0}^{N-1} h[k]x[n-k] \qquad (16)$$

Where h(0) $\neq$0 through   h[N-1] $\neq$0 are the filter's N coefficients. They also correspond to the FIR's impulse response. For LTI systems it is some times more convenient to express (16) in the z-domain with

$$Y(z)=H(z)X(z) \qquad (17)$$

Where   H(z) is the FIR's transfer function defined in the z-domain by

$$H(z) = \sum_{k=0}^{N-1} h[k]z^{-k} \qquad (18)$$

The Nth order LTI FIR filter is graphically interpreted in fig.3. It can be seen to consist of a collection of a "tapped delay line" adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons.
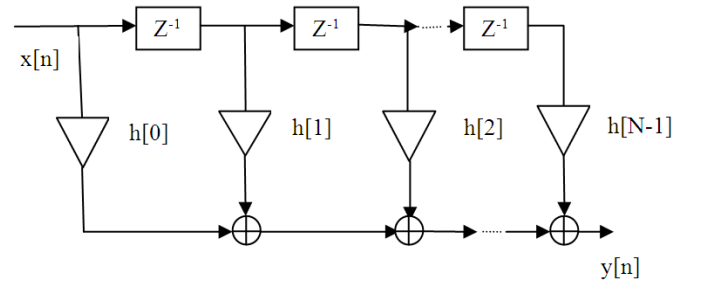

Fig. 3 FIR filter in the direct form structure

The roots of polynomial H (z) in (18) define the zeros of the filter. The presence of only zeros is the reason that FIRs are sometimes called all zero filters. We note that non-recursive filters are always FIR, whereas recursive can be IIR.

A. Constant co-efficient Design

There are only a few applications (e.g., adaptive filters) where we need general programmable filter architecture. In much application, the filters are LTI (i.e., linear time invariant) and the coefficients do not change over time. In this case the hardware effort can essentially be reduced by

exploiting the multiplier and adder (trees) needed to implement the FIR filter arithmetic.

With available digital filter design software the production of FIR coefficient is a straightforward process. Here the co-efficients are obtained for linear phase with application of kaiser window. The challenge remains to map the FIR design into a suitable architecture. The direct or transposed forms are preferred for maximum speed and lowest resource utilization.

The direct FIR filter can be implemented in VHDL using (sequential) PROCESS statements or by "component instantiations" of the adders and multipliers. A PROCESS design provides more freedom to the synthesizer, while component instantiations gives full control to the designer.

In a practical situation, the FIR coefficients are obtained from a computer design tool and presented to the designer as floating point numbers .The performance of a fixed –point FIR, based on floating point coefficient , needs to be verified using simulation or algebraic analysis to ensure that design specifications remain satisfied. Another issue that must be addressed when working with fixed-points designs is protecting the system from dynamic range overflow .Fortunately, the worst-case dynamic range growth G of Nth order FIR is to compute and it is defined as:

$$G \leq \log_2 \left(\sum_{k=0}^{N-1} |h[k]| \right) \tag{19}$$

The total bit width is then the sum of the input bit width and the bit growth G.

V. PERFORMANCE INDICES

A. Total harmonic distortion

The total harmonic distortion (THD) [12] is used to define the effect of harmonics on the power system voltage. It is used in low-voltage, medium-voltage, and high-voltage systems. It is expressed as a percent of the fundamental and is defined as

$$THD(voltage) = \frac{\sqrt{\sum_{h=2}^{50} V_h^2}}{V_1} *100\% \tag{20}$$

$$THD(current) = \frac{\sqrt{\sum_{h=2}^{50} I_h^2}}{I_1} *100\% \tag{21}$$

According to IEEE-519 the permissible limit for distortion in the signal is 5%.

VI. RESULTS AND DISCUSSION

To investigate the performance of the DSTATCOM for proposed control strategy, simulations are performed on matlab platform. A three phase three wire distribution system with parameters given below is considered for simulation.

A. System Parameters:

Supply voltage: 50Vrms (L-L), 50Hz, three phase balanced
Source impedance: R_s=0.1Ω, L_s=0.5mH
Nonlinear load: Three phase full bridge diode rectifier with load (L=10mH,R_L=3.7Ω)
DC storage Capacitor C_{dc}=3000μF
Interface inductor L_f=10mH , R_f=0.1Ω
DC Link voltage V_{dc}=100V
Hysteresis band=0.25A
Unbalanced Linear load: Z_a=67+j31.42Ω , Z_b=37+j18.55Ω, Z_c=28.5+j12.56Ω
PI regulator parameters: K_{pr}=1.0259,K_{ir}=227.9288

B. Design specification of Digital Filter:

Low-pass FIR filter has been implemented with Response type: Low pass
Design method: Constant coefficient FIR design (window technique)
Filter Length or no. of taps: 5
Hardware architecture: Direct form
Sampling frequency: 5kHz
Cut-off frequency: 25Hz(LPF2),100Hz (LPF1)
Input data length: 13 bits
Output data length: 14 bits
Arithmetic: fixed point
The performance of the proposed control strategy is evaluated based on three different cases.
Case1- Balanced Source and balanced Non-Linear load
Case2- Balanced Source and Unbalanced Non-linear load.
Case3- Balanced distorted Source and Unbalanced Non-linear load.

In **case 1** the source is assumed to be sinusoidal and balanced whereas the load is considered as non-sinusoidal and balanced with load as six pulse diode full bridge rectifier. Before compensation the THD of load current is found to be **23.2361%.** After compensation the THD for proposed control strategy is listed in the T**able1.**

In **case 2** the source is balanced and sinusoidal but the load is unbalanced non –sinusoidal (load current harmonic is found to be **22.2914%)** .The THD of the load current for phase **a** after compensation is summarized in **Table1.**

The results demonstrated here are considered for phase a only.

In **case 3** the source is balanced and distorted(**distorted voltage source harmonic is 13.7477%)** but the load is unbalanced non sinusoidal (load current harmonic is found to be **22.2914%)** . The THD of the load current for phase **a** after compensation is summarized in **Table 1.**The results demonstrated here are considered for phase a only.

The digital filter LPF1 which has been used across the source voltages need to extract fundamentals from distorted sources. In this simulation implementation of LPF1 on FPGA has been demonstrated. The convolved output for five samples is also demonstrated in VHDL test bench simulation.

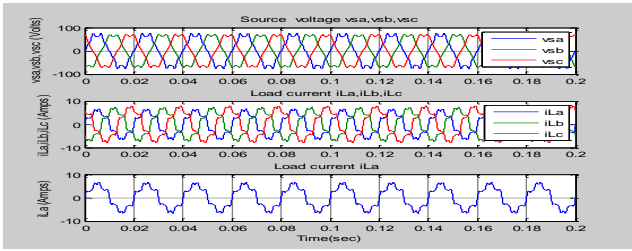## C. Case 3 Proposed control strategy simulation

Fig.4a Balanced distorted source voltage, Unbalanced Load current,
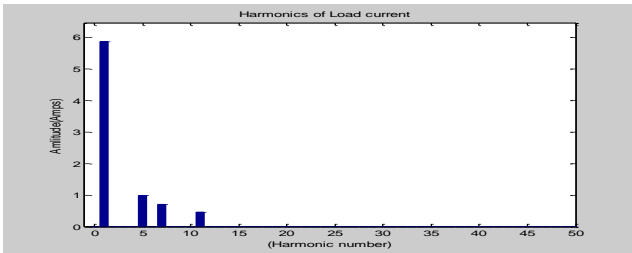
Phase a Load current

Fig.4b Harmonics of Load current of Phase a
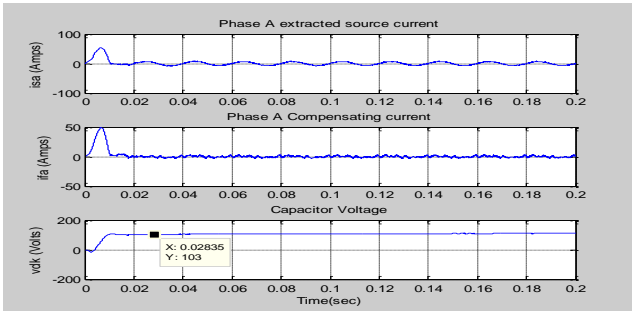

Fig.4c Phase A extracted Source current, Compensating
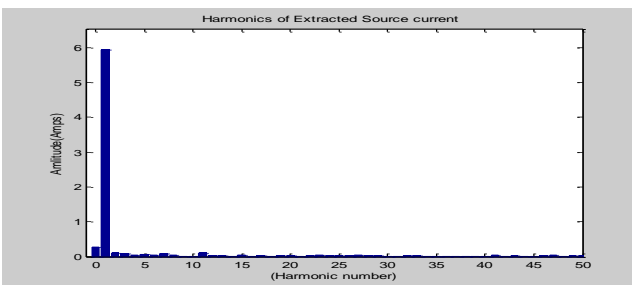
Current and DC link Capacitor Voltage

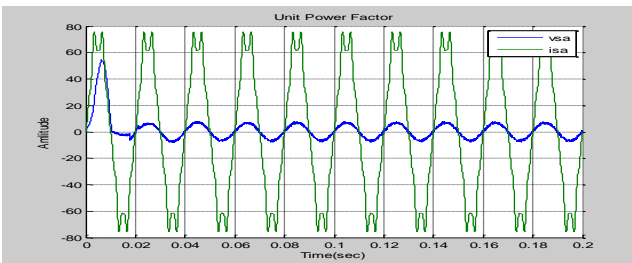Fig.4d Harmonics of extracted Source current

Fig.4e Unit power factor of compensated load

Fig.4 (a, b, c, d, e) shows the dynamic performance of the system.

Table1. THD% of extracted source current

Control strategy	THD(%) of Extracted source current		
	CASE-1	CASE-2	CASE-3
PROPOSED	3.6914	4.2566	**4.7345**

D. Simulation of Digital Filter

The Fig. 5a shows the magnitude response of desired filter The response curve indicates that when the normalized cutoff frequency is 0.04(equal to 100Hz) then the magnitude is approximately satisfy the linear phase(-6dB). Fig.5 (b, c) shows the filter output more than one sample for vhdl simulation. Fig.5d shows the RTL schematic and Fig.5e depicts the interfacing of ADC module with FIR module is named as top module in the design.
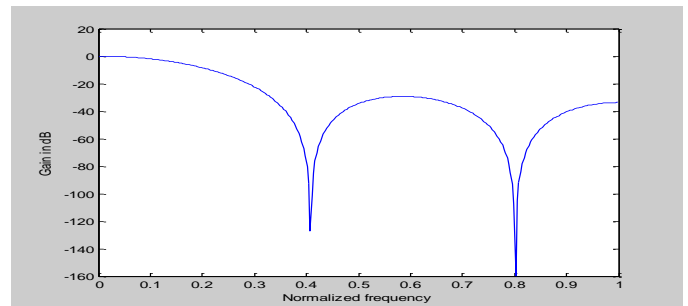

Fig.5a Low pass 5-tap FIR filter magnitude response   with f_c = 100 Hz, f_s=5kHz

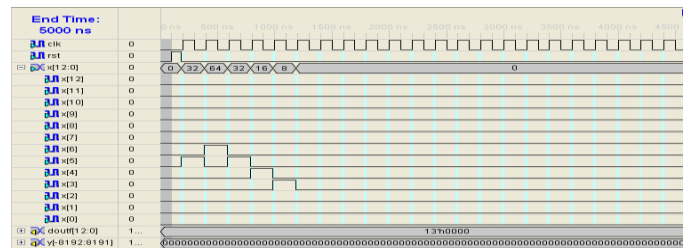Filter co-efficients hn =[0.1928 0.2036 0.2072   0.2036 0.1928]

Fig.5b VHDL test bench i/p for 5 samples
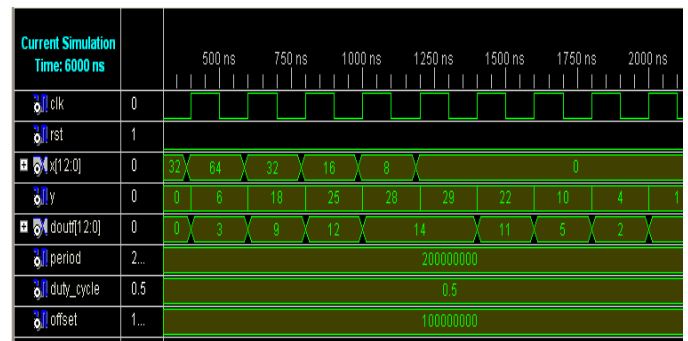

Fig.5c VHDL Test bench o/p for 5 samples

Fig.5d RTL Schematic of top module

Fig.5e ADC Interfacing with FIR module

E. Implementation Result

The design is implemented in VHDL using ISE10.1 tool from Xilinx. The testing board has hardware configuration such as FPGA - XC2VP4 with on chip PowerPC-405 Processor, ADC - 14 bit, 10MSPS analog input channel is available using AD9240, DAC - One channel, using 12-bit DAC, AD7541of conversion time – 100ns with System clock 40 MHz, DSO and Signal Generator. Fig.6a shows the resource utilization indicates the area consumed in FPGA.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	107	6,016	1%
Number of 4 input LUTs	608	6,016	10%
Logic Distribution			
Number of occupied Slices	362	3,008	12%
Number of Slices containing only related logic	362	362	100%
Number of Slices containing unrelated logic	0	362	0%
Total Number of 4 input LUTs	653	6,016	10%
Number used as logic	608		
Number used as a route-thru	45		
Number of bonded IOBs	31	348	8%
Number of BUFGMUXs	2	16	12%

Fig.6a Device utilization summary

VII. CONCLUSION

In all cases it is observed that proposed control strategy is working fine and able to compensate the nonlinear unbalanced load successfully. The THD obtained here are within the limit of 5% prescribed by IEEE 519. The digital filter LPF1 and LPF2 have been implemented successfully on FPGA

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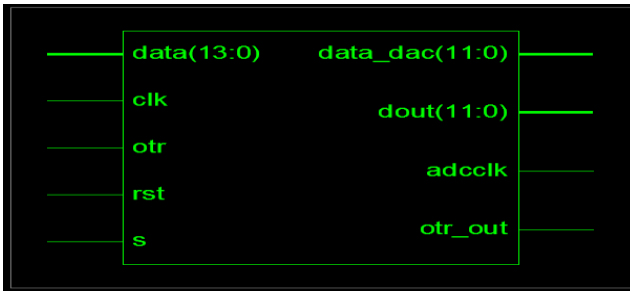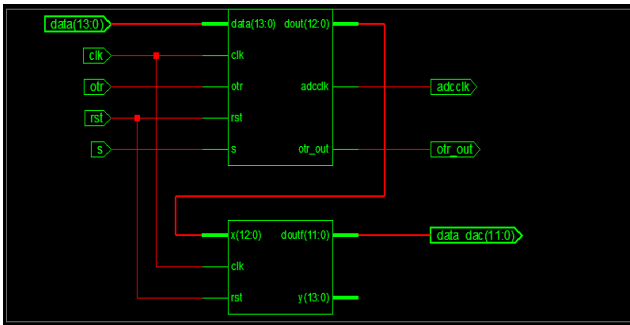[12] IEEE Recommended Practices and Requirements /or Harmonic Control in Electrical Power Systems, *IEEE Standard 519*, 1992.