A Novel Low Power 3T Inverter

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***Abstract*---** **Though CMOS logic inverter is widely appreciated because of its negligible static power consumption still sometimes it is deprecated because of the high dynamic power consumption. The high dynamic power consumption is because of the charging and discharging of the load capacitor and also because of the unwanted short-circuits current from V_{dd} to ground. The proposed three transistor saturated NMOS inverter reduces the short-circuit current and hence reduces the overall power consumption. The proposed inverter reduces the average power consumption by 35% for any input signal of frequency less than or equal to 1 MHz and by 15% for any input signal up to around 10MHz. But the power consumption slowly increases when the input frequency goes beyond 100 MHz. So the proposed inverter can be used in MHz applications to save a good amount of power.**

***Index Terms*— Inverter, dynamic power, short circuit current, low power, stability.**

I. INTRODUCTION

The revolutionary advancement in the electronics industry is no doubt the result of adoption of the very large scale integration technology. The VLSI technology is capable to build complex to more complex applications in very a small and faster chip consuming a very small amount of energy. All this can happen only because of the Digital Complementary Metal Oxide Semiconductor (CMOS) technology [1,2]. This is because of the salient features like low power consumption, constantly decreasing feature size, high reliability, increasing speed and standard fabrication process. Still a continuous effort is given to improve the digital circuit to increase its performance in terms of its area, speed and power consumption. As the digital logic inverter is common almost in all the digital circuit giving some effort to reduce the energy consumption of the logic inverter block really helps to reduce the overall power consumption of the circuit.

The power consumption in an inverter circuit can be broadly divided into two parts. (a) The static power consumption. It is mainly due to the leakage and the sub threshold current during the interval when no state of the circuit changes. (b) The dynamic power consumption [3,4]. It is mainly because of the current which charges or discharges the load capacitance at the time of state change, and the short circuit current which is completely undesirable as it comes under the energy loss of the circuit. This paper presents a novel three transistor inverter circuit which helps to block the short circuit current hence reduces the overall power consumption.

II. CONVENTIONAL INVERTER

As shown in figure 1 when the input goes low the NM0 should be off and PM0 should be on which supply a charging current from V_{dd}, to charge the load capacitance C_{Load}. When the input goes high the PM0 should be off and NM0 should be on allowing the load capacitor to discharge through it. But as none of the practical input signal can be an ideal one, it must have some definite rise and fall time. Analysis should be done to see the behavior of the circuit in this transition period

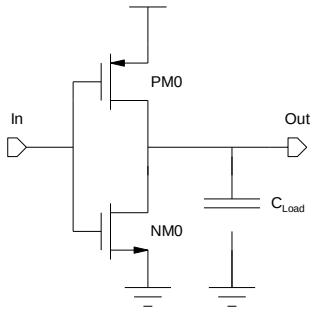


Fig. 1: Conventional inverter

As shown in Fig. 2, in a CMOS circuit during the falling input transition when the input reaches at V_{dd}-$|V_{tp}|$ the PMOS starts to conduct whereas the NMOS stops conduction when the input reaches at $V_{tn.}$ Hence the duration when the input transits from V_{dd}-$|V_{tp}|$ to V_{tn} both PMOS and NMOS will be on, leading to a short circuit current, which will not be utilized to increase the output node voltage rather that will be wasted through the NMOS [5]. Similarly during a rising input of a CMOS circuit when the input reach at V_{tn} the NMOS switches on whereas the PMOS switches off when the input voltage reaches at V_{dd}-$|V_{tp}|$. So the duration when the input transit from V_{tn} to V_{dd}-$|V_{tp}|$ there will be a short circuit current from V_{dd} to gnd which will lead to power loss [6-8]. The proposed

saturated NMOS inverter blocks the short-circuit current and hence reduces the overall power consumption.

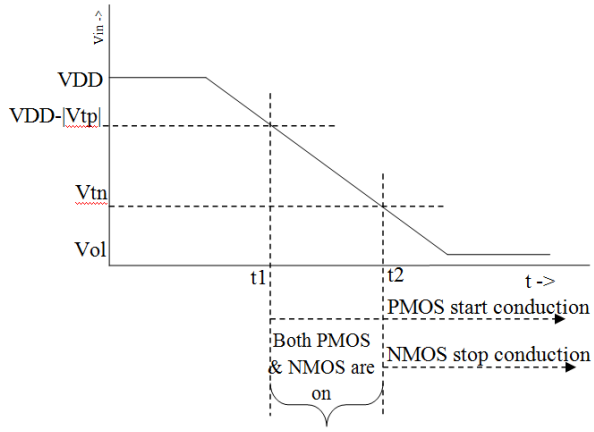


Fig. 2: Analysis of a falling input pulse

III. SATURATED NMOS INVERTER

Figure 3 shows the saturated NMOS inverter which contains the NMOS NM1 connected in-between NM0 and PM0. The source of NM1 is connected to the drain of NM0. The drain of PM0 is connected to the gate as well as to the drain of the NM1. As gate and drain of NM1 are shorted, NM1 can lie either in saturation or in cutoff mode. NM1 will start conduction only if V_{gs1} is more than the threshold voltage of NM1. So at least the output should be V_{th} amount more than V_{ds0} for NM1 to starts conduction.

During the falling transition shown in the figure 1 when input falls below V_{dd}-$|V_{tp}|$ point, PM0 switches on. The charging current starts to flow from V_{dd} through PM0 and the output node starts to charge. Initially as the output node is not charged NM1 is in off state. Hence all the current flowing from V_{dd} is utilized to charge up the output node. Once the output node charges up to V_{th} then NM1 switches on. Hence now some fraction of the current will be utilized to charge up the output node and rest portion of the current will lead to a short-circuit current. The short circuit current stops when the input falls below V_{tn}.

Had it been a conventional inverter, as soon as input falls below V_{dd}-$|V_{tp}|$ point, PM0 would have switched on and short-circuit current would have started to flow through PM0-NM1-NM0. Summarily the duration of short-circuit current is more in case of conventional inverter in comparison to saturated NMOS inverter.

Similarly during a rising input when the input crosses V_{tn} the NMOS switches on. As initially the output node would be fully charged so NM1 would be on and the output node starts discharging. Along with that as the PM0 is also on during this duration so the short-circuit current also starts to flow. But as the input voltage increases and the output voltage continues to fall. When the output voltage falls below V_{th1} NM1 switches off, which stops the short-circuit current. Hence during the rising input transition also the duration of short-circuit current flow is reduced which decreases the power loss and the overall power consumption.

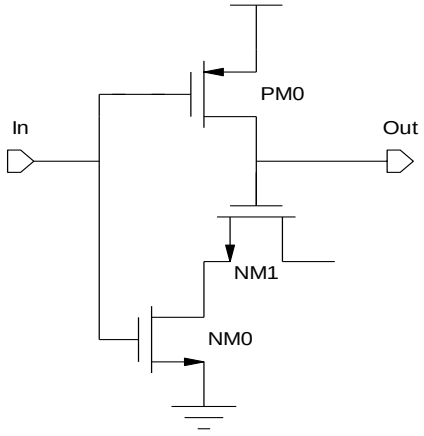


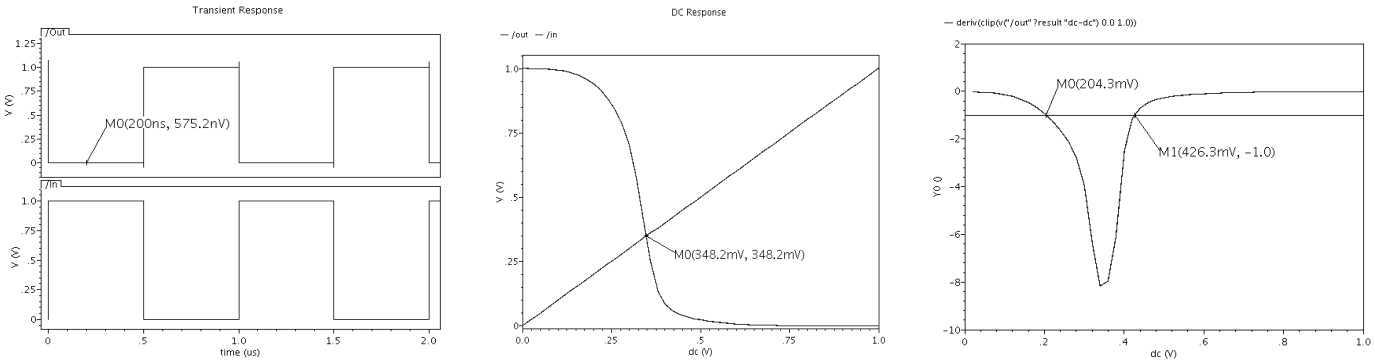
Fig. 3: The saturated NMOS inverter

IV. ANALYSIS OF SATURATED NMOS INVERTER

A rigorous analysis and a comparative study were performed to find the pros and cons of the saturated NMOS in comparison to the conventional inverter. A conventional inverter and a saturated NMOS inverter was designed using 90 nm technology and the transient analysis was performed using a 1MHz input signal. Figure 4(a) and 5(a) shows the transient analysis results for the conventional and the proposed inverter circuits respectively. From figure 4(a) & 5(a) it can be marked the V_{ol} of conventional inverter reaches around 572.2nv whereas the V_{ol} of the proposed inverter reaches around 2.916mv respectively. Though in case of the proposed inverter V_{ol} is high in comparison to that of the conventional inverter, still the value is much less than it's switching threshold voltage, which is equal to 406.1mv. Hence the proposed inverter inverts the signal properly. The noise margin of both the inverters are determined by taking the derivative of their voltage transfer characteristics and putting a horizontal marker at y = -1 point. Figure 4(b) & 5(b) depicts the VTC of conventional & proposed inverter respectively & Figure 4(c) & 5(c) represents their derivatives. The V_{IL} , V_{IH} , V_{OL} ,V_{OH} , NM_L & NM_H of the conventional and the proposed inverter are shown in table 1. From table 1 it can be found that the noise margin low of the proposed cell improves by 19.5% than the conventional inverter whereas the noise margin high degrades by 2.16%.

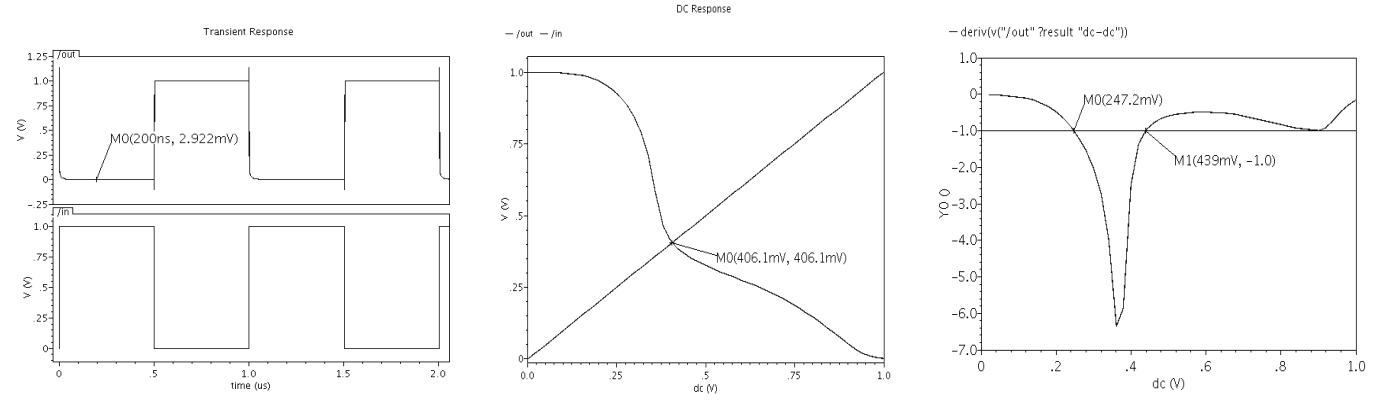
	V_{IL} (mV)	V_{IH} (mV)	V_{OL}	V_{OH}(mV)	NM_L(mV)	NM_H(mV)
Conventional	204.3	426.3	866.0nV	999.268	204.299	572.968
Proposed	247.2	439.0	2.915mV	999.554	244.285	560.554

Table 1: Noise margin of conventional & proposed inverter



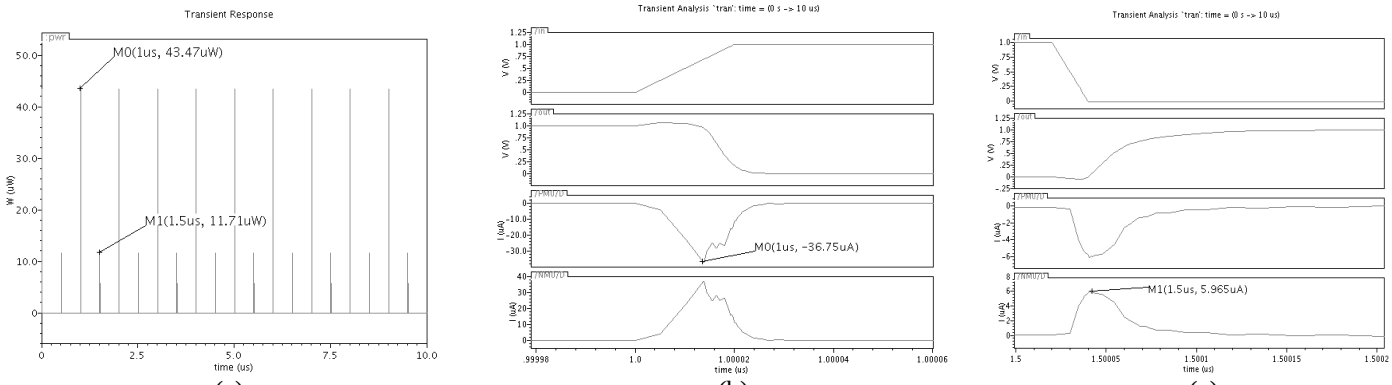
(a) (b) (c)

Figure.5: Conventional CMOS inverter: (a) Transient analysis (b) Voltage transfer characteristics (c) Derivative of the VTC



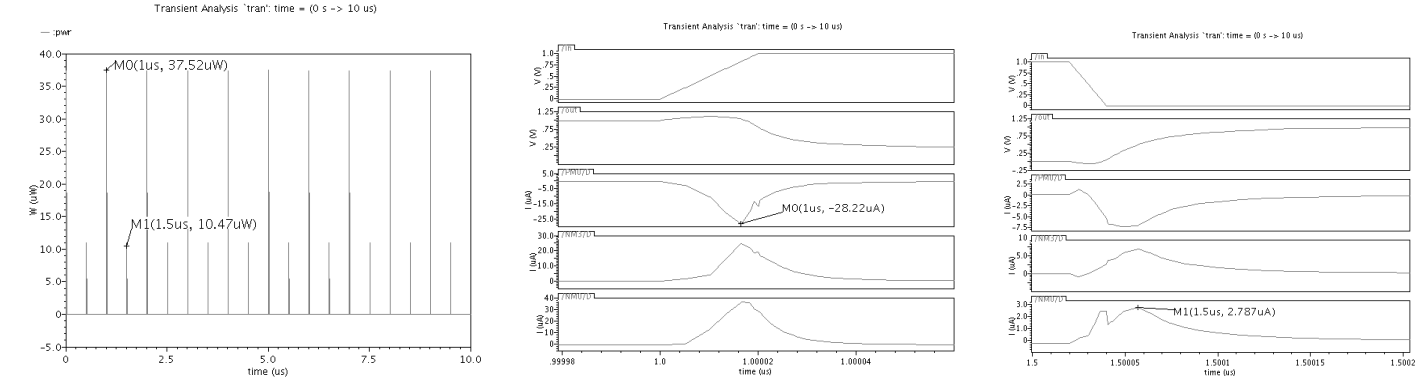
(a) (b) (c)

Figure.6: Proposed saturated NMOS inverter: (a) Transient analysis (b) Voltage transfer characteristics (c) Derivative of the VTC



(a) (b) (c)

Figure.6: Conventional CMOS inverter: (a) Transient power pattern (b) Low to high input transition (c) High to low input transition



(a) (b) (c)

Figure.7: Proposed saturated NMOS inverter: (a) Transient power pattern (b) Low to high input transition (c) High to low input transition

Figure 6(a) & 7(a) represents the power consumption during the transient analysis with a 1MHz input signal for the conventional & the proposed inverter respectively

Comparing Figure 6(a) & 7(a) it can be found that the power consumption during low to high transition & high to low transition of the conventional inverter are 43.47uw & 11.71uw respectively & for the proposed inverter it is 37.52uw & 10.47uw respectively. Hence in case of the proposed inverter the power consumption is reducing significantly. The reduction in power consumption is because of the reduction in the drain current which is due to the blockage by the saturated NMOS. Comparing figure 6(b) & 7(b) it can be found that during a low to high input transition the drain current of PM0 goes minimum up to -36.75uA for conventional inverter whereas for the proposed inverter it goes minimum up to -28.22uA. Similarly comparing figure 6(c) & 7(c) it can be found that during a high to low input transition the drain current of NM0 goes maximum up to 5.965uA for conventional inverter whereas for the proposed inverter it goes maximum up to 2.787uA. Table 2 shows the average power consumption, power consumption during a rising & a falling input, and the maximum current flow during the rising & falling input for both the inverter.

Inverter type	Avg (nW)	Rise (uW)	Fall (uw)	Rise(uA)	Fall (uA)
Conventional	13.23	43.47	11.71	-36.75	5.965
Proposed	8.533	37.52	10.47	-28.22	2.787

Table 2: Comparison of power consumption

All the results shown above were for an input frequency of 1MHz. When the input frequency increases the reduction in power consumption decreases. Table 3 represents the reduction in power consumption by the proposed inverter in comparison to conventional inverter for different frequencies.

Frequency	0.1KHz	1KHz	10KHz	100KHz	1MHz	10MHz	100MHz	1GHz
Conventional inverter (nw)	12.56	12.56	12.56	12.62	13.23	19.3	80.07	692.8
Proposed inverter (nw)	7.669	7.67	7.678	7.755	8.533	16.31	93.05	837.9
Decrement of power (in %)	38.94	38.93	38.87	38.55	35.5	15.5	-16.21	-20.94

Table 3: Comparison of power consumption of conventional inverter & the proposed inverter at different frequency.

V. Conclusion

A three transistor based inverter is designed to reduce the overall power consumption by reducing the short-circuit current. It is found that the proposed saturated NMOS inverter reduces around 38% of power consumption for any input signal less than 100 KHz. It reduces around 35% of power consumption for a 1 MHz input signal. As the input signal frequency approaches 10 MHz the reduction in power consumption decreases to 15%. & finally for a 100 MHz signal the power consumption increases about 16%. Hence it can be concluded the proposed inverter is advantageous for an operating frequency less than 10MHz.

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