A Fixed Frequency Dual-Mode DC-DC Buck Converter with Fast-Transient Response and High Efficiency Over a Wide Load Range

Somnath Maity and Y. Suraj

***Abstract*—Maintaining high efficiency and achieving fast dynamic response over wide load condition are extremely important in most modern power management applications, and also for various typical load demands. In this paper, we present the design of a fixed frequency hysteretic current (FFHC) controlled dual-mode tri-state dc-dc step-down (Buck) switching regulators/converters for wide load variation. Depending on the load requirements, it can adaptively switch between two operating modes — pseudo-continuous continuous mode (PCCM) to discontinuous conduction mode (DCM) and adjust the switching frequency of operation accordingly. Moreover, based on simplified discretized model or map, we also show that under certain conditions the proposed dual-mode tri-converter is not only useful for achieving the fast dynamic responses under wide load range, but also improve the power conversion efficiency, especially, at light load condition.**

***Index Terms*—Tri-state dc-dc converter, discrete-time modeling, fixed frequency hysteretic current control (FFHC), efficiency, fast-scale instability.**

I. Introduction

Higher power conversion efficiency over wide load range is required to power todays power managed Integrated Circuits (ICs) and loads to achieve energy savings and longer battery life in battery powered applications especially in cellular phones, PDAs, GPSs, etc. In these applications, load conditions usually change drastically from high to low power levels [1]. Since these devices operate at light load or stand-by mode for most of the time, the improvement of light-load (stand-by mode) efficiency of these power management ICs is important for extending battery life. Moreover, along-with the high efficiency, dc-dc converter with tight steady-state and dynamic performances specifications with smaller size and lower cost are also very important related issues [2].

In recent times, several power management techniques such as pulse frequency modulation [3], [4], pulse-skip [5], [6], bulk-voltage reduction [], phase-shedding [7], and burst mode operation [8], [9] have been proposed, and successfully implemented in order to make the efficiency curve of the dc-dc converters flatter. Although the described techniques have shown their improved efficiency at load efficiency, but they suffer from some major drawbacks that limit their uses in various area of applications. For example, a major problem of reducing the switching frequency at light loads is an increased current ripple caused by the increased volt-second product in the core of the output filter inductor. This increase in the ripple current has an adverse effect on the efficiency because it increases the conduction loss. Also they may lead to poor output voltage regulation and electromagnetic interference (EMI) concerns due to the load dependence of switching frequency f_s. While in bulk voltage reduction and stage-shedding techniques, the dynamic performance specifically the ability to restore full-power capability without output disturbance or other performance deterioration when the load suddenly changes from light load to full load. On the other hand, it is known that the efficiency of the fixed frequency PWM voltage-mode o current-mode controller becomes limited as switching frequency increases. The control system can have high efficiency at heavy loads as the conduction loss is kept low by using low resistance of power switches. However, since the increasing value of switching loss dominates at high switching frequency, efficiency decreases drastically when the load gradually decreases to no load condition. In addition, high switching frequency may cause to deteriorate the performances, accuracy and the stability of the power converter due to limited response time of the inductor current sensor and presence of high switching noise [10]. Although these shortcomings are easily eliminated by operating the converter at relatively low switching frequency, however it may cause an increase in output voltage ripple and low efficiency [11], and also has a strong impact the dynamic and steady-state performances of the voltage regulator due to fast-scale instability, which are important for many ICs operation. In last two decades, many research efforts have been devoted to predict the border of occurrence of such instabilities [12] in dc-dc converter. However, most of the reported analysis is based on discrete-time models, which are indeed very powerful to accurately predict the fast-scale instability, but are complex, and not very suitable to obtain clear design-oriented of stability analysis in terms of the circuit parameters. So far only few works on such design-oriented instability prediction for complete parameter space have been reported for closed-loop dc-dc converter [13].

With this view, we attempt to provide a design-oriented study of tri-state dc-dc converter by using a simplified discrete-time model, where the controller is implemented by using the concepts of both selective frequency hopping techniques [14], [15] and fixed frequency hysteritic current (FFHC) control logic. The objective of such combined system is that it not only provides high efficiency due to multiple operation modes but also exhibits fast transient response [16] and stable period-1 operation over a wide load range. In order to show this, the paper is organized as follows. Section II presents

a descriptive modeling of the proposed controller and its operating principle. While the simplified discretized model is derived in Section III. Based on this modeling approach, we have also shown how the control system can exhibit different kinds of periodic and aperiodic behaviors under wide load variation. Moreover, in Section IV we deal their effects on both steady state and dynamic performances, and power conversion efficiency. Finally, a conclusion is made in Section V.

II. Frequency Hopping Based FFHC-Controlled DC-DC Buck Converter

A. Controller Architecture

The schematic diagram of FFHC-controlled tri-state buck converter is shown in Fig. 1. It consists of an inductor L, a capacitor C, a load resistance R, a conduction loss series resistance r, ESR of the capacitor r_c, an uncontrollable switch D, and two controllable switches Q_1 and Q_2. Here, the switching logic is implemented by nested two-loop feedback controller. The slow outer voltage controller is used to generate the quasi-stationary boundary layers of the hysteresis loop. This is achieved by obtaining the equivalent reference current signals $i^+_{\rm ref}$ and $i^-_{\rm ref}$ as a linear combination of the output capacitor voltage v and a reference voltage $V_{\rm ref}$ in the form

$$i^+_{\rm ref} = k_p(V_{\rm ref} - v), \quad \text{and} \quad i^-_{\rm ref} = i^+_{\rm ref} - \Delta \tag{1}$$

where k_p is the gain of the proportional controller, and Δ is the bandwidth between $i^+_{\rm ref}$ and $i^-_{\rm ref}$. While the fast inner current controller is used to generate the binary control signal $u \in (0,1)$ where $u = (u_1 \quad u_2)^T$, by comparing the sensing inductor current i with two threshold reference currents $i^+_{\rm ref}, i^-_{\rm ref}$ and an externally generated clock pulse of time period T. Here, T is chosen based on the selective load current i_o approximately within the range $i_o < 10\%$, $10\% < i_o < 25\%$, and $\leq$ 100% load (normally categorized as light, medium and heavy load), which are often used to meet off-line target efficiencies requirement [17].

However, for a particular loading condition, the switching frequency T is fixed. During that mode, the inductor current i raises at the starting of every clock cycle with switch Q_1 being turned ON. When this i reaches a peak value of $i^+_{\rm ref}$, the Q_1 is turned OFF. The diode D is turned ON and the inductor current i starts falling until it reaches $i^-_{\rm ref}$. The switch Q_2 is turned ON when i reaches $i^-_{\rm ref}$ and remains ON until the arrival of the next clock pulse. If i reaches the next clock pulse without a nonzero value without intersecting $i^-_{\rm ref}$, the operation is said to be in continuous conduction mode (CCM), otherwise in pseudo-continuous conduction mode (PCCM). But if i reach zero value before the next clock cycle, with switch D being turned OFF, the operation is said to be in discontinuous conduction mode (DCM). This mode of operation may occurs when the boundary layers currents $i^+_{\rm ref}$ and $i^-_{\rm ref}$ become negative. In this case, it can only happen when the load requirement is very low.

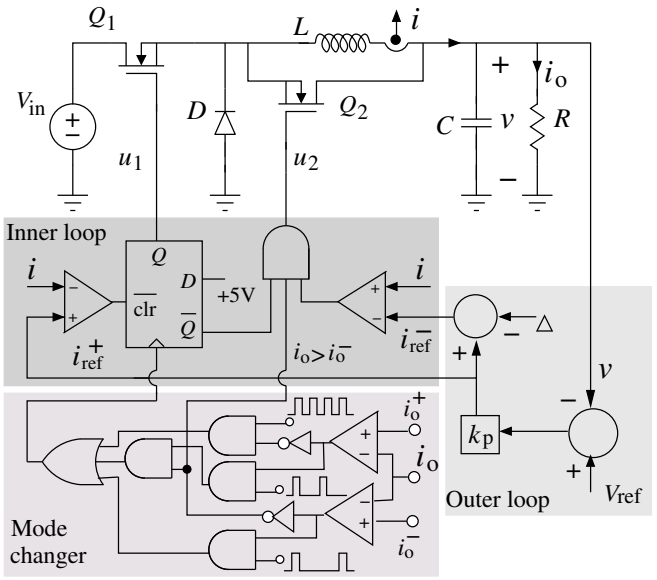

Fig. 1. Schematic diagram of the dual-mode FFHC controlled tri-state buck converter.

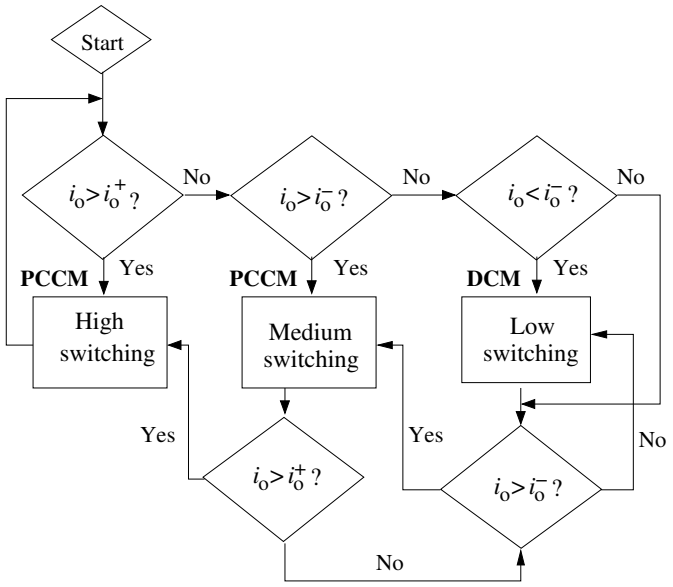

Fig. 2. Flow digram of dual-mode operation with frequency hopping.

B. Principle of Frequency Hopping Operations

For high-switching operation, power conversion efficiency decreases drastically when load current changes from heavy to light. The dual-mode technique needs to hop switching frequency to find a trade-off between power conversion efficiency and output voltage ripple when load current decreases [25]. This frequency hopping can be achieved by sensing the load current $i_{\rm o}$ of the converter system with a simple "mode changer' circuit (see Fig.1). The principle of such frequency hopping operation is shown in Fig. 2. It shows that if $i_{\rm o}$ is greater than the predefined threshold value $i^+_{\rm o}$, the system operates in heavy load condition with a higher

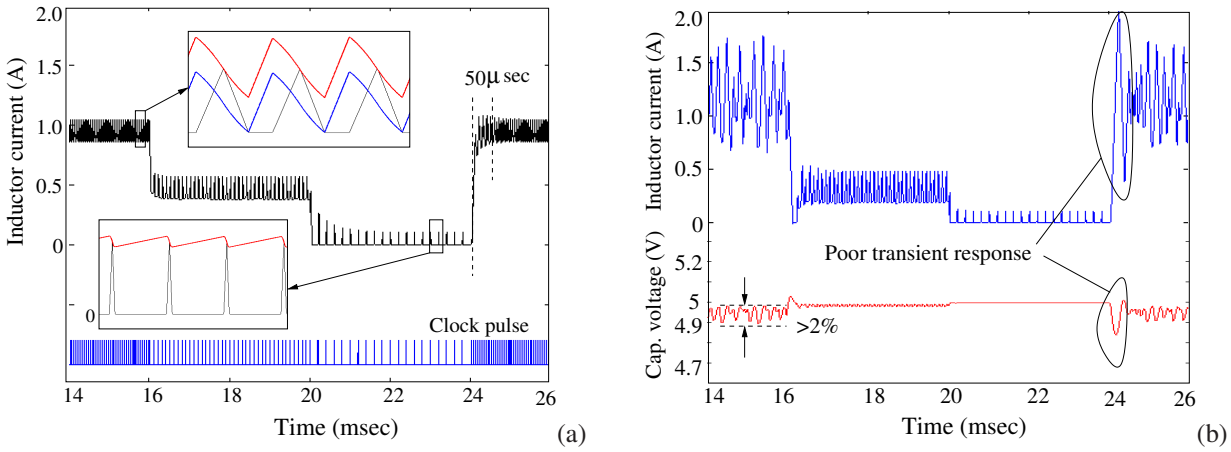

Fig. 3. The dynamic performances of dual-mode tri-state buck converter at (a) $i_{\rm o}$ = 0.667 A (full load) and 25% and 0.8% of full load condition; and at (b) $i_{\rm o}$ = 1.0 A and 18%, 3% of $i_{\rm o}$ with corresponding switching frequency 20, 10, and 5 kHz. The other parameters value are $V_{\rm in}$ = 10 V, $V_{\rm ref}$ = 5 V, L = 500 μH, C = 600 μF, Δ = 0.1 and (a) k_p= 10, (b) k_p = 40.

value of switching frequency. However, if $i_{\rm o}$ lies between $i_{\rm o}^+$ and $i_{\rm o}^-$, the system operates in medium load condition and switching frequency will be automatically adjusted and set to lower value than that of heavy-load condition. While for light-load condition, i.e., $i_{\rm o} < i_{\rm o}^-$, the switching frequency will be reduced further, to improve the light load efficiency of the system. Here, the threshold currents $i_{\rm o}^+$ and $i_{\rm o}^-$ are approximately chosen as 25% and 10% of the full load current.

In addition, depending on the load requirement, the desired switching frequency should be selected in such a way that the mode changer circuit will drive the converter to operate either in DCM for light load, or in PCCM for heavy or medium load condition [see Fig. 2]. The main idea of using such controlled converter is not only to improve the efficiency over wide load variation, but also to enhance the performance of the system in term of steady state and transient response under frequent load fluctuation. The tri-state converters under FFHC control were found to exhibit a fast transient response and larger stable operating region than the conventionally used peak current-mode controller [16]. However, there is a boundary value of circuit parameters, beyond that critical value, the converters may loose their stability and show some random noise-like chaotic waveform, which are inherently making causes to increase the ripple amplitude, thus, increases the conduction losses. Therefore in order to show such dynamic performances during nominal period-1 and aperiodic mode of operations, we numerically simulate the proposed converter over a wide range of operating condition. Fig. 3 shows that although converter shows the faster transient response ($\leq$ 50 μsec) and smaller ripple magnitude (for example, voltage ripple $\Delta v \leq 0.35\%$) in stable period-1 mode, however its dynamic response and ripple magnitude ($\Delta v > 2\%$) deteriorate drastically in aperiodic mode of operation, especially, at heavy load condition [see Fig.3(b)]. It is therefore a great importance to be able to analyze and predict such instabilities to extract the best optimized performance in terms of stability and dynamic behavior of the proposed controlled converter.

The averaged models are unable to predict such fast-scale instabilities due to inherent elimination of the switching action from the circuit description by averaging the state variable over the switching cycle. Although improved averaged model by adding ripple information, such as multifrequency averaged model [18], [19] are accurate enough, but still difficult to use for obtaining a complete design-oriented stability analysis in term of the circuit parameters.

III. Prediction of Fast-Scale Instability Using Simplified Discrete-Time Modeling

A. Order of the Converter System

With this view, we attempt to provide a design-oriented study of tristate buck converter by using simplified discrete-time averaged model. It can be easily derived by observing the dynamic of the system, especially, the inductor current over a complete switching cycle T when it operates either in PCCM or in DCM in nominal operation condition. During these modes of opeartion, converter toggles between three linear circuits and each of them is governed by first-order linear differential equation, given by

$$\frac{dx}{dt} = \begin{cases} A_1 x + B_1 V_{\rm in} \ \forall \ nT \leq t < nT + d_1 T \\ A_2 x + B_2 V_{\rm in} \ \forall \ nT + d_1 T \leq t < nT + d_2 T \\ A_3 x + B_3 V_{\rm in} \ \forall \ nT + d_2 T \leq t < (n+1)T \end{cases} \tag{2}$$

with output voltage dynamics

$$v = \left[\frac{R}{R + r_c} + \frac{R r_c}{R + r_c} \right]^T x. \tag{3}$$

where

$$A_1 = A_2 = \begin{pmatrix} \frac{-1}{C(R+r_c)} & \frac{R}{C(R+r_c)} \\ \frac{-R}{L(R+r_c)} & \frac{-(r+R \parallel r_c)}{L} \end{pmatrix},$$

$$A_3 = \begin{pmatrix} \frac{-1}{C(R+r_c)} & \frac{R}{C(R+r_c)} \\ 0 & -\frac{r}{L} \end{pmatrix},$$

$$B_1 = \begin{pmatrix} 0 \\ 1/L \end{pmatrix},\ B_2 = B_3 = \begin{pmatrix} 0 \\ 0 \end{pmatrix},\ x = (v_c \quad i)^T,$$

and d_1 and d_2 are the ON-time and OFF-time duty ratios.

However, it has been observed that under some situation the FFHC-controlled converter may operate in all three modes such as CCM , PCCM and DCM [16].

In order to operate the converter in PCCM, we need to calculate first the critical hysteresis bandwidth $\Delta^c = i^+_{\rm ref} - i^c$ (i_c is the n-th instant inductor current at the edge of CCM operation) as shown in Fig. 4. Here, Δ^c is the boundary condition between two isolated converter topologies CCM and PCCM respectively. If the inductor current ripple Δ less than this critical value Δ^c, the converter operates in PCCM, otherwise it operates in CCM. Considering the initial position of state variables at $t = nT+dT$ as $\begin{bmatrix} V_c & i^+_{\rm ref} \end{bmatrix}^T$ (V_c represents the steady-state capacitor voltage and d is the steady-stae duty ratio during CCM) and solving the solution of subsystem equation M_2 based on first-order approximation, the critical inductor current i^c can be easily expressed as a function of on/off switching instants inductor current $i(dT)$ as

$$i^c = i^+_{\rm ref} - \frac{r(1-d)T}{L} i^+_{\rm ref} - \frac{d(1-d)T}{L} V_{\rm in} \tag{4}$$

where $i(dT) = i^+_{\rm ref}$ and $i^+_{\rm ref}$ is the upper boundary function defined by $i^+_{\rm ref} = k_p(V_{\rm ref} - v)$. Further substitution of $i^+_{\rm ref}|_{t=dT} \approx k_p(V_{\rm ref} - dV_{\rm in})$ into (4) therefore yields the critical condition

$$\Delta^c = \frac{rk_p(1-d)T}{L} V_{\rm ref} + \frac{d(1-d)T(1-rk_p)}{L} V_{\rm in} \tag{5}$$

When duty ratio d = 0.5, the value of (4) will be maximum. Thus, to ensure the converter operation in PCCM, one must choose Δ so that, the condition

$$\Delta < \Delta^c_{\rm max} := \frac{k_p rT}{2L} V_{\rm ref} + \frac{(1-rk_p)T}{4L} V_{\rm in} \tag{6}$$

is satisfied. In other words, in PCCM we can acheive maximum ripple current which is slightly laess than $\Delta^c_{\rm max}$. However, depending on the load requrement average inductor current I_o of the converter vary. This results the converter to switch from one mode to another. If the inductor current at the instant of every clock pulse i_n is identically zero, the mode of operation is said to be in DCM. While it said to be in PCCM if $i_n = I_{\rm dc} \neq 0$. As a result, the dynamics of the converter is dfined by only one state variable capacitor voltage, and the system becomes 1- dimensional (1-D).

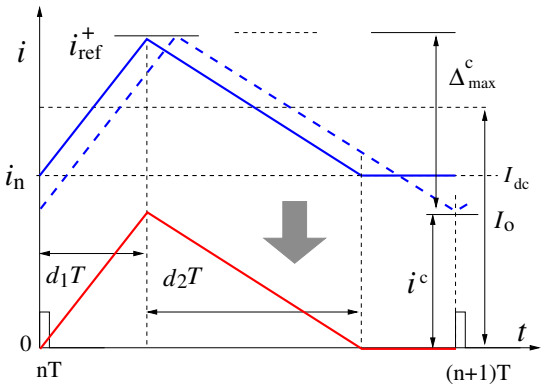

Fig. 4. Critical condition for PCCM operation.

B. Derivation of First-Order Discrete-Time Equation or 1-D Map

However, in order to derive the first-oder discrete-time equation or 1-D map, one need to expressed the n+1-th instant capacitor voltage $v_{c,n+1}$ as a function of previous instant value $v_{c,n}$, i.e., $v_{c,n+1} = f(v_{c,n})$. This can be easily achieved by stacking the consecutive solutions of each subsystem dynamics (2) over a complete switching cycle, as

$$x_{n+1} = \Phi x_n + \int_0^{d_1 T} e^{A_1(t-\tau)} B_1 d\tau. \tag{7}$$

where $\Phi = e^{[A_1 d_1 + A_2 d_2 + A_3(1-d_1-d_2)]T}$, d_1 and d_2 are the ON and OFF-time duty ratios. Due to presence matrix exponent component $e^{[A_1 d_1 + A_2 d_2 + A_3(1-d_1-d_2)]T}$, it is not possible to express the equation (7) in explicit form. However, it can be possible to express explicitly, if we approximate Φ by neglecting 3^{rd}+higher-order term and sequentially substitute the values of matrices [from equn.(2)] and duty ratios d_1 and d_2 into (7). Here duty ratios are related to the controlled currents and volt-sec relationship by

$$d_1 \approx \frac{L(i^+_{\rm ref} - I_{\rm dc})}{(V_{\rm in} - V_{\rm ref}))T} \ \text{ and } \ d_2 = \left(\frac{V_{\rm in}}{v} - 1\right) d_1 \tag{8}$$

where $I_{\rm dc} \approx I_o - \Delta/2 \approx V_{\rm ref}/R - \Delta/2$ [see Fig. 4]. Substituting (1) and (3) into (8), the closed-loop discrete-time model in term of capacitor voltage can be obtained using (7) as

$$v_{c,n+1} = \begin{cases} \alpha v_{c,n} - \beta V_{\rm in} d_1^2 \left(1 - \dfrac{V_{\rm in}}{v_{c,n}}\right) & \text{for } \ i_n = 0 \\ \alpha v_{c,n} - \beta V_{\rm in} d_1^2 \left(1 - \dfrac{V_{\rm in}}{v_{c,n}}\right) + \gamma i_n & \text{for } \ i_n = I_{\rm dc} \end{cases} \tag{9}$$

where

$$\alpha \approx 1 - \frac{T}{C(R+r_c)},\ \beta \approx \frac{RT^2}{2LC(R+r_c)},$$
$$\gamma \approx \frac{RT}{C(R+r_c)},\ \text{since } r,\ r_c,\ \frac{T^2}{R^2C^2} << 1.$$

Equation (9) is the well-known 2-D Poincaré return map. As we have mentioned before, since the inductor current assumes

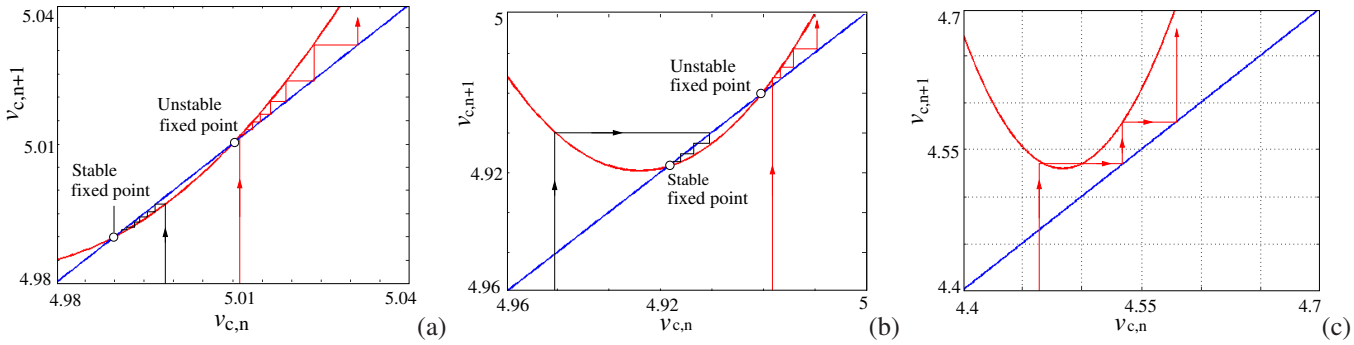

Fig. 5. 1-D Poincaré map illustrating the cause of more oscillation during transient state when converter oprates in: (a) DCM for 0.8% of full load and (b) PCCM at full load i_o = 0.667A, and (c) unstable operation in PCCM at extra heavy laod (i_o = 5 A). The parameters value are same as in Fig. 3.

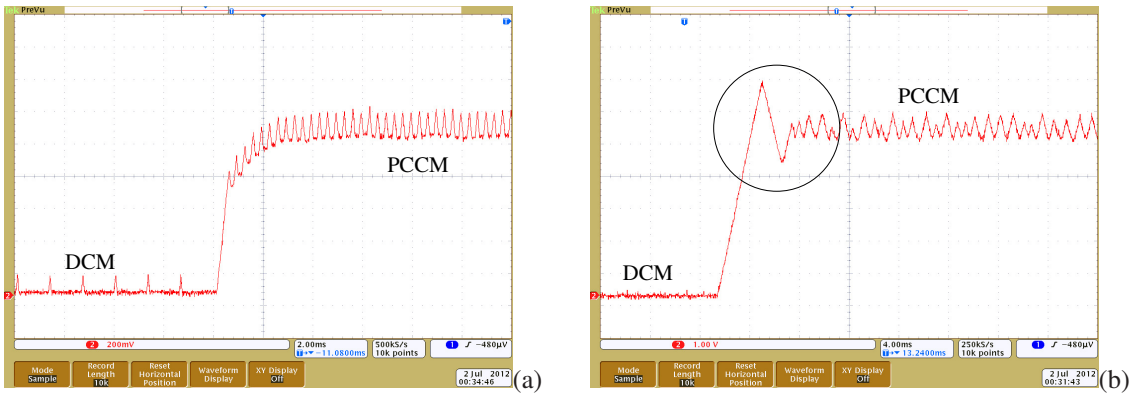

Fig. 6. Experimental confirmation of simulation results: (a) Fig. 5(a) and (b), and (b) Fig. 5(a) and (c).

the same value at the beginning as well as at the end of a clock period under the tristate operation, the point of instability can be accurately determined from the voltage dynamics alone. Hence, the 1-D voltage map is considered for stability analysis.

IV. Performance Analysis and Efficiency Measurement

A. Prediction of Dynamic Performances

Even though 1-D map can successfully predicts the fast-scale instability or subharmonic oscillation of voltage-mode [] and current-mode [] controlled buck converter, however, occurrence of such instability (through period doubling bifurcation and/or saddle-node bifurcation) are quite different. In the saddle-node bifurcation, a stable and an unstable solution may merge together, thereafter they disappear altogether as the converter parameter varies. This sudden disappearances or jumps of steady-state solutions may have an effect on system's behaviors in term of steady-state and transient responses. In fact, without any fast-scale instability, the system may show much more oscillatory behavior during transient state. Therefore it is important to investigate the cause of occurrence of such kind of instability, so that, practicing engineer can design the controller efficiently in order to fulfill the desired converter specifications satisfactorily.

To explore this, here we study the converter system using (9). We have seen that saddle-node bifurcation resulting the fast-scale instability can occur in FFHC-controlled buck converter, and also can be explained successfully by observing the characteristic of the 1-D Poincaré map. If map (9) does not intersect the unity slope line, system will become unstable; if it intersects the system will be stable or bistable depending on the nature of intersection points. Moreover, the nature of such points — stable point (when slope of the curve is less than 1) and unstable point (when slope is greater than 1), and initial value of the capacitor voltage $v_{c,n}$ together may affect the system's dynamics drastically. For example, if $v_{c,n}$ stay within the zone of attraction of stable fixed point, then, after finite numbers of iteration state will converge to it [see Fig. 5(a) and (b)]. However, if it stay within the attracting zone of unstable point, the state will eventually diverge and will move to a new stable attractor [see Fig. 5(c)]. As a result, ripple will increase and power conversion will decrease. Experimental validation of such different modes of operations and their stability status are shown in Fig 6.

B. Efficiency Measurement from Light-to Heavy-Load Condition

Since the amplitude and nature ripple (periodic or chaotic) play an important role on the stability and efficiency of the system, it is therefore necessary to estimate the fast-scale stability margin at the clock speed. The necessaty is not only usefull to achieve the best dynamic responses but also to improve the efficiency under wide load variation. Moreover, it

is also required to estimate the range of external parameters to ensure periodic operation without the onset of chaos. Because it enhances the ripple magnide.

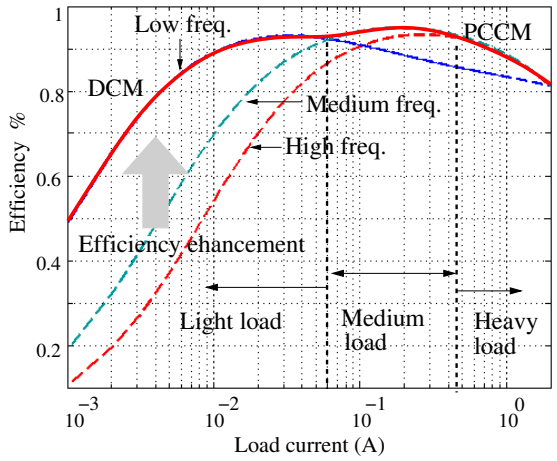

Fig. 7. Schetimodal switching operation.

In this system, we have seen that, even though the presence of the extra switch in PCCM deteriorates the efficiency of the system slightly, but its performance is enhanced considerably and ripples magnitude become smaller as compared to that in CCM. Even, efficiency can be maintained slightly better by carefully choosing low switching frequency as compared to the operation of the converter in CCM without losing the fast-scale instability. Similar methodology is followed in medium load condition. However, in case of light load condition, the system is operated in DCM. The system operating in DCM is known to show good transient performance. Furthermore, under the proposed control scheme, one could expect the higher efficiency, especially, in light load condition because of low ripple due to reduced operating frequency and low conduction loss as shown in Fig. 7. shows the load versus efficiency curve for wide load range condition.

V. Conclusion

Efficient power delivery has become a key element for the potable appliances to improve battery life and meet various dynamic and steady-state specifications. A fixed frequency hysteretic current control (FFHC) based tri-state buck converter is proposed to fulfill the requirements. Based on simplified discrete-time modeling or 1-D map, we have shown that FFHC-controlled buck not only deliver power efficiently under wide load variation, but also exhibit good dynamic performances. We also discuss, under certain load condition how the performances can deteriorates. However, still much more analysis are required since the energy efficiency requirements continues to tighten. Moreover the proposed system also needs to be validated by fulfilling all the specifications for real-life Integrated Circuits (ICs) implemetation.

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