An Analytical Surface Potential Modeling of Fully-Depleted Symmetrical Double-Gate (DG) Strained-Si MOSFETs Including the Effect of Interface Charges

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***Abstract*—A two-dimensional (2D) surface potential model for a fully-depleted symmetrical double-gate strained- Si MOSFET damaged with oxide interface charges is being proposed. The damage due to the hot carrier effect, is a common phenomenon in short-channel devices. The parabolic potential approximation is utilized to solve 2D Poisson's equation in the channel region. The developed surface potential model incorporates the effect of both positive as well as negative interface charges. The effects of interface charge density, extent of the damaged region and the strain variations in the channel region on the surface potential have been studied comprehensively. The model results are in reasonable agreement with simulation results of ATLAS™, a numerical simulator by Silvaco Inc.**

***Index Terms*--Carrier mobility, Double Gate (DG), Drain Induced Barrier Lowering (DIBL), Hot Carrier Effect (HCE), Interface Charge, Silicon on Silicon-Germanium, Strained Si.**

I. Introduction

As the scaling of the conventional CMOS becomes a challenge in sub-50nm regime due to short channel effects (SCEs), various non conventional device structures have been evolved to counter it [1], [2]. Among them, the double-gate (DG) MOSFETs are the front runners with the short-channel effect (SCE) immunity, high transconductance and ideal subthreshold performance [3]. The scalability of DG MOSFETs has been extended further with the incorporation of strain in the channel region. This is verified by Li Jin *et al.* [4]. But as the carrier velocity increases due to strain, higher lateral electric field give rise to hot carriers [5]. Further due to higher vertical electric field these hot carriers may also be trapped in the oxide region of MOSFETs. Thus, trapped charges in the oxide region of MOSFETs change the potential profile of the channel and have disastrous effects on further scaling by shifting the threshold voltage. Hence, the effect analysis of hot carriers becomes one of the most crucial tasks [5], [6].

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This paper presents an analytical model of surface potential for short-channel symmetrical double-gate (DG) strained-Si MOSFETs including the effects of the interface charges. The parabolic potential approximation method is utilized while solving the two-dimensional (2D) Poisson's equations along with the assumption that the interface charge distribution is uniform along the channel [5], [7], [8]. The simulation results from ATLAS™ are utilized to verify the obtained model [9].

II. Device Structure

Fig. 1 shows the cross section of the fully-depleted symmetrical DG strained-Si MOSFET with the interface charges. The biaxial strain in the channel is obtained by either mechanical means or by growing a silicon layer over a thin relaxed $Si_{1-x}Ge_x$ wafer. Here we consider a very thin layer of $Si_{1-x}Ge_x$ over which Si is pseudo-morphically grown. The $Si_{1-x}Ge_x$ layer is neglected in the shown figure to keep the analytical model simple whereas its effect of strain in Si layer is considered.

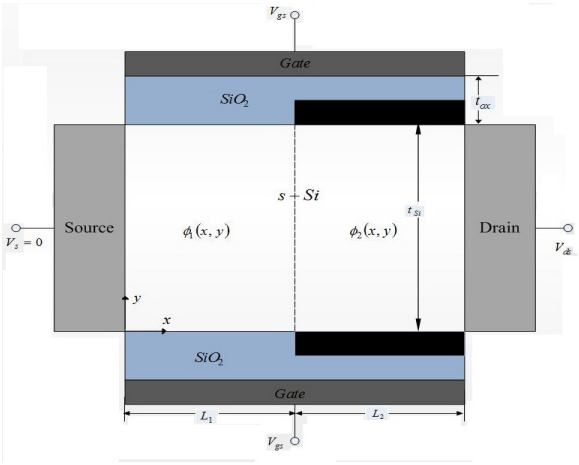

Fig.1. Cross sectional view of DG s-Si MOSFET

The strained channel region, below the interface charges which is shown by dark shade, is here on considered as the damaged region and the corresponding channel length as

damaged length L_2. Undamaged channel length is L_1 whereas total channel length is $L = L_1 + L_2$. The thickness of the strained-Si layer is t_{s-Si} and that of oxide is t_{ox}. The interface charge has a concentration of N_f cm^{-2} whereas the channel is doped with N_a cm^{-3}. The channel is inverted with the gate potential of V_G and the drain current is driven by a drain potential of V_D.

III. Strain Modeling

Fig. 2 displays the change in silicon energy band structure because of biaxial strain in the silicon channel. The device simulator model library of ATLAS™, thus, has been modified according to the effects of strain on the Si band structure [10]. The effects of strain on the Si band structure can be modelled as

$$\Delta E_C = 0.57X \quad (1)$$

$$\Delta E_g = 0.4X \quad (2)$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X \quad (3)$$

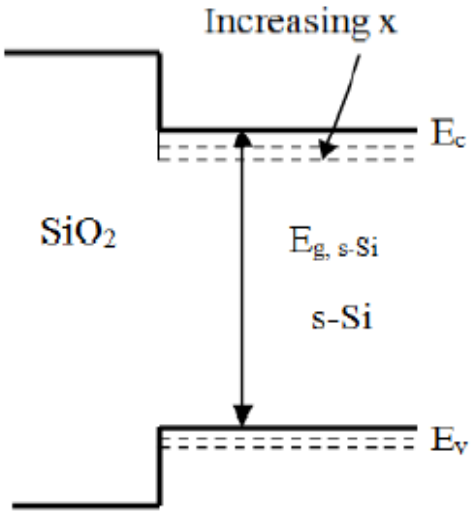

Fig. 2. Modified Silicon Band Structure due to strain

Where, X is the Ge mole fraction in the $Si_{1-X}Ge_X$ substrate; ΔE_C is change in the conduction band energy due to strain; ΔE_g is the decrease in the band gap of silicon due to strain; V_T is the thermal voltage; $m^*_{h,Si}, m^*_{h,s-Si}$ are the hole effective masses; $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states in the valence band in normal and strained silicon, respectively and q is the electronic charge.

The effect of strain on the channel flat-band voltage can be modeled as

$$(V_{FB})_{s-Si} = (V_{FB})_{Si} + \Delta V_{FB} \quad (4)$$

Where, $(V_{FB})_{Si} = \phi_M - \phi_{Si}$ (5)

and, $\Delta V_{FB} = -\frac{\Delta E_C}{q} + \frac{\Delta E_g}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$ (6)

ϕ_M, ϕ_{Si} are the metal work function and the unstrained silicon work function respectively, where ϕ_{Si} is

$$\phi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_{f,Si} \quad (7)$$

$$\phi_{f,Si} = V_T \ln\left(\frac{N_a}{n_i}\right) \quad (8)$$

Where, χ_{Si}, E_g, $\phi_{f,Si}$, n_i are the electron affinity, band gap energy, the Fermi potential and intrinsic carrier concentration of the unstrained Silicon respectively.

The built-in voltage across the source-body and drain-body junctions in the strained-Si thin film is also affected by strain as

$$V_{bi,s-Si} = V_{bi,Si} + \Delta V_{bi} \quad (9)$$

Where, $V_{bi,Si} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right)$ (10)

and $\Delta V_{bi} = -\frac{\Delta E_g}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$ (11)

ΔV_{bi} is the change in the built in potential due to strain.

IV. Modeling of the Surface Potential

The potential distribution of undamaged and the damaged regions are taken as as $\phi_1(x,y)$ and $\phi_2(x,y)$ respectively. To obtain these potential variations, the 2D Poisson's equations are solved for the two regions.

$$\frac{\partial^2 \phi_k(x,y)}{\partial x^2} + \frac{\partial^2 \phi_k(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}}, \; k = 1,2 \quad (12)$$

Where ε_{Si} is the permittivity of the silicon. The potential distributions in the two regions are approximated by parabolic approximation as

$$\phi_k(x,y) = P_{0k}(x) + P_{1k}(x)y + P_{2k}(x)y^2, \; k = 1,2 \quad (13)$$

The equality of the potential and continuity of the electric field across the interface of undamaged and damaged regions are:

$$\phi_1(L_1,0) = \phi_2(L_1,0) \quad (14)$$

$$\left[\frac{\partial \phi_1(x,y)}{\partial x}\right]_{x=L_1} = \left[\frac{\partial \phi_2(x,y)}{\partial x}\right]_{x=L_1} \quad (15)$$

Electric flux at SiO_2/s-Si interface is continuous in the front and the back gate interface:

$$\left[\frac{\partial\phi_k(x,y)}{\partial y}\right]_{y=0} = \frac{C_{ox}}{\varepsilon_{Si}}\left[\phi_k(x) - V_{gs} + V_{FBk}\right] \quad (16)$$

$$\left[\frac{\partial\phi_k(x,y)}{\partial y}\right]_{y=t_{s-Si}} = -\frac{C_{ox}}{\varepsilon_{Si}}\left[\phi_k(x) - V_{gs} + V_{FBk}\right] \quad (17)$$

with $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ (18)

and $\phi_k(0,x) = \phi_k(t_{s-Si},x) = \phi_k(x)$ (19)

where $\phi_k(x)$ is the desired surface potential. The flat band voltages are given as

$$(V_{FB1})_{s-Si} = (V_{FB})_{Si} + \Delta V_{FB} \quad (20)$$

$$(V_{FB2})_{s-Si} = (V_{FB})_{Si} + \Delta V_{FB} \pm qN_f / C_{ox} \quad (21)$$

Where, $\pm qN_f$ represents the amount of charge of both polarity (positive/negative) trapped in the oxide.
Solving the Poisson's equation with the aforementioned boundary conditions, we get

$$P_{0k}(x) = \phi_{bk}(x) = \phi_{fk}(x) = \phi_k(x) \quad (22)$$

$$P_{1k}(x) = \frac{C_{ox}}{\varepsilon_{Si}}\left[\phi_k(x) - V_{GS} + V_{FBk}\right] \quad (23)$$

$$P_{2k}(x) = -\frac{C_{ox}}{\varepsilon_{Si}t_{s-Si}}\left[\phi_k(x) - V_{GS} + V_{FBk}\right] \quad (24)$$

The potentials at the source and drain end can be given by

$$\phi_1(0,0) = V_{bi,s-Si} \quad (25)$$

$$\phi_2(0,L) = V_{bi,s-Si} + V_{DS} \quad (26)$$

Solving the Poisson's equation at the oxide semiconductor interface, we get a differential equation in $\phi_k(x)$ as

$$\frac{d^2\phi_k(x)}{dx^2} - \alpha\phi_k(x) = \beta_k \quad (27)$$

Where,

$$\alpha = \frac{2C_{ox}/C_{s-Si}}{t_{s-Si}^2} \quad (28)$$

$$\beta_k = \frac{qN_{As-Si}}{\varepsilon_{s-Si}} - \frac{2C_{ox}}{\varepsilon_{s-Si}t_{s-Si}}\left[V_{GS} - V_{FBk}\right] \quad (29)$$

Final expression of surface potential can be given as

$$\phi_{s1} = \frac{\psi_{d1}\sinh(\eta x) - \psi_{s1}\sinh\left(\eta(x-L_1)\right)}{\sinh(\eta L_1)} - \sigma_1 \quad (30)$$

$$\phi_{s2} = \frac{\psi_{d2}\sinh\left(\eta(x-L_1)\right) - \psi_{s2}\sinh\left(\eta(x-L)\right)}{\sinh(\eta L_2)} - \sigma_2 \quad (31)$$

$$\eta = \sqrt{\alpha} \quad (32)$$

$$\sigma_i = \frac{\beta_i}{\alpha} \quad (33)$$

$$\psi_{s1} = V_{bi,s-Si} + \sigma_1 \quad (34)$$

$$\psi_{d2} = V_{bi,s-Si} + V_{DS} + \sigma_2 \quad (35)$$

$$\psi_{d1} = V_p + \sigma_1 \quad (36)$$

$$\psi_{s2} = V_p + \sigma_2 \quad (37)$$

$$V_p = \frac{\psi_{d2}\cos ech(\eta L_2) + \psi_{s1}\cos ech(\eta L_1)}{\coth(\eta L_1) + \coth(\eta L_2)} - \frac{\sigma_1\coth(\eta L_1) + \sigma_2\coth(\eta L_2)}{\coth(\eta L_1) + \coth(\eta L_2)} \quad (38)$$

$\eta, \psi_{s1}, \psi_{s2}, \psi_{d1}, \psi_{d2}, \sigma_1$ and σ_2 are the constants obtained from the boundary conditions mentioned above.

TABLE 1
DEVICE PARAMETERS USED IN THE SIMULATION

Parameters	**Value**
Ge mole fraction in SiGe substrate	0-0.2 (0-20%)
Source /Drain doping	10^{20} cm^{-3}
Channel doping	$10^{18}cm^{-3}$
Channel length	30 nm
Oxide thickness	2 nm
Gate Metal work function	4.8eV
Strained Si film thickness	10 nm
Gate Bias	0.3 V
Interface trapped charges	$\pm 5x10^{12}cm^{-2}$

V. RESULTS AND DISCUSSIONS

A comparison is made here between the analytical model results and the numerical simulation data extracted from simulation of the device structure under consideration, from a commercially available 2D device simulator ATLAS™ by Silvaco Inc. All the required modifications are made in the ATLAS library to include the effects of strain as discussed in Sec. II. Field dependent mobility model, drift-diffusion model for carrier transportation and SRH recombination are utilized for the structure simulation. The coupled partial differential equations were solved using Newton's method. The model results are in excellent agreement with the simulation results as shown in Figs. 3, 4 and 5.

Figure 3 shows the surface potential variation along the channel length for various amounts and polarity of interface trapped charges in the oxide. As observed from the figure, the minimum of the surface potential is at the channel center for an undamaged device and is moving towards the source and drain, respectively for positive and negative interface charges.

It is clear that positive interface charge will impose higher short channel effect over the device than its negative charge counterparts because of higher barrier height. However negative interface charges will cause more drain induced barrier lowering (DIBL) effect as the minimum potential point
shifts towards the drain end. So both positive and negative interface charges are detrimental to the device operation.

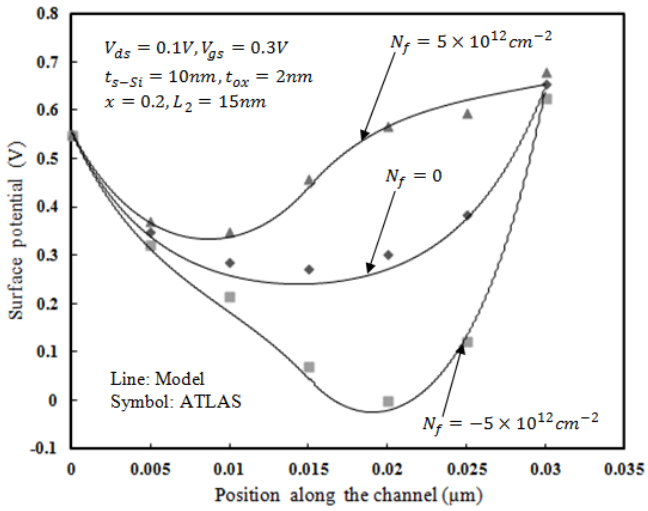

Fig. 3. The surface potential for charge variations (in magnitude and polarity)

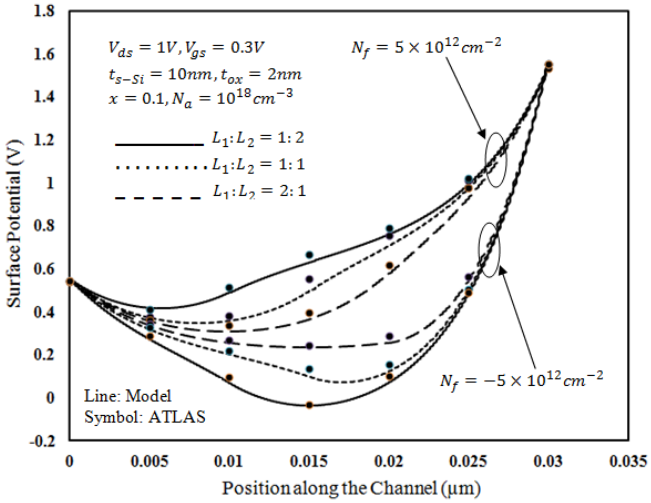

Fig. 4. The surface potential profile along the channel length for different length ratio (L_1:L_2) of undamaged and damaged region

Fig. 4 depicts the surface potential with the damaged region length variation for both positive and negative charges in the oxide interface. As seen for the positive interface charges, the increase in the extent of the damaged region length raises the minimum surface potential and shifts it towards the source side and the position of the minimum surface potential is closer to source for a greater length of the damaged region than lesser damaged region length. This indicates a higher SCE in the device as the damaged region extends more. This will further lead to lower source-channel barrier height and hence a higher threshold voltage roll-off. But in the case of negative interface charges, the increase of the damaged region decreases the minimum surface potential. This causes a higher source-channel barrier height and hence a lower threshold voltage roll-off. The shifting of the minimum surface potentials are same as that of in the positive interface charge case but the only difference is that, the distance between source and minimum surface potential positions are more in negative interface charge case than their positive counterparts.

Fig. 5 shows the surface potential variations immunity to drain voltage (V_{ds}) variations at different amount of strain in the channel (X). For $X = 0$, the change in the drain voltage changes the minimum surface potential to a considerable extent $(\approx 18\text{mV})$, whereas for $X = 0.2$, this change in minimum potential gets lower $(\approx 14\text{mV})$ as observed. Thus applying higher strain in the channel, we may obtain better immunity to the DIBL along with higher mobility of the carriers.

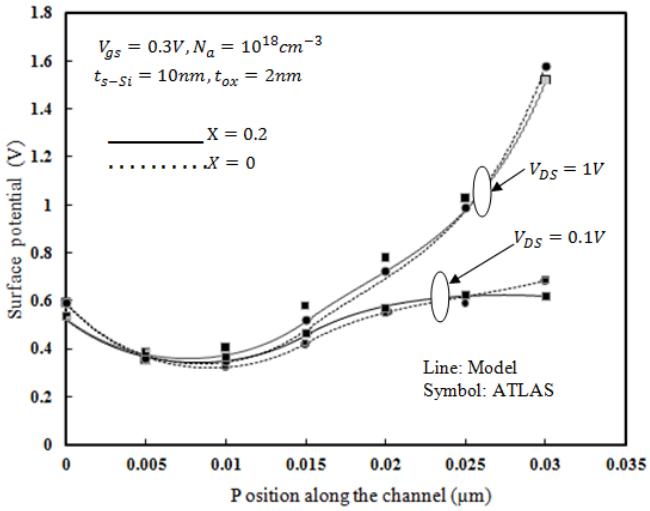

Fig. 5. Surface Potential along the channel length for different drain voltage and mole fraction variation

VI. Conclusions

An analytical surface potential model has been developed for the short-channel DG s-Si MOSFET which is damaged due to interface charges generated by hot carriers. The effects of the polarities of interface charges, the undamaged to damaged length ratio (L_1:L_2), strain (X), and drain to source voltage on surface potential are studied. The accuracy of the proposed model was verified by the simulation results.

VII. Acknowledgment

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