A Power Improvement Technique for a Differential LNA

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***Abstract* – This work presents the design of an inductively source degenerated CMOS Differential Low Noise Amplifier (LNA) operating at 2 GHz. LNA is designed using UMC 0.18 µm technology and simulated in Cadence Spectre_RF tool to validate its performance. Power constrained methodology is used for the design of CMOS Differential Low Noise Amplifier. At 1.8V supply voltage, the designed LNA consumed 9mA current. The amplifier provides a power gain (S_{21}) of 22.53dB, noise figure (NF_{min}) of 1.845dB, $S_{11}\ of\ -9.781dB$, $S_{12}\ of\ -11.42dB$ and consumes 16.2mW of power.**

Keywords – Low Noise Amplifier (LNA), CMOS, noise figure (NF), power.

I. INTRODUCTION

The growth of wireless services and other telecom applications has pushed the semiconductor industry towards complete system-on-chip solutions. Wireless systems comprise of a front-end and a back-end section. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver. The main effect of the LNA is to amplify the faint signal which is received by the antenna. It should provide enough gain, low noise figure, high linearity, great input and output matching with restraint of power consumption [1].

Here a design of differential cascade LNA is presented. The LNA has a double-ended input and differential outputs to avoid an external balun for low cost communication. In Section II, The Source Degenerated LNA, Noise Figure and Differential LNA design are explained. Simulation results are discussed in section III, Section IV concludes this paper.

II. LNA DESIGN

A. Source Degenerated LNA

The L_s is the degeneration inductor. We can adjust the inductor to tit the variation of f_T, but f_T is so large that the value of the inductor will be less than 0.4nH, which is difficult to be implemented on chip [2] is shown in figure 1 and small signal equivalent circuit of Source Degenerated LNA is as shown in figure 2.

The capacitor C_{gs} is added between the gate of the MOSFET and source of MOSFET is as shown in figure 3. The use of C_{gs} capacitance is to increase the Source Degenerated inductor value, increase the noise figure, and reduce the power gain of LNA. Writing KCL and KVL equations for Source degeneration LNA

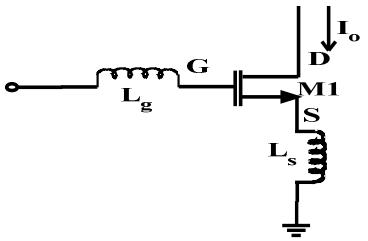

Fig. 1. Source Degenerate LNA

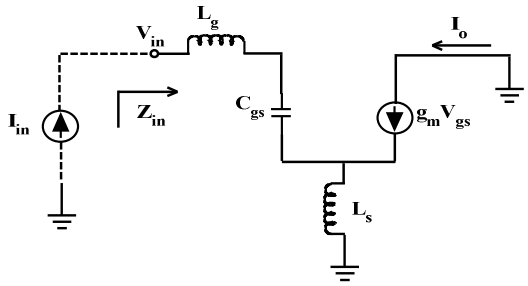

Fig. 2. Small signal equivalent circuit if Source Degenerated LNA.

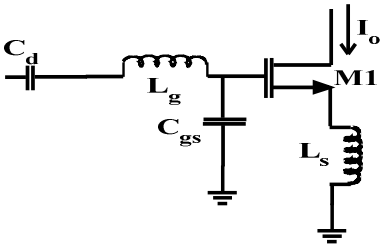

Fig. 3. Capacitor C_{gs} is added between the gate and source of the MOSFET

$$I_0 = g_m V_{gs} = I_{in} \times \frac{1}{sC_{gs}} g_m = \frac{g_m}{sC_{gs}} I_{in} \quad (1)$$

$$V_{in} = [s(L_g + L_s) + \frac{1}{sC_{gs}}]I_{in+} I_0 s L_s \quad (2)$$

Solving (1) and (2)

$$Z_{in} = \frac{V_{in}}{I_{in}} = s(L_G + L_S) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \quad (3)$$

$$Z_{in}(j) = j\left[(L_g + L_s) - \frac{1}{C_{gs}}\right] + \frac{g_m L_s}{C_{gs}} \quad (4)$$

Matching occurs when $Z(j\omega_0) = R_s . R_s$ is the resistor, which is associated in the input voltage source. That is

$$(L_G + L_s)_0 = \frac{1}{{}_0 C_{gs}} \quad (5)$$

$${}_0{}^2 = \frac{1}{(L_G + L_S) C_{gs}} \quad (6)$$

and

$$R_s = \frac{g_m l_s}{C_{gs}} \quad (7)$$

$$L_G = \frac{1}{{}_0{}^2 C_{gs}} - L_s \quad (8)$$

and

$$L_S = \frac{1}{{}_0{}^2 C_{gs}} - L_G \quad (9)$$

B. Noise Figure

The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF). It needs higher linearity and sufficient gain. The noise Factor is defined as:

$$F_{total} = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \cdots \quad (10)$$

Where F_n (n=1, 2, 3 …) is the noise factor of each stage, G_n (n=1, 2, 3…) is the gain of each stage.

C. Differential LNA

Differential circuits are an important part of integrated circuit design because they offer several important advantages over single-ended circuits [3]. In order to make the differential LNA circuit, two single-ended circuits built, where each transistor and circuit component has a complimentary transistor or component [4]. The first important advantage is the differential LNA offers a stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the differential LNA the measured results of one-half circuit are always taken with respect to other half circuit. Another significant and relevant benefit of using a differential circuit is noise reduction [5].

Inter-stage inductor with parasitic capacitance form impedance match network between input stage and cascoded stage boost gain lower noise figure. Input match condition will be affected. The circuit diagram of the Differential LNA is shown in Fig.4.

I. SIMULATION

The schematic of fully Differential LNA designed with 0.18µm technology is shown in Figure 5 [5]. We have simulated our design using Cadence spectre_RF tool on UMC 0.18 µm technology. Cadence EDA tools used are Virtuoso for Schematic Editing and Spectre for Simulation.

A. Simulation Results

The various simulation iterations are performed on the LNA circuit to meet design requirements. The simulation results of

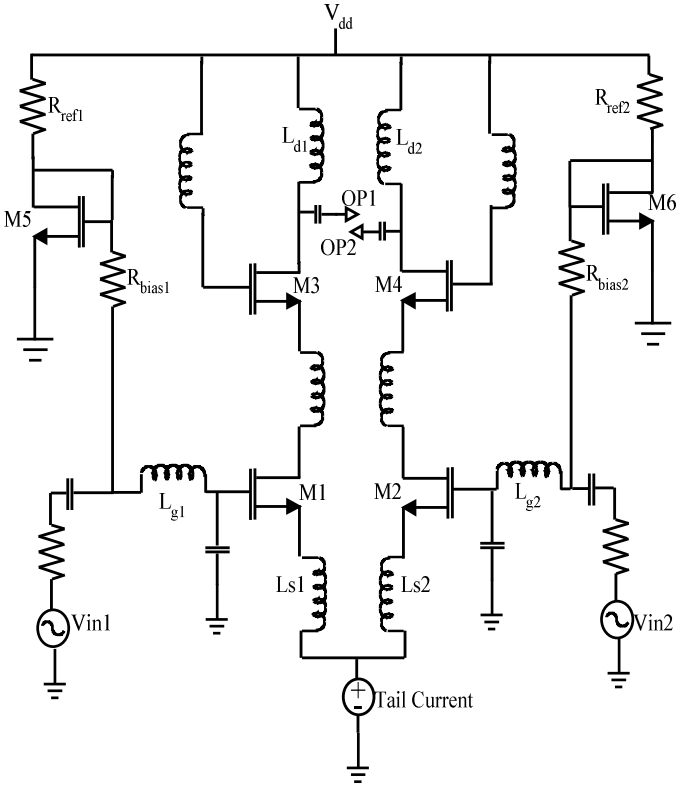

Fig. 4. Differential LNA

Differential LNA achieved at the typical process are summarized in the Table I.

B. Simulation Figures

After the simulation of the Differential LNA at 2GHz frequency we obtained various results which are shown in the below figures. In order to meet power consumption requirement, we have to adjust the DC bias accordingly. To achieve required values for Noise Figure (NF_{min}), Gain, IIP3 and S_{11}, we have adjusted the sizes of transistors, inductors and capacitors. As is shown, figure 6 gives us the Noise Figure parameter. The noise figure (NF_{min}) in our design is 1.845dB. Figure 7, figure 8, figure 9 and figure 10 show the voltage gain, power gain, S_{11}, and IIP3 at 2GHz frequency. The voltage gain is 23.1066dB, power gain is 22.53dB, S_{11} is -9.781dB and IIP3 is -18.2287 obtained by simulation.

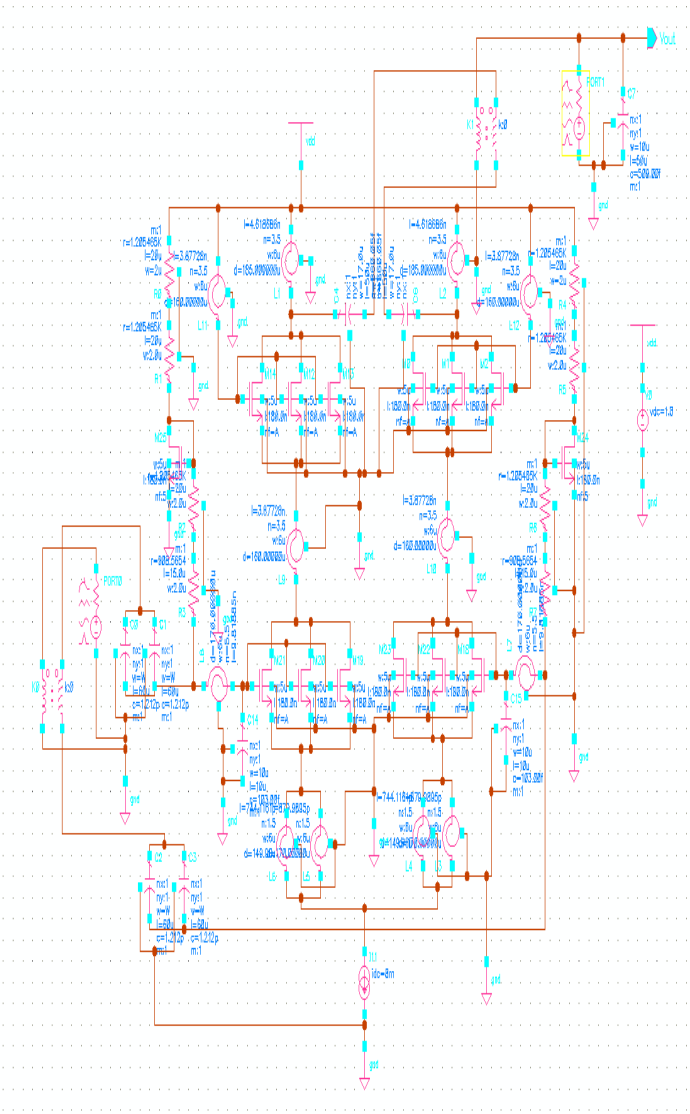

Fig. 5. Schematic of Differential LNA

Table I. SUMMARY OF DIFFERENTIAL LNA PERFORMANCE

Performance Parameters (Unit)	**Differential LNA**
Minimum Noise Figure(NF_{min}) (dB)	1.845
Noise Figure(NF) (dB)	2.846
Voltage Gain (dB)	23.1066
Power Gain(S_{21}) (dB)	22.53
S_{11} (dB)	-9.781
S_{12} (dB)	-40.68
S_{22} (dB)	-11.42
I_D (mA)	9
Power Consumption (mW)	16.2
1-dB Point (dBm)	-28.8865
IP3 Point (dBm)	-18.2287
Total input referred noise (V^2/HZ)	$4.91561e^{-19}$

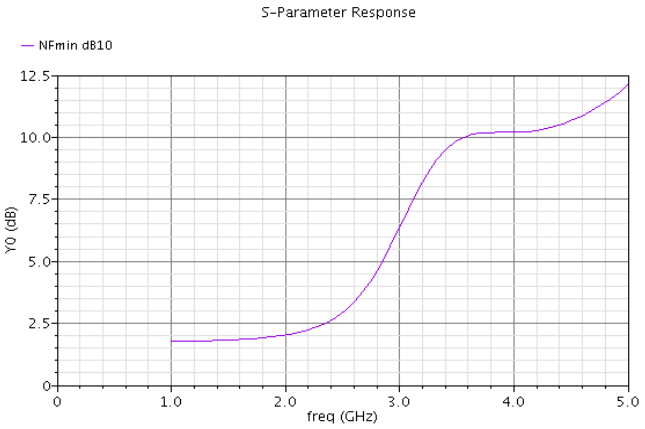

Fig. 6. Plot of Noise Figure (NF_{min})

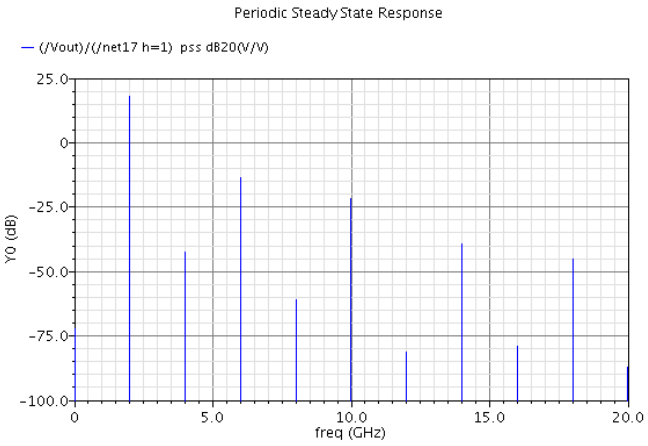

Fig. 7. Plot of Voltage Gain

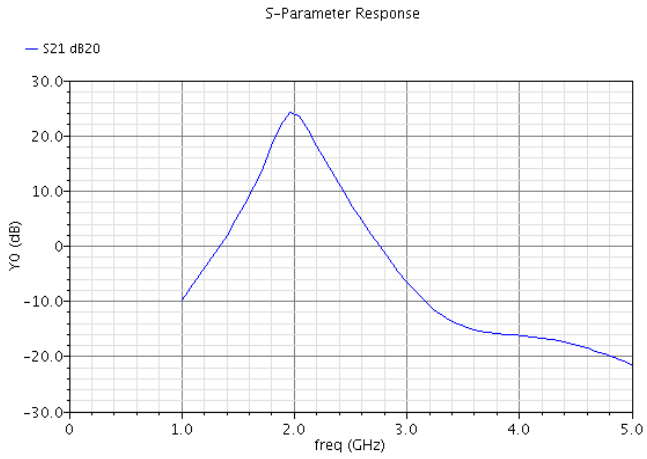

Fig. 8. Plot of Power Gain

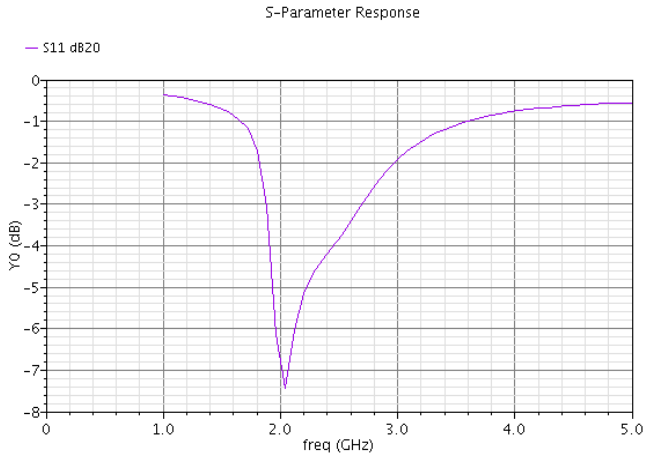

Fig. 9. Plot of S_{11}

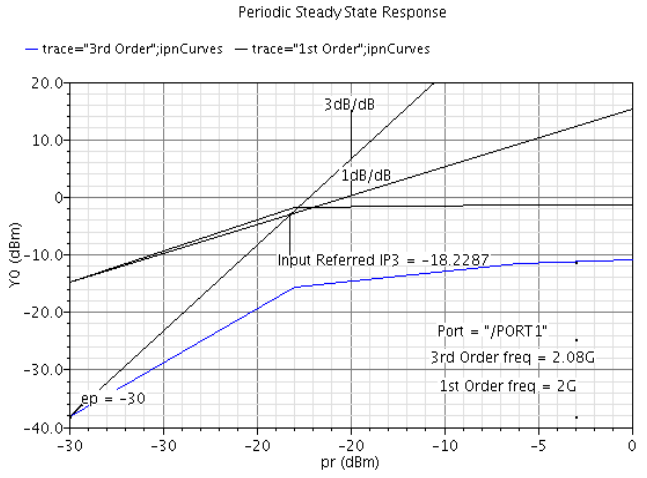

Fig. 10. Plot of IIP3

II. CONCLUSION

In this paper, a Differential low noise amplifier, we obtained a noise figure (NF_{min}) of about 1.845dB, voltage gain is 23.1066dB and power gain (S_{11}) is 22.53dB. In this design the gain can be depends on source inductance and Inter-stage Inductor between input stage and cascoded stage boost gain and lower noise figure. Using the power constrained method the power dissipation of the designed LNA is 16.2mW. The CMOS Differential LNA is designed, and it can be utilized in wireless RF receiver which is operated at 2 GHz.

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