A Simulation-based Study of Gate Misalignment Effects in Triple-Material Double-Gate (TM DG) MOSFETs

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Abstract— **In this work, a simulation based study of gate misalignment effects in triple- material double-gate (TMDG) MOSFETs is presented. An attempt is made to analyze the effects of gate misalignment on the front and back gates surface potential considering the misalignment for both the source and drain side. The surface potential profile for misaligned gate TMDG MOSFET is compared with its double and single material counterparts to predict the electrical parameters like threshold voltage roll-off. The surface potential profile is obtained through 2-D simulations by ATLAS^{TM} from Silvaco Inc.**

Keywords—TMDG, Gate Misalignment, Short Channel Effects, DIBL.

I. INTRODUCTION

Double-Gate (DG) MOSFET has established itself as one of the premiere structure to check the short-channel effects in the sub 100nm device. It has not only registered itself with an idealized subthreshold slope of 60 mV/decade but also with the higher drain current density and improved transconductance[1]. Further, researchers like Reddy *et al.* [2] and Tiwari *et al.*[3] proposed structures of double-material (DM) and triple-material (TM) DG MOSFETs respectively to improve the drain induced barrier lowering (DIBL) effect and minimize the hot carrier effect. Furthermore, comparative study reveals that TMDG MOSFET structure is superior to DM DG MOSFET structure in terms of both short-channel effects and hot-carrier effects.

Although DG MOSFET is expected to be a front runner in sub-50 nm regime of MOS technology yet an inherent difficulty lies in aligning the top gate over the bottom gate. The misalignment causes the gate to source/drain overlap capacitance and loss of current drive [4]. Further, the gate misalignment problem becomes more severe with DM-DG and TM-DG MOSFET structures because a possible process variation in the fabrication may mar the performance of the MOSFET in terms of increased threshold voltage, lower drain current and lower transconductance [5]. Shen *et al.* confirmed how bottom gate misalignment in conventional DG adversely affects the subthreshold swing and on-current, gives a smaller on-off current ratio [1]. Misalignment in the source side is more tolerable for on current but is far detrimental to the subthreshold swing as compared with drain misalignment. The misalignment has been studied widely and reported for the conventional and the double material DG MOSFET [6,7,8].

When misalignment creeps into the TMDG structure, the effects on the threshold voltage, drain current and transconductance needs to be investigated and the first order analysis comes with the surface potential profile. The present paper gives the potential response for various amounts of misalignment both at the source and the drain ends.

II. DEVICE STRUCTURE

The Figs. 1 and 2 show the cross-section of a TMDG with drain side misalignment respectively. The channel is fully depleted at channel doping of N_a cm^{-3} and the drain/ source doping is N_d cm^{-3}. The channel length is L and misalignment length is m_a in either source or drain side. The silicon film of thickness t_{Si} forms a sandwiched structure between the thin oxide (SiO_2) layers with a thickness of t_{ox}. M_1, M_2 and M_3 form the metal trio with decreasing order of the workfunction towards the drain. Here M_2 and M_3 form the screening gate whereas the M_1 is the control gate. The source terminal grounded and gate and drain potential is maintained at constant potential V_{ds} and V_{gs} respectively.

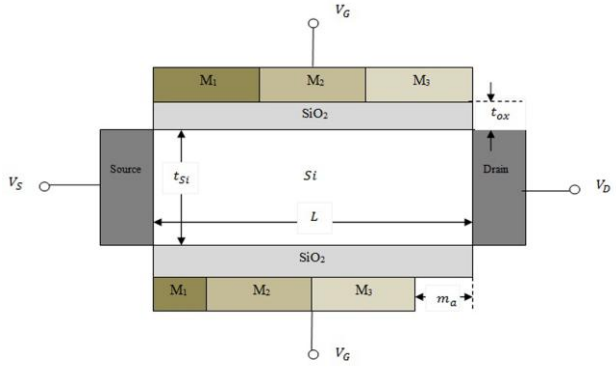

Fig. 1. Cross-section view of a TM DG MOSFET with drain side misalignment.

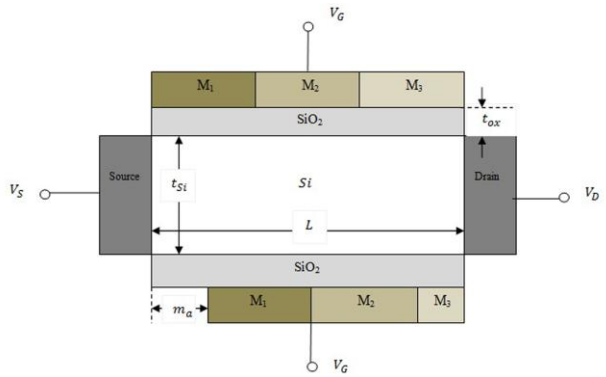

Fig. 2. Cross-section view of a TM DG MOSFET with source side misalignment.

III. SIMULATION RESULTS AND DISCUSSIONS

The simulations are carried using a 2-D numerical simulator named ATLAS™ from Silvaco Inc. SRH recombination model, field dependent mobility model and drift-diffusion model for carrier transportation are utilized in structure simulation. Newton's method is exploited to solve the partial differential equations.

TABLE II PARAMETERS FOR THE SIMULATIONS

Parameter	Value
Source /Drain doping (N_d)	10^{20} cm^{-3}
Channel doping (N_a)	$10^{18}cm^{-3}$
Oxide thickness (t_{ox})	2 nm
Channel Length (L)	90 nm
Misalignment Length (m_a)	0-45nm
Silicon film thickness (t_{si})	10 nm
Gate Metal work function (M_1)	4.8 eV
Gate Metal work function (M_2)	4.6 eV
Gate Metal work function (M_3)	4.4 eV
Drain to source voltage (V_{ds})	100mV
Gate to source voltage (V_{gs})	200mV

Fig. 3 represents the front surface potential with varying misalignment lengths at the drain side. As seen, the minimum surface potential increases with increased misalignment length, resulting in decreased barrier height and lesser threshold voltage. This phenomenon matches our physical understanding as when the back gate keeps on losing its influence over the channel the minority carriers are easily pulled by the front gate to form an early inversion of the front channel. However, it can be said that higher the gate misalignment at the drain end results in higher threshold voltage roll-off in the device.

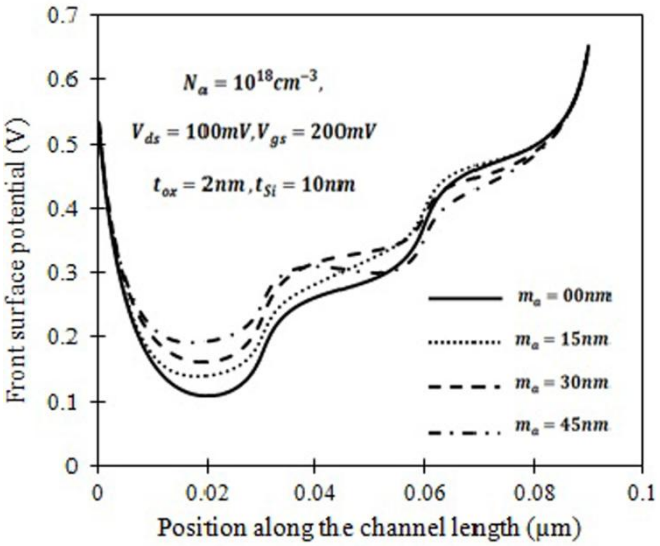

Fig. 3. Front channel surface potential with variation in the misalignment length at the drain side.

Fig. 4 represents the back surface potential with varying misalignment lengths at the drain side. The minimum of the surface potential increases with an increase in the misalignment and barrier height reduces. The minority carriers in the non overlapped channel region are attracted heavily by the back gate (overlapped channel) than the front gate due to its proximity and changes the barrier height more than that of the front gate as is confirmed by the graphs.

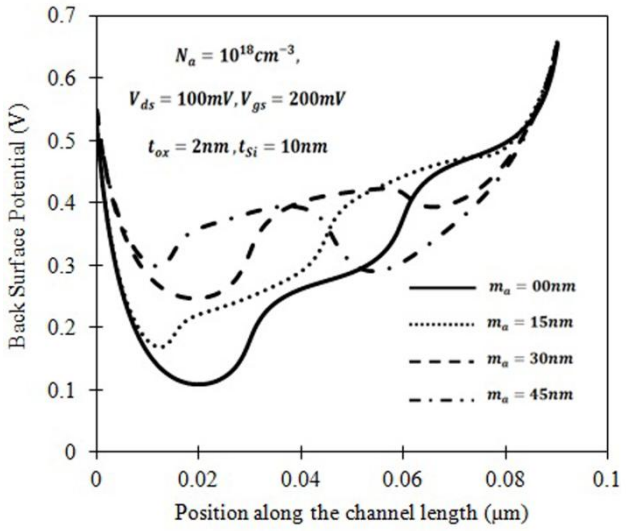

Fig. 4. Back channel surface potential with variation in the misalignment length at the drain side.

Comparison of Figs. 4 and 5 revels that even for symmetric TM DG MOSFET structure, front and back surface potentials become asymmetric due to the misalignment in the front and back gates and hence threshold voltage will be determined by

that surface which will have lower source-channel barrier height.

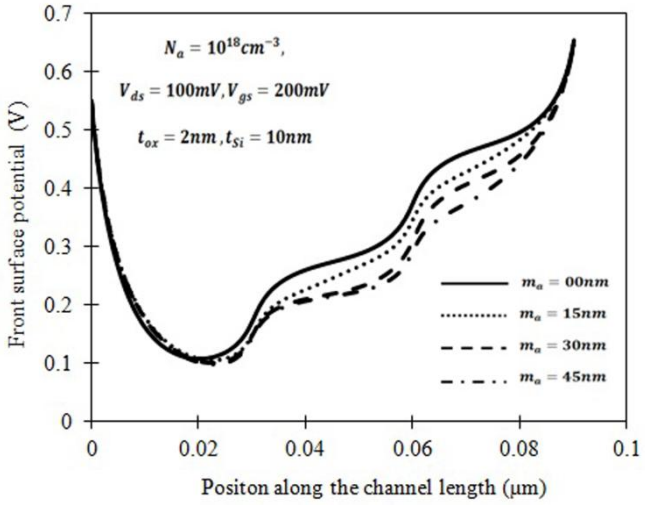

Fig. 5. Front channel surface potential with variation in the misalignment length at the source side.

Fig. 5 represents the front surface potential with varying misalignment lengths at the source side. The minimum surface potential makes little or no change on varying the misalignment.

Fig. 6 represents the back surface potential with varying misalignment lengths at the source side. As opposed to the drain side misalignment, the minimum surface potential decreases and barrier height increases. When gate shifts towards the drain side, the charges are drained out from the non-overlapped region increasing the barrier height to some extent. Also the control gate with high work function reduces charges in the bulk and hence the potential in the channel drops significantly as evident from the graph.

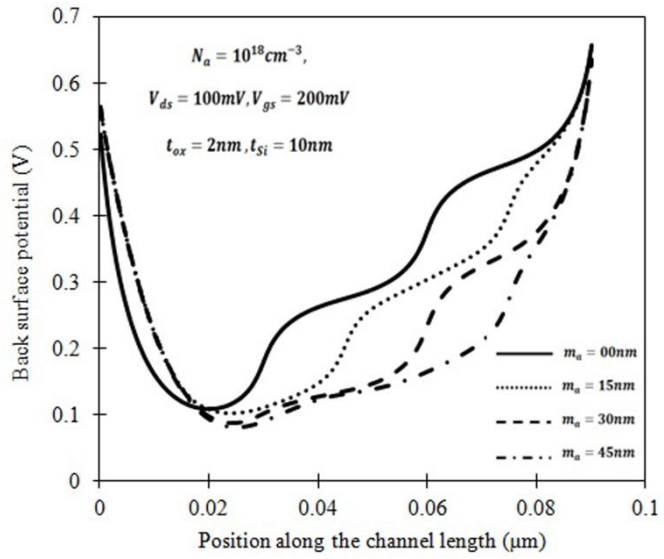

Fig. 6. Back channel surface potential with variation in the misalignment length at the source side.

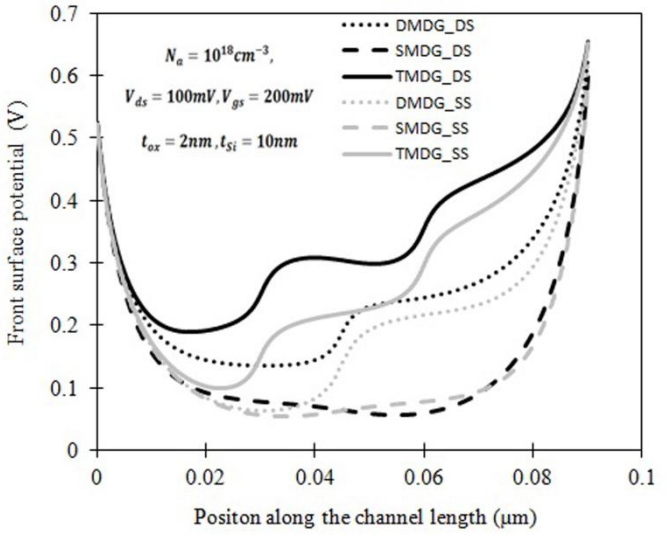

Fig. 7. Front Channel Surface Potential with 50% misalignment at the drain and source side for SMDG, DMDG and TMDG MOSFET .

Fig. 7 represents the front channel surface potential with 50% misalignment at the drain and source side for single (SMDG with workfunction 4.8eV), double (DMDG with workfunction of M_1=4.8eV and M_2=4.6 eV) and triple (TMDG with the metioned workfunctions) material double gate MOSFET. The minimum surface potential increases as the number of materials increases in the gate as seen from the graph. The higher workfunction in SMDG is responsible for a lower potential than the relatively lower workfunction in the case of DM and TMDG. It may be easily noted that DG MOSFET is less prone to the effects of gate misalignment compared to the DM DG and TM DG MOSFETs.

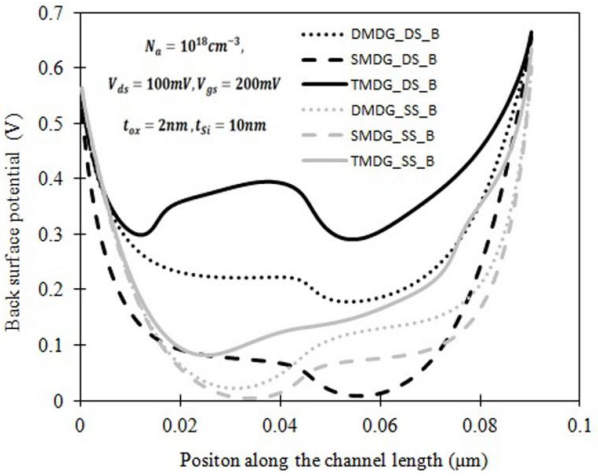

Fig. 8. Surface Potential in the back channel with variation in the misalignment length at the source side.

Fig. 8 represents the back channel surface potential with 50% misalignment at the drain and source side for single, double and triple material double gate MOSFET. The minimum surface potential increases as the number of

materials increases in the gate for the same reason as mentioned above. These variations are larger for the back gate than the front gate.

TABLE II COMPARISON OF BARRIER HEIGHT AT DIFFERENT MISALIGNMENTS

m_a (%)	Percentage variation in Barrier Potential at different misalignment lengths			
	TMDG DRAIN SIDE		TMDG SOURCE SIDE	
	FRONT CHANNEL	BACK CHANNEL	FRONT CHANNEL	BACK CHANNEL
16.67	-7.6%	-13.7%	0.7%	1.3%
33.33	-12.5%	-32.2%	1.6%	5.1%
50	-19.2%	-42.2%	2.1%	6.3%

The changes in source-channel barrier height for different values of m_a are presented in TABLE II. It is evident from the TABLE II. that drain side misalignment has a larger impact on the barrier height. For a drain side misalignment, the back channel is more prone to barrier height variation. For a 50% misalignment, the back channel barrier decreases by 42.2% while the front channel is affected by 19.2%. For a source side, a 50% misalignment gives only 2.1% for front gate and 6.3 % for back gate.

TABLE III COMPARISON OF MINIMUM SURFACE POTENTIAL FOR DIFFERENT DG STRUCTURES (50% MISALIGNMENT) WITH THE RESPECTIVE NON MISALIGNED DG MOSFET

Mis-alignment	Structure type	Front channel	Back channel
Drain Side	SMDG	26%	89%
	DMDG	-59%	-101%
	TMDG	-75%	-168%
Source Side	SMDG	28.2%	94%
	DMDG	24%	74.5%
	TMDG	7.8%	24%

The TABLE III. gives comparison of the minimum surface potential for different DG MOSFET structures with the non misaligned. It is seen that the effects of the drain side misalignment is too high than that for the source side. For a drain side misalignment, the TM DG MOSFET gives a 168% and 75% reduction respectively in the back and front channel minimum surface potential. So, TMDG gives worse performance than its other two counterparts with respect to drain misalignment. For a source side misalignment, the TMDG shows the least affection with 7.8% and 24% respectively for the front and back channel minimum surface potential. Thus, TMDG gives the best results for sensitivity against the source side misalignment.

IV CONCLUSION

In this paper, an extensive study has been made for the effect of gate misalignment for a 90-nm-gate-length TMDG MOSFET. It is analyzed for different amount of misalignment (0%, 16.67%, 33.33% and 50%) at both the source end and the drain end. It is concluded that the source-channel barrier potential is more prone to the drain side misalignment than the source side. It is also observed that the drain side misalignment is more severe for the TMDG MOSFE than DM DG MOSFET and DG MOSFET while for source side misalignment, TMDG gives better performance than the other DG structures.

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REFERENCES

[1] J. Shen, T. Man, and M. Chan, "2D Analysis of Bottom Gate Misalignment and Process Tolerant for Sub- 100nm Symmetric Double-Gate MOSFETs", *IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 201-204, 2003.

[2] G. Reddy, M.J. Kumar," A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-two-dimensional analytical modeling and simulation", *IEEE Transactions on Nanotechnology*, vol. 4, no.2, pp-260 – 268, 2005.

[3] Tiwari *et al*, "A two dimensional analytical model threshold voltage of short channel triple material double gate metal-oxide-semiconductor field-effect-transistors", *Journal of Appl. Physics*, vol. 108, no. 7, pp. 074508, 2010.

[4] A. Kranti, G. Armstrong, "High Tolerance to Gate Misalignment in Low Voltage Gate-Underlap Double Gate MOSFETs", IEEE *Electron Device Letters*, vol. 29, issue:5, pp. 503-505, 2008.

[5] R. K. Sharma, M Gupta and R. S. Gupta, "Optimization of the Gate Misalignment Effects in Graded Channel DG FD SOl n-MOSFET with high-K gate dielectrics," *International Conference on Recent Advances in Microwave Theory and Applications*, pp. 50-52, 2008.

[6] J.B. Kuo and E.C. Sun, "A compact threshold voltage model for Gate Misalignment Effect of DG FD SOI nMOS devices considering fringing electric field effects" *IEEE Trans. on Electron Devices"*, vol. 51, no. 4, pp. 587-596, 2004.

[7] R. Valin, C. Sampedro, M. Aldegunde, A. Garcia-Loureiro, N. Seoane, A.Godoy and F. Gamiz, "Two-Dimensional Monte Carlo Simulation of DGSOI MOSFET Misalignment", *IEEE Trans. on Electron Devices",* vol. 59, no. 6, pp. 1621-1628, 2012.

[8] R.K. Sharma, R. Gupta, M. Gupta and R. S. Gupta, "Dual-Material Double-Gate SOI n-MOSFET: Gate Misalignment Analysis"*IEEE Trans. on Electron Devices",* vol. 56, no. 6, pp. 1284-1291, 2009.