An Analytical Study of Short-Channel Effects of Strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs Including Interface Charges

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***Abstract*—In this paper, an analytical threshold voltage model is developed for short-channel Strained-Si (s-Si) on Silicon-Germanium-on-insulator (SGOI) MOSFET including the effects of interface charges. The two-dimensional Poisson's equation is solved in the undamaged and damaged strained-Si and relaxed $Si_{1-x}Ge_x$ regions to find out the surface potential minimum for calculating the threshold voltage. The results obtained from the developed model have been compared with the numerical simulation results obtained using ATLAS™ from Silvaco. The extent of influence of hot carriers induced effects in terms of interface charges and damaged s-Si/front gate oxide interface on threshold voltage roll-off and drain induced barrier lowering (DIBL) have been studied.**

Keywords-strained-Si; SGOI; short-channel effects; inteface charges

I. INTRODUCTION

The use of strained silicon channel has become an unavoidable feature for sub 100nm regime CMOS technology, to maintain the expected performance improvements through scaling [1]. Among various proposed strained channel MOS structures, strained-Si on silicon-germanium-on-insulator (SGOI) MOSFET has received considerable attention because of providing more flexibility to control the strain in channel [2]. At such nanometer scaled devices, hot-carrier induced interface charges grievously affect the device performance, [3]. Besides this, downscaling of device also makes the short-channel effects (SCEs) severe [4]. It has been reported that the performance of the nanometer strained-Si devices is significantly dependent on the interface state charges near the Si/SiO_2 interface [5]. Thus, it becomes obligatory to investigate the depth up to which the interface charges can affect the short-channel device performance. A number of researchers have reported the study including interface charges for strained-Si SOI MOSFETs [3, 6]. Recently, a threshold voltage model is presented for strained-Si on SGOI MOSFETs [7]; however the effects of localized charges on short-channel effects are not investigated.

In this paper, a threshold voltage model is presented for strained-Si on SGOI MOSFETs including the effects of interface charges. Effects of the interface charges on the drain induced barrier lowering (DIBL) and threshold voltage roll-off are discussed. A uniform distribution of localized charges has been taken into consideration. In Section II, the device structure is briefed in terms of various device parameters. Section III deals with the modeling approach carried out while deriving the surface potential and threshold voltage of the device. All the theoretical results have been compared with the 2D simulation results, obtained by ATLAS™ 2D device simulator [8], and discussed in Section IV. The paper has been concluded in Section V.

II. DEVICE STRUCTURE

Fig. 1 shows the schematic cross sectional view of the strained-Si on SGOI MOSFET structure with induced localized charges. A layer of Si is grown pseudomorphically on the relaxed $Si_{1-x}Ge_x$ layer, where x is the Ge mole fraction, which causes the strain in the Si layer due to lattice mismatching with $Si_{1-x}Ge_x$.

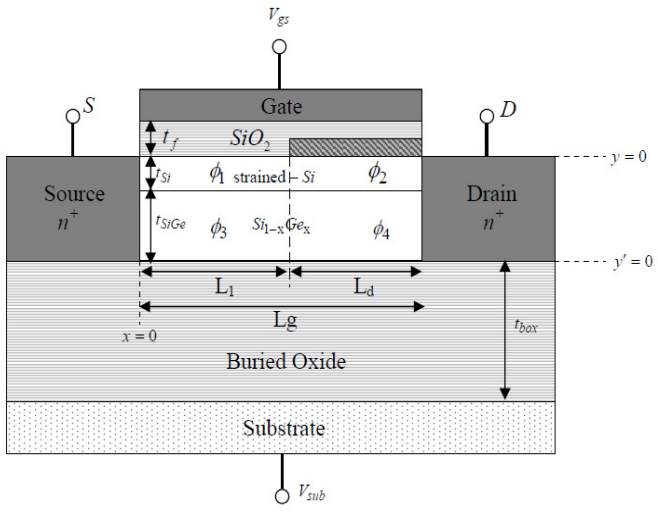

Figure 1. Cross sectional view of Strained-Si on SGOI MOSFET

L_d and L_1 are damaged and undamaged region lengths, respectively, along the channel connected in a non-overlapping way. The interface charge density in the damaged oxide region is assumed to be $N_I\,\mathrm{cm}^{-2}$. The

symbols t_{Si} , t_f , t_{box} and t_{SiGe} represent the thicknesses of the strained-Si, front gate oxide, buried oxide and $Si_{1-x}Ge_x$ layers, respectively.

III. MODELING APPROACH

Fig. 2 displays the change in silicon energy band structure because of strain in the silicon channel. The device simulator model library of ATLAS™, thus, has been modified according to the effects of strain on Si band structure [9].

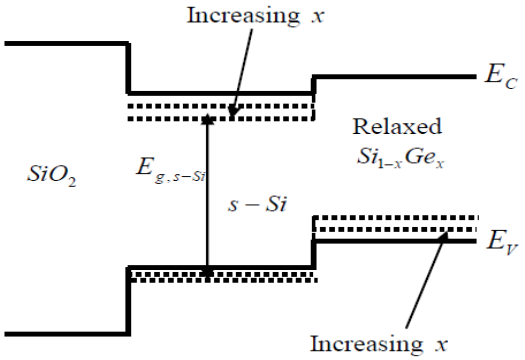

Figure 2. Effect of strain on band structure of Silicon

A. Surface Potential Formulation

First, To find out the potential distribution ($\phi(x,y)$) in the channel region, the 2D Poisson's equations has been solved in all the four regions of strained-Si and relaxed $Si_{1-x}Ge_x$ layers as shown in Fig. 1. The equations are

$$\frac{\partial^2\phi_{i,j}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{i,j}(x,y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si,SiGe}} \quad (1)$$

For $Si_{1-x}Ge_x$ layer, y -coordinate should be considered as y' . Subscripts denote the channel region as i stands for 1 and 2 whereas j stands for 3 and 4; N_A is the body doping concentration; q is the electronic charge; ε_{Si} and ε_{SiGe} are the permittivity of strained-Si film and relaxed $Si_{1-x}Ge_x$. The potential distributions in all the four regions are approximated by parabolic approximation [10] as

$$\phi_i(x,y)=\phi_{si}(x)+C_{i1}(x)y+C_{i2}(x)y^2 \quad (2)$$

$$\phi_j(x,y')=\phi_{bj}(x)+C_{j1}(x)y'+C_{j2}(x)y'^2 \quad (3)$$

Here, the coefficients $C_{i(j)1,2(3,4)}$ are the functions of x only; ϕ_{si} is the surface potential at SiO_2/s-Si interface for both damaged and undamaged regions, ϕ_{bj} is potential along buried-SiO_2/$Si_{1-x}Ge_x$ interface for both damaged and undamaged regions. The continuity of potential and electric field across the interface of undamaged and damaged regions are [6]:

$$\phi_1(L_1,0)=\phi_2(L_1,0) \quad (4)$$

$$\left[\frac{\partial\phi_1(x,y)}{\partial x}\right]_{x=L_1}=\left[\frac{\partial\phi_2(x,y)}{\partial x}\right]_{x=L_1} \quad (5)$$

$$\phi_3(L_1,0)=\phi_4(L_1,0) \quad (6)$$

$$\left[\frac{\partial\phi_3(x,y')}{\partial x}\right]_{x=L_1}=\left[\frac{\partial\phi_4(x,y')}{\partial x}\right]_{x=L_1} \quad (7)$$

Electric flux at SiO_2/s-Si interface should be continuous in the undamaged and damaged regions [7]:

$$\left[\frac{\partial\phi_1(x,y)}{\partial y}\right]_{y=0}=\frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s1}(x)-V'_{gs}}{t_f} \quad (8)$$

$$\left[\frac{\partial\phi_2(x,y)}{\partial y}\right]_{y=0}=\frac{\varepsilon_f}{\varepsilon_{Si}}\frac{\phi_{s2}(x)-V''_{gs}}{t_f} \quad (9)$$

where, ε_f is the permittivity of the SiO_2, t_f is the thickness of front gate oxide; $V'_{gs}=V_{gs}-(V_{FB,f})_{s-Si}$ with V_{gs} as the gate to source voltage, $(V_{FB,f})_{s-Si}$ is the front channel flat-band voltage of strained-Si film and $V''_{gs}=V_{gs}-(V_{FB,f})_{s-Si}+qN_I/C_f$.

Electric flux at $Si_{1-x}Ge_x$/buried oxide interface is continuous, we may write [7];

$$\left[\frac{\partial\phi_3(x,y')}{\partial y'}\right]_{y'=0}=\frac{\varepsilon_{box}}{\varepsilon_{SiGe}}\frac{\phi_{b3}(x)-V'_{sub}}{t_{box}} \quad (10)$$

$$\left[\frac{\partial\phi_4(x,y')}{\partial y'}\right]_{y'=0}=\frac{\varepsilon_{box}}{\varepsilon_{SiGe}}\frac{\phi_{b4}(x)-V'_{sub}}{t_{box}} \quad (11)$$

where $V'_{sub}=V_{sub}-(\Phi_{sub}-\Phi_{SiGe})$, V_{sub} being the substrate voltage and t_{box} is the buried oxide thickness; Φ_{SiGe} is the work-function of relaxed $Si_{1-x}Ge_x$ layer; Φ_{sub} is the work-function of the silicon substrate under buried oxide.

The potential and electric field at the Si/$Si_{1-x}Ge_x$ interface should be continuous as [6];

$$\phi_1(x,t_{Si})=\phi_3(x,t_{SiGe}) \quad (12)$$

$$\left[\frac{\partial\phi_1(x,y)}{\partial y}\right]_{y=t_{Si}}=-\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial\phi_3(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \quad (13)$$

$$\phi_2(x,t_{Si})=\phi_4(x,t_{SiGe}) \quad (14)$$

$$\left[\frac{\partial\phi_2(x,y)}{\partial y}\right]_{y=t_{Si}}=-\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial\phi_4(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \quad (15)$$

The potentials at the source and drain end can be given by [7];

$$\phi_1(0,0)=V_{bi,s-Si} \quad (16)$$

$$\phi_3(0,0)=V_{bi,SiGe} \quad (17)$$

$$\phi_2(L,0)=V_{bi,s-Si}+V_{ds} \quad (18)$$

$$\phi_4(L,0)=V_{bi,SiGe}+V_{ds} \quad (19)$$

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where, $V_{bi,s-Si}$ is the built-in voltage for strained-Si and $V_{bi,SiGe}$ is the built-in voltage for $Si_{1-x}Ge_x$; V_{ds} is drain-to-source voltage.

With the help of the boundary conditions described by (5)-(19), the final expression of surface potential can be written as [10];

$$\phi_{s1} = A_1 \exp(\lambda x) + B_1 \exp(-\lambda x) - \sigma_1 \quad (20)$$

$$\phi_{s2} = A_2 \exp(\lambda(x - L_1)) + B_2 \exp(-\lambda(x - L_1)) - \sigma_2 \quad (21)$$

where,

$$B_1 = \frac{(V_{bi,s-Si} - \sigma_1)(\exp(\lambda L) - 1) - (\sigma_2 - \sigma_1)(1 - \cosh(\lambda L_d)) - V_{ds}}{2\sinh(\lambda L)}$$

$$A_1 = V_{bi,s-Si} + \sigma_1 - B_1$$

$$A_2 = A_1 \exp(\lambda L_1) + (\sigma_2 - \sigma_1)/2$$

$$B_2 = B_1 \exp(-\lambda L_1) + (\sigma_2 - \sigma_1)/2$$

λ, σ_1 and σ_2 are the constants obtained from the boundary conditions mentioned above.

The position $(x_{1(2),\min})$ of the minimum surface potential for both negative and positive interface charges under the undamaged and damaged regions respectively can be determined by solving $\left.\frac{d\phi_{s1(2)}}{dx}\right|_{x=x_{1(2),\min}} = 0$ [6] and hence be given as;

$$x_{1,\min} = \ln(B_1/A_1)/2\lambda \text{ and}$$

$$x_{2,\min} = L_1 + \ln(B_2/A_2)/2\lambda$$

By substituting the values of the minima position into (20) and (21), the minimum surface potentials can be expressed

$$\phi_{s1,\min} = 2\sqrt{A_1 B_1} - \sigma_1 \quad (22)$$

$$\phi_{s2,\min} = 2\sqrt{A_2 B_2}\cosh(\lambda L_1) - \sigma_2 \quad (23)$$

B. Threshold Voltage Formulation

The Because of the coexistence of the damaged and the undamaged regions in our device structure, the minimum surface potential of device is determined by the magnitude and polarity of the charge present in the damaged region. Thus, depending on the polarity of interface charges, threshold voltage, say $V_{th+(-)}$, for positive (negative) type of interface charges can be found as follows as [7]:

$$\left.\phi_{s1(2),\min}\right|_{Vgs=V_{th}+(-)} = 2\Phi_{F,Si} + \Delta\Phi_{s-Si} = \Phi_{th} \quad (24)$$

where, $\Phi_{F,Si}$ is the difference between the Fermi potential and the intrinsic Fermi level in the bulk region, $\Delta\Phi_{s-Si}$ is the change in the work-function of silicon due to strain, Φ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping.

Solving (24), we obtain the final expression of threshold voltages as

$$V_{th+(-)} = \frac{-\eta_{1(2)} + \sqrt{\eta_{1(2)}^2 - 4\rho\xi}_{1(2)}}{2\rho} \quad (25)$$

where,

$$\rho = N^2\left[2(\cosh(\lambda L) - 1) - \sinh^2(\lambda L)\right]$$

$$\eta_1 = N\left[2(\Phi_{th} + M_1)\sinh^2(\lambda L) - R_1(\exp(\lambda L) - 1) - S_1(1 - \exp(\lambda L))\right]$$

$$\xi_1 = R_1 S_1 - (\Phi_{th} + M_1)^2 \sinh^2(\lambda L)$$

$$R_1 = (V_{bi,s-Si} + M_1)(1 - \exp(-\lambda L)) + V_{ds} + (\sigma_2 - \sigma_1)(1 - \cosh(\lambda L_d))$$

$$S_1 = (V_{bi,s-Si} + M_1)(\exp(-\lambda L) - 1) - V_{ds} - (\sigma_2 - \sigma_1)(1 - \cosh(\lambda L_d))$$

$$u_2 = \frac{qN_A}{\varepsilon_{Si}} + \frac{C_{box}V'_{sub}}{(C_{Si} + C_{SiGe})t_{Si}^2} + \frac{C_f(2C_{SiGe} + C_{Si})\left((V_{FB,f})_{s-Si} + (qN_I/C_f)\right)}{C_{Si}(C_{Si} + C_{SiGe})t_{Si}^2}$$

$$\nu_1 = \frac{C_f(2C_{SiGe} + C_{Si})}{C_{Si}(C_{Si} + C_{SiGe})t_{Si}^2}$$

$$u_1 = \frac{qN_A}{\varepsilon_{Si}} + \frac{C_{box}V'_{sub}}{(C_{Si} + C_{SiGe})t_{Si}^2} + \frac{C_f(2C_{SiGe} + C_{Si})(V_{FB,f})_{s-Si}}{C_{Si}(C_{Si} + C_{SiGe})t_{Si}^2}$$

$$u_3 = \frac{qN_A}{\varepsilon_{SiGe}} + \frac{C_{box}(C_{SiGe} + 2C_{s-Si})V'_{sub}}{C_{SiGe}(C_{Si} + C_{SiGe})t_{SiGe}^2} + \frac{C_f(V_{FB,f})_{s-Si}}{(C_{Si} + C_{SiGe})t_{SiGe}^2}$$

$$u_4 = \frac{qN_A}{\varepsilon_{SiGe}} + \frac{C_{box}(C_{SiGe} + 2C_{Si})V'_{sub}}{C_{SiGe}(C_{Si} + C_{SiGe})t_{SiGe}^2} + \frac{C_f\left((V_{FB,f})_{s-Si} + (qN_I/C_f)\right)}{(C_{Si} + C_{SiGe})t_{SiGe}^2}$$

$$\nu_2 = \frac{C_{ox}}{(C_{SiGe} + C_{Si})t_{SiGe}^2}$$

$$\sigma = \frac{\beta_1(u_4 - u_3) - \alpha_2(u_2 - u_1)}{\alpha_1\alpha_2 - \beta_1\beta_2}$$

$$\eta_2 = N\left[\begin{array}{l} 2(\Phi_{th} + M_2)\sinh^2(\lambda L) - R_2(\exp(\lambda L_d) - \exp(-\lambda L_1)) \\ \qquad - S_2(\exp(\lambda L_1) - \exp(-\lambda L_d)) \end{array}\right]$$

$$\xi_2 = R_2 S_2 - (\Phi_{th} + M_2)^2 \sinh^2(\lambda L)$$

$$R_2 = \left[\begin{array}{l} (V_{bi,s-Si} + M_1)(\exp(\lambda L_1) - \exp(-\lambda L_d)) + V_{DS}\exp(\lambda L_1) \\ \qquad + (\sigma_2 - \sigma_1)(\exp(\lambda L_1) - \cosh(\lambda L_1)\exp(-\lambda L_d)) \end{array}\right]$$

$$S_2 = \left[\begin{array}{l} (V_{bi,s-Si} + M_1)(\exp(\lambda L_d) - \exp(-\lambda L_1)) - V_{DS}\exp(-\lambda L_1) \\ \qquad - (\sigma_2 - \sigma_1)(\exp(-\lambda L_1) - \cosh(\lambda L_1)\exp(\lambda L_d)) \end{array}\right]$$

$C_f = \frac{\varepsilon_f}{t_f}$, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$, $C_{SiGe} = \frac{\varepsilon_{SiGe}}{t_{SiGe}}$ and $C_{box} = \frac{\varepsilon_{box}}{t_{box}}$ are front gate oxide, strained-Si, relaxed $Si_{1-x}Ge_x$ layer and buried oxide capacitances respectively and M, M_1 and N are constants. It may be pointed out that the threshold voltage of strained-Si SGOI MOSFETs significantly depends on the polarity of the interface charge density.

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IV. RESULTS AND DISCUSSION

This section contains the comparison between the analytical results obtained from our proposed model with the numerical simulation data extracted from simulating the device structure under consideration with a commercially available 2D device simulator ATLAS™ [8]. The threshold voltage is extracted from the ATLAS simulation by maximum transconductance method. Fig. 3 shows the variation of threshold voltage roll-off with positive and negative interface charge densities for different damaged region length, L_d. It is found that threshold voltage roll-off increases for both positive and negative interface charge densities but rate of increment is higher for negative charge density. However, the nature of variation is different in both of the cases. In the case of positive interface charge density, there is an increase in threshold voltage roll-off with L_d whereas for negative interface charges, roll-off decreases with L_d. Fig. 4 discusses the impact of drain voltage on device characteristics in terms of drain induced barrier lowering (DIBL) variation with respect to interface charge density. It can be observed that that DIBL increases very sharply with increasing negative interface charge density but very slightly decreases with positive interface charge density.

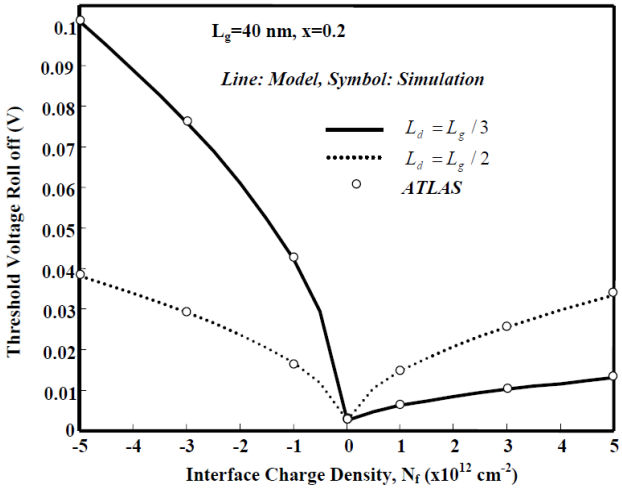

Figure 3. Threshold voltage roll-off versus interface charge density of strained-Si on SGOI MOSFET for different damaged length

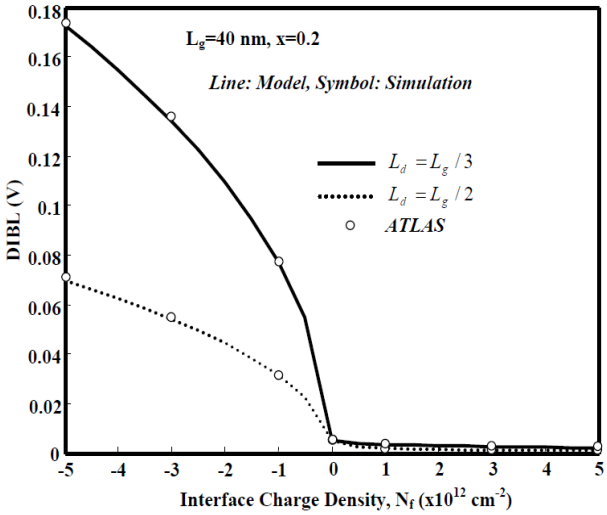

Figure 4. DIBL versus interface charge density of strained-Si on SGOI MOSFET for different damaged length with $V_{ds} = 0.1$V and 1V

DIBL is large for smaller damaged length for negative interface charge density. Finally, Fig. 5 compositely illustrates the effect of damaged region length on threshold voltage roll-off and DIBL for different Ge mole fraction (x). It is observed that larger x, which also corresponds to the higher strain in the channel region, suppresses the threshold voltage roll-off and drain induced barrier lowering effectively. However, with respect to the length of damaged region, the trend of variation becomes reverse i.e., the threshold voltage roll-off decreases whereas DLBL increases with the increases in L_d.

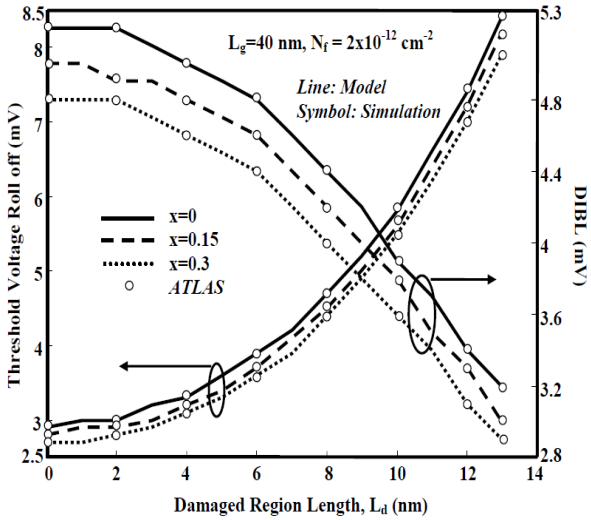

Figure 5. DIBL and Threshold Voltage Roll-off versus damaged region length of strained-Si on SGOI MOSFET for different Ge mole fraction (x) in SiGe layer on a fixed positive interface charge density

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V. CONCLUSION

An analytical threshold voltage model is derived including the effect both positive and negative interface charges. It is observed that the negative interface charge density has more severe effect than the positive interface charge density on the DIBL and threshold voltage roll-off of the strained-Si on SGOI MOSFETs. However, it is found that strain in the silicon channel suppresses short-channel effects. The proposed model results are in good agreement with the numerical simulation results.

REFERENCES

[1] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide semiconductor field-effect transistors," J. Appl. Phys., vol. 97, 011101 (2005), pp. 1-27.

[2] F. Gamiz, P. C. Cassinello, J. B. Roldan, and F. J. Molinos, "Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates," J. Appl. Phys., vol. 92, no. 1, Jul. 2002, pp. 288–295.

[3] Y. Leblebici and S-M Kang, "Modeling of nMOS Transistors for Simulation of Hot-Carrier-Induced Device and Circuit Degradation," IEEE Trans. Computer-Aided Design, vol. 11 , no. 2, February 1992, pp. 235-246.

[4] A. Chaudhry and M. Jagadesh Kumar, Controlling Short-Channel Effects in Deep-Submicron SOI MOSFETs for Improved Reliability: A Review, IEEE Transactions on Device and Materials Reliability, vol. 4, 2004, pp. 99-109.

[5] P. S. Jack, J.-Y. Kuo, "On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs," IEEE Electron Dev. Lett, vol. 28, no. 7, 2007, pp. 649-52.

[6] Eleftherios G. Ioannidis, Andreas Tsormpatzoglou, Dimitrios H. Tassis, Effect of Localized Interface Charge on the Threshold Voltage of Short-Channel Undoped Symmetrical Double-Gate MOSFETs, IEEE Trans. Electron Devices, vol. 58, no. 2, Feb 2011, pp. 433-440.

[7] V. Venkataraman, S. Nawal, and M. J. Kumar, "Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Silicon–Germanium-on-Insulator (SGOI) MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 3, March 2007, pp. 554-562.

[8] ATLAS Users Manual, Silvaco International, Santa Clara, CA, 2000.

[9] Numata, T., Mizuno, T., Tezuka, T., Koga, J., Takagi, S.: Control of threshold-voltage and short-channel effects in ultrathin strained-SOI CMOS devices. IEEE Trans. Electron Devices, Vol. 52, 2005, pp. 1780–1786.

[10] K. K. Young, Short-channel effect in fully depleted SOI MOSFETs IEEE Trans. Electron Devices, Vol. 36, 1989, pp. 399–402.

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