An Ultra Low Power Encoder for 5 Bit Flash ADC

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***ABSTRACT*- This investigation suggests a low power encoding scheme proposed for 4GS/s 5 bit flash analog to digital converter. One of the demanding issues in the design of a low power flash ADC is the design of thermometer code to binary code. An encoder in this paper converts the thermometer code into binary code without any intermediate stage. To decrease the power consumption of the encoder, the implementation is done using dynamic CMOS logic. The proposed encoder is designed using 90 nm technology at 1.2 V power supply using CADENCE tool. The simulation results shown for a sampling frequency of 4GHz and the average power dissipation of the encoder is 1.833 µW.**

Keywords – Analog to digital converter, Flash ADC, Dynamic CMOS logic.

I. INTRODUCTION

Flash ADC is the fastest ADC in comparison with other ADC architectures. The flash ADC is the best choice in high speed low resolution applications. So it is highly used in high data rate links, high speed instrumentation, wideband radar, digital oscilloscopes and optical communications. Since flash ADC is operating in parallel conversion method, maximum operating frequency in the range of gigahertz is possible [1].

Figure 1 illustrates a typical flash ADC block diagram. The flash ADC architecture requires 2^N -1 comparators to achieve an N bit resolution. In this structure an array of comparators compares the input voltage with a set of increasing reference voltages. One of the inputs of all the comparator is connected to an analog input and output is produced in a single cycle. The comparator output represents the input signal in a thermometer code . An encoder is designed which will convert the thermometer code into a binary weighted output code. The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and an encoder structure. Exponentially increasing number of comparators makes it difficult to obtain a high resolution while maintaining at the same time a large bandwidth, a low power consumption and a small die size [2].

The power of the encoder is one of the bottlenecks of any flash ADC. Generally ADCs are should be integrated with digital circuits on a single chip for the portable devices. For prolonged battery life, all battery powered devices are designed to include low power techniques. The designing of an ADC which operates at low voltages offers a great difficulty because of the relatively high threshold voltage of the transistors. Moreover for achieving low power, ADCs require low power architecture. The proposed encoder is designed using a logic style called dynamic logic for achieving the ultra low power consumption. Background study is presented in section II. The design and implementation of the proposed encoder are described in section III and IV respectively. Simulation results, discussion and conclusion are provided in the succeeding sections.

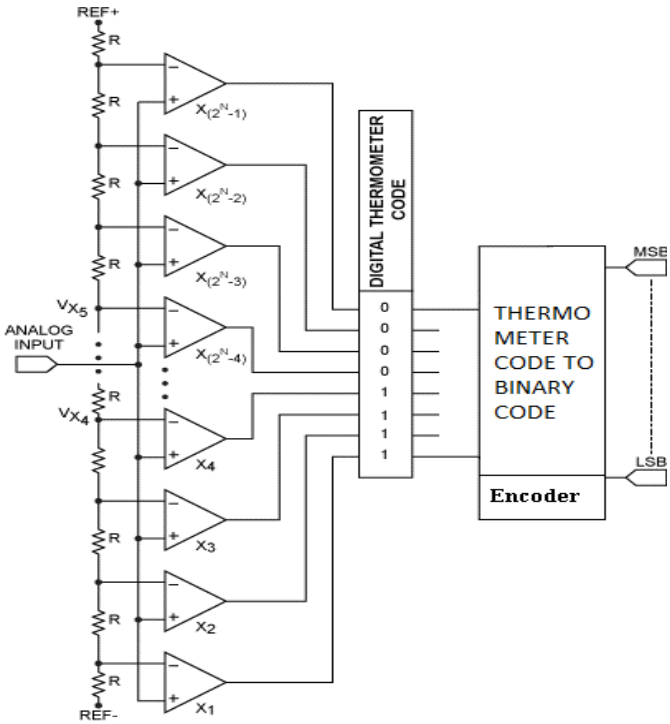


Fig. 1. Flash ADC Block Diagram

II. BACKGROUND

Reference [3] uses a logic style called pseudo dynamic logic for achieving the highest speed [5 GHz] for 4 bit encoder with a power dissipation of 184.8 µW. As the resolution of the ADC increases, the maximum frequency of operation decreases. The pseudo dynamic CMOS circuit consists of a PMOS transistor , a bunch of NMOS transistors and an inverter. The PMOS transistor is used for pre-charge operation. During the precharging operation, the output node is charged to a logic high value through the PMOS transistor. The output node is evaluated depending upon the logic implemented in the pull down network. The power dissipation in a circuit is mainly divided into static power dissipation and dynamic power dissipation. The power dissipation occurring at the time of switching is called dynamic power dissipation. This will be the major part of the total power dissipation. Static power dissipation occurs when both pull up and pull down

transistors are on. The current which flows from rail to rail (VDD to GND) dissipates a power in the circuit that leads to static power dissipation.

One of the disadvantages of the pseudo dynamic CMOS implementation is the presence of static power dissipation. When a clock signal is low and the NMOS transistors in the pull down network are on, then a current will flow from VDD to GND which contributes a specific amount of power (static power dissipation) to the total power dissipation.

To achieve ultra low power dissipation, the implementation of the encoder is done using a dynamic CMOS logic style which is not having static power dissipation. The truth table which gives the relation between thermometer code and the corresponding to 5 bit binary code is presented in table1.

B4	B3	B2	B1	B0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	00000000000000000000000000000011
0	0	0	1	1	00000000000000000000000000000111
0	0	1	0	0	00000000000000000000000000001111
0	0	1	0	1	00000000000000000000000000011111
0	0	1	1	0	00000000000000000000000000111111
0	0	1	1	1	00000000000000000000000001111111
0	1	0	0	0	00000000000000000000000011111111
0	1	0	0	1	00000000000000000000000111111111
0	1	0	1	0	00000000000000000000001111111111
0	1	0	1	1	00000000000000000000011111111111
0	1	1	0	0	00000000000000000000111111111111
0	1	1	0	1	00000000000000000001111111111111
0	1	1	1	0	00000000000000000011111111111111
0	1	1	1	1	00000000000000000111111111111111
1	0	0	0	0	00000000000000001111111111111111
1	0	0	0	1	00000000000000011111111111111111
1	0	0	1	0	00000000000000111111111111111111
1	0	0	1	1	00000000000001111111111111111111
1	0	1	0	0	00000000000011111111111111111111
1	0	1	0	1	00000000000111111111111111111111
1	0	1	1	0	00000000001111111111111111111111
1	0	1	1	1	00000000011111111111111111111111
1	1	0	0	0	00000001111111111111111111111111
1	1	0	0	1	00000011111111111111111111111111
1	1	0	1	0	00000111111111111111111111111111
1	1	0	1	1	00001111111111111111111111111111
1	1	1	0	0	00011111111111111111111111111111
1	1	1	0	1	00111111111111111111111111111111
1	1	1	1	0	01111111111111111111111111111111
1	1	1	1	1	11111111111111111111111111111111

Table1. Binary Code Encoder Truth Table

The design equations of the proposed encoder are derived from the truth table given in table 1.

III. DESIGN OF THE PROPOSED ENCODER

Designing of converting thermometer code into binary code is one of the main design issues of any flash ADC encoder [4]. The main feature of this encoder is that the thermometer code is converted to binary output code without any intermediate stage. This will help in reducing the number of transistors used in the design. The following equations gives the relation between the thermometer coded data and the binary coded data for a 5 bit encoder.

$$B_4 = I_{15}$$

$$B_3 = I_7.\overline{I_{15}} + I_{23}$$

$$B_2 = I_3.\overline{I_7} + I_{11}\overline{I_{15}} + I_{19}\overline{I_{23}} + I_{27}$$

$$B_1 = I_1.\overline{I_3} + I_5.\overline{I_7} + I_9.\overline{I_{11}} + I_{13}.\overline{I_{15}} + I_{17}.\overline{I_{19}} + I_{21}.\overline{I_{23}} + I_{25}.\overline{I_{27}} + I_{29}$$

$$B_0 = I_0.\overline{I_1} + I_2.\overline{I_3} + I_4.\overline{I_5} + I_6.\overline{I_7} + I_8.\overline{I_9} + I_{10}.\overline{I_{11}} + I_{12}.\overline{I_{13}} + I_{14}.\overline{I_{15}} + I_{16}.\overline{I_{17}} + I_{18}.\overline{I_{19}} + I_{20}.\overline{I_{21}} + I_{22}.\overline{I_{23}} + I_{24}.\overline{I_{25}} + I_{26}.\overline{I_{27}} + I_{28}\overline{I_{29}} + I_{30}$$

IV. IMPLEMENTATION OF THE PROPOSED ENCODER

There are different logic styles to implement the design of thermometer code to 5 bit binary code. In order to avoid static power dissipation and to achieve moderate speed, the implementation is done using dynamic CMOS logic [5]. The basic construction of dynamic logic AND gate is shown in fig. 2.

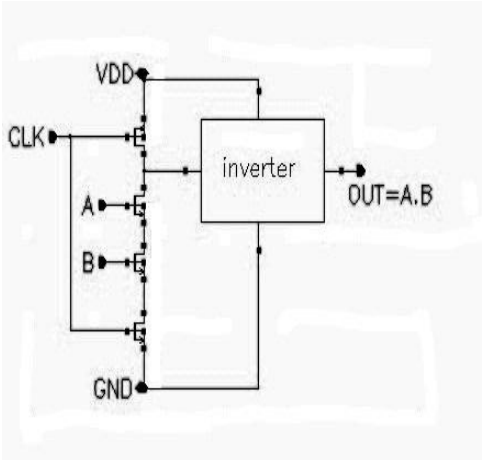
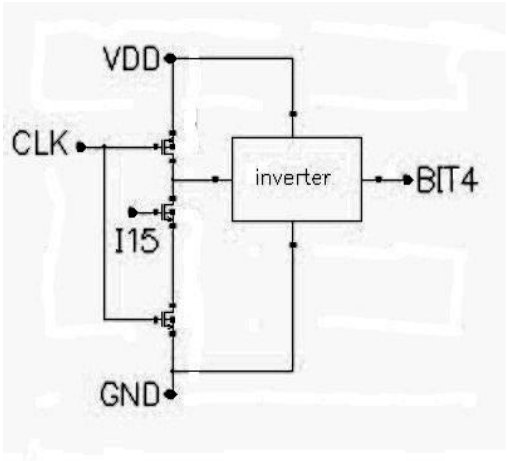


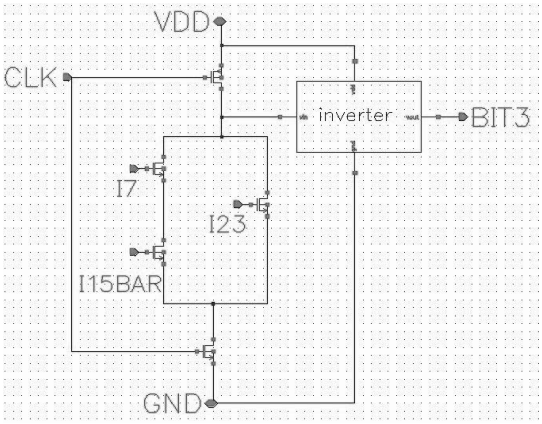
Fig. 2. Two Input AND Gate Using Dynamic Logic

Operation of the circuit is divided into two phases : precharge and evaluation. During the precharging time (CLK = 0) output node is precharged to VDD by the pullup PMOS transistor. The pull down network is off during this time independent of the condition of the other NMOS transistors, since one of the NMOS transistor id off which is connected to clock. This eliminates any static power which will be consumed during the precharging period. When CLK =1 (evaluation), the precharge transistor (PMOS transistor in the pull up path) is off and one of the NMOS transistor which is connected to CLK is switched on. The output is evaluated during this time depending upon the NMOS transistor conditions in the pull down network. The important part in the implementation of this encoder is that the inputs to this gate can make at most one transition during evaluation. When the pull down network is turned off, the output will be in high impedance state. The inverter in the output will invert the state and will give logic low or logic high value. Dynamic logic implementation

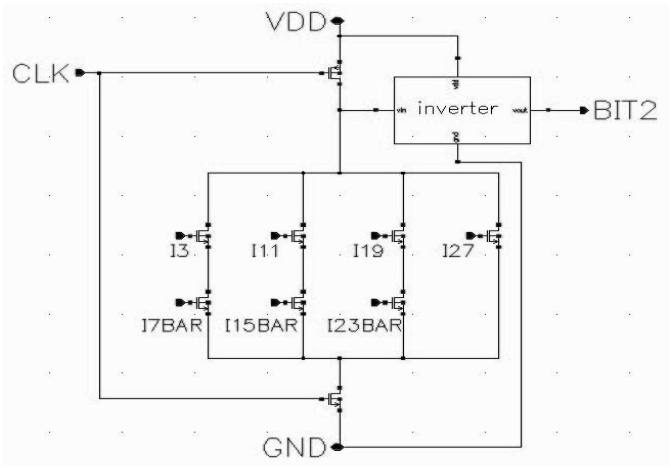
has faster switching speed in comparison with static CMOS because of the lower number of transistors required for implementation and single transistor load per fan in. The low and high output levels of V_{OL} and V_{OH} are GND and VDD. The schematic of the encoder for each bit is designed using proposed method and the schematic is shown in fig. 3.



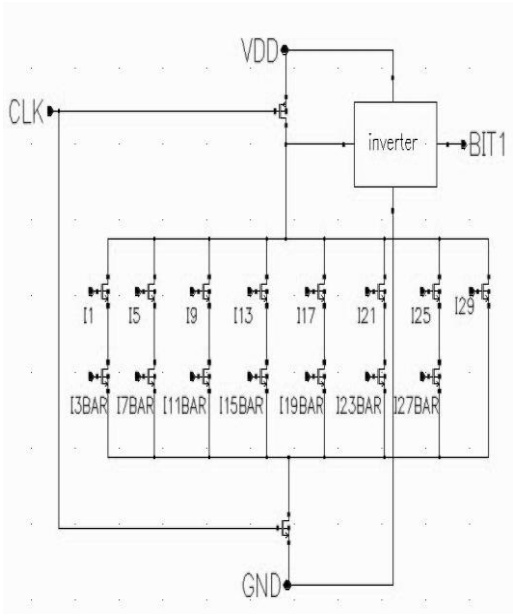
(a) Binary Code Bit 4 Generation Circuit



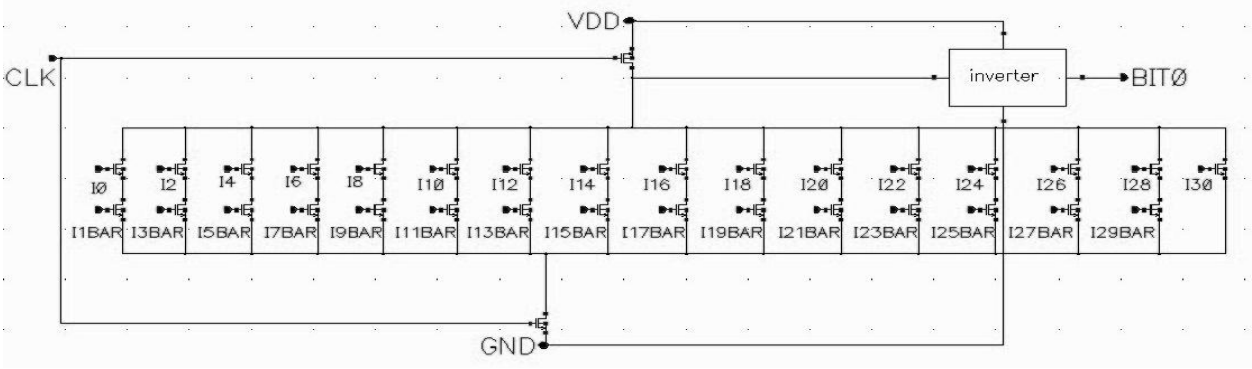
(b) Binary Code Bit3 Generation Circuit



(c) Binary Code Bit2 Generation Circuit



(d) Binary Code Bit 1 Generation Circuit



(e) Binary Code Bit 0 Generation Circuit

Fig. 3. Schematic of Binary Code Encoder using Dynamic CMOS Logic

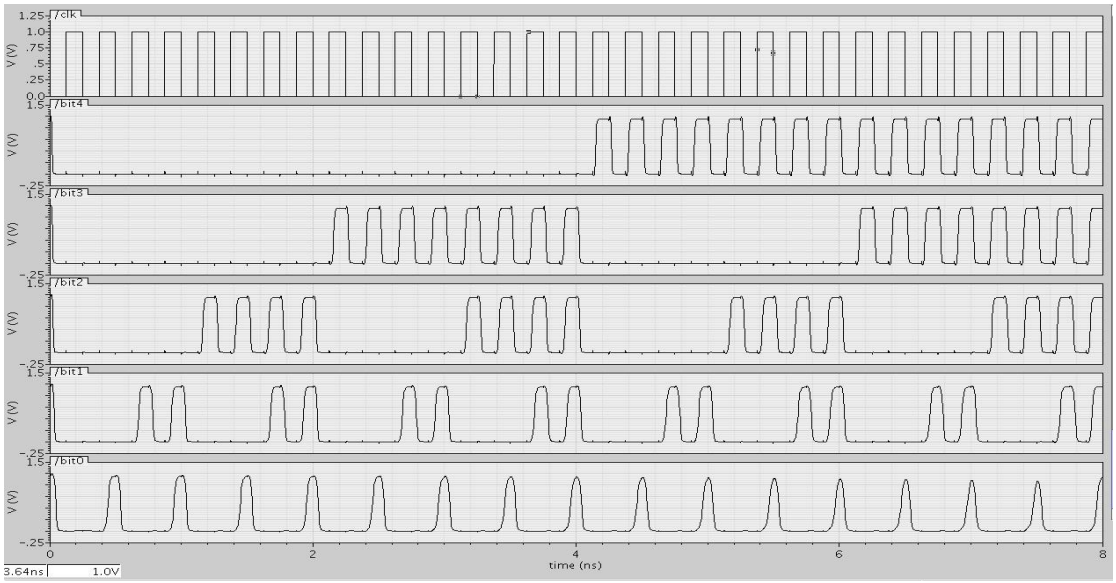


Fig. 4. Simulation of Binary Code Encoder

V. SIMULATION RESULTS AND DISCUSSION

The encoder is designed by combining all the five bits outputs, tested and verified using all the input combinations from the truth table using gpdk 90 nm technology with a 1.2 V supply. The simulation result is shown in fig. 4.

The maximum frequency of operation achieved using pseudo dynamic logic is 5 GHz for 4 bit output. As the resolution increases, the maximum frequency of operation will decrease. The summary of the encoder simulation results and compare with the pseudo dynamic encoder are presented in the table 2.

Results	Pseudo dynamic Encoder	Proposed Encoder
Architecture	Flash	Flash
Resolution	4 bits	5 bits
Technology	90 nm	90 nm
Sampling Frequency	5GHz	4 GHz
VDD	1.2V	1.2 V
Current	154 µA	1.5275 µA
Power Dissipation	184.8 µW	1.833 µW

Table2. Summary and Comparison of Proposed Encoder

The maximum sampling frequency that can be achieved using dynamic logic implementation is 4GHz for 5 output bits. The average power dissipation is 1.833 µW which is very low value in comparison with pseudo dynamic logic implementation. The results show that the new design consumes ultra low power than other types of encoders [3, 4, 6,7].

VI. CONCLUSION

The power dissipation of an encoder plays a major role in the design of flash ADC. The proposed encoder uses a dynamic CMOS logic to reduce the power dissipation by eliminating the presence of static power dissipation. The encoder is designed and simulated using gpdk 90 nm technology using CADENCE tool. The proposed encoder which operates at 4 GHz consumes 1.833 µW from 1.2 V.

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