An Improved Low Dynamic Power High Performance Adder

Sauvagya Ranjan Sahoo[1], Kamala Kanta Mahapatra[2]

Department of Electronics & Communication Engineering

National Institute of Technology Rourkela
Rourkela, India

[1]sauvagya.nitrkl@gmail.com

[2]kmaha@gmail.com

***Abstract*— This paper presents the design of a low power dynamic logic circuits using a new CMOS dynamic logic family called as low dynamic power dynamic logic i.e. LDPD. Dynamic logic styles are more significant because of its faster speed and lesser transistor requirement as compared to static CMOS logic styles. The proposed circuit has very less dynamic power consumption compared to the recently proposed circuit techniques for the dynamic logic styles. The proposed circuit is simulated using 0.18 µm, 1.8 V CMOS process technology. Intensive simulation results in Cadence environment shows that the proposed modified low-power structure reduces the dynamic power approximately by 36% for 10-stage of inverters and 4-bit ripple carry adder. The concept is validated through extensive simulation. The limitation of dynamic logic styles like charge redistribution and requirement of inverter during cascading are completely eliminated.**

***Keywords*- CMOS logic circuits, low-power, adder.**

I. INTRODUCTION

The design of low power CMOS integrated circuits, while maintaining its high performance is a challenge for designers. Dynamic logic are used for high speed circuit design, it reduces number of transistor to implement a given logic. The reduction in number of transistors results in significant reduction of area of the device. However, it is not widely used because of its excessive power dissipation due to the switching activity and clock as compared to static CMOS logic styles. In order to reduce excessive power dissipation of dynamic logic circuit, dual supply voltage technique in [1], dual V_T technique in [2], feedthrough logic (FTL) in [3], have been proposed. To reduce the power consumption of dynamic logic circuit further without affecting its performance a low dynamic power dynamic logic (LDPD) is proposed in [4].

The dynamic logic family i.e. LDPD in [4], improves the performance as comparison to dynamic domino CMOS circuits. This logic has additional feature that output is evaluated partially before all of its input are valid. This results in very fast evaluation time. The limitation of domino logic [5] like charge sharing, requirement of inverter for cascading are completely eliminated by LDPD.

The dynamic power dissipation in CMOS digital gate is given by in [6],

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$$P_{dynamic} = \alpha . C_L . V_{DD}^2 . f$$

Where α is the switching activity, C_L is the output node capacitance and V_{DD} is the power supply voltage, f is the clock frequency.

In this paper we present the design of a novel logic circuit using LDPD scheme. The proposed LDPD uses one additional PMOS transistor but the simulation results show that the power consumption of the proposed circuit reduces by approximately 36% when compared with the recent proposal. It can be used in domino like cascaded stage.

The rest of this section is organized as follows. The operation of existing LDPD is described in section II. Section III presents the design of novel circuit for low power. Simulation results and comparisons are discussed in section IV. Section V concludes with some final remarks and comments.

II. CONVENTIONAL LDPD

The basic structure of a inverter designed by conventional LDPD [4] is shown in Fig. 1.(a). It consists a reset transistor M_{N2} in series with M_{N3}, and a pull up PMOS load transistor M_{P1}. During CLK=1, the output node (OUT) is pulled to ground through M_{N3} depending upon IN value. If IN =1, OUT=0. During CLK=0 (evaluation phase), the output node initially rises to V_{TH} then according to IN value it is partially evaluated. If IN =1, OUT=V_{OL}, else OUT= V_{OH}. This logic is faster because the output makes transition from V_{TH} to V_{OH} or V_{OL} [4].

III. PROPOSED LDPD

The proposed LDPD is shown in Fig. 2. It consists of a PMOS transistor M_{P2} in series with M_{P1}. The insertion of additional PMOS transistor increases the total resistance in the path from V_{DD} to output. Due to ratio logic total power consumption reduces as compared to LDPD in [4]. During the reset phase the proposed LDPD circuit operation is same as conventional LDPD. During evaluation phase if IN = 1, then the output node (OUT) pulled down to logic low i.e. V_{OL}. This V_{OL} is small as compared to V_{OL} of conventional LDPD, as a result the power consumption of proposed LDPD reduces.

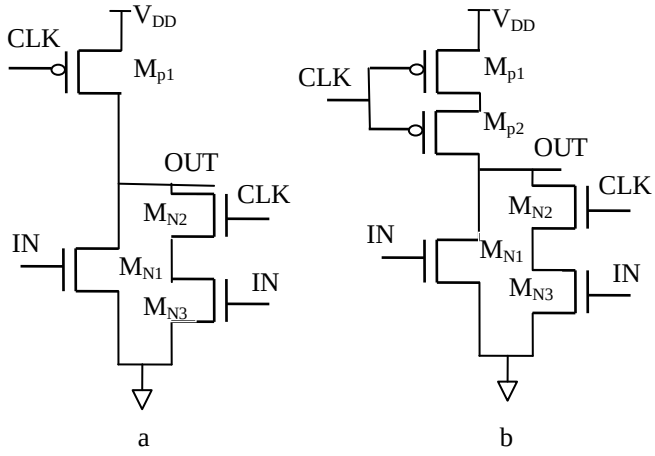

Fig.1 Inverter circuit in (a) LDPD in [4] (b) Proposed LDPD

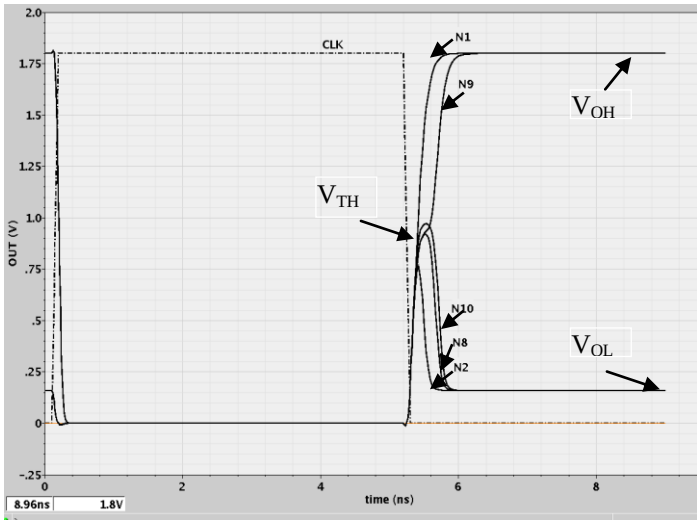

Fig. 2. Plot of the output voltages from 1st stage (N1) to 10th (N10) stage of inverters.

IV. Simulation Results and Comparisons

The design entry of the circuits is carried out in the cadence Analog Virtuoso Environment using 0.18 µm 1.8V CMOS process technology model library from UMC. Circuits are simulated in HSPICE simulator. The inverter designed by the proposed LDPD is compared with the inverter designed by LDPD [4]. Table 1 shows the dynamic power comparison for inverter shown in fig.1.(a), (b).

The values of dynamic power for a 10 stages of inverter with 10 fF capacitive loads in all output nodes are shown in Table II. It also shows the dynamic power comparison of 10-stage inverter in [4] and the proposed LDPD structure.

Fig. 2. shows the plot of output voltage from the 1st stage of inverter to the 10th stage of inverter at 10 fF capacitive loads for IN = 0. The output voltage falls to a lower voltage V_{OL} which is less than the V_{OL} in [4].

A full adder cell is designed by using the proposed LDPD structure. Table III. shows the dynamic power comparison for a 4-bit ripple carry adder designed by proposed logic and the existing structure in [4].

Table I. Simulation results for dynamic power for the LDPD in Fig. 1. (a) and proposed LDPD in Fig. 1. (b).

Logic family	Power(µW)
LDPD in [4]	39.8
Proposed LDPD	24.5

Table II. Simulation results for dynamic power for the proposed circuit and the existing LDPD structure in [4]. (10-inverter)

Logic family	Power(µW)
LDPD in [4]	408
Proposed LDPD	254

Table III. Simulation results for dynamic power for an 4-bit ripple carry adder designed by proposed circuit and the existing LDPD structure in [4]

Logic family	Power(µW)
LDPD in [4]	507
Proposed LDPD	323

V. Conclusions

In this paper, we proposed a novel low power dynamic circuit. The proposed circuit is simulated in 0.18 µm CMOS process technology from UMC. The proposed circuit when compared with the recently proposed FTL scheme has 36% less dynamic power consumption. The simulation for a 4-bit ripple carry adder is also carried out in this work. The proposed circuit can be used for design of a low power processor where power consumption is of primary importance.

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