An Improved Feedthrough Logic for Low Power Circuit Design

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***Abstract*—This paper presents the design of a low power dynamic circuit using a new CMOS domino logic family called feedthrough logic. Dynamic logic circuits are more significant because of its faster speed and lesser transistor requirement as compared to static CMOS logic circuits. The proposed circuit has very low dynamic power consumption compared to the recently proposed circuit techniques for the dynamic logic styles. The concept is validated through extensive simulation. The problem of requirement of output inverter and non-inverting logic are also completely eliminated in the proposed design.**

***Keywords*- Feedthrough logic (FTL);dynamic CMOS logic circuit; low-power adder.**

I. INTRODUCTION

Dynamic logic is used for high speed circuit design; it reduces the number of transistors to implement a given logic. The reduction in number of transistors results in significant reduction of area of the device as compared to static CMOS logic [1,2,3], but the major drawback with this logic is its excessive power dissipation due to the switching activity and clock, also it suffers from charge redistribution and requirement of additional output inverter. In order to reduce excessive power dissipation of dynamic logic circuit, a mix of dynamic and static circuit styles [4], use of dual supply voltages [5] and dual threshold voltage (V_T) [6] have been proposed in the literature.

To improve the power consumption of dynamic logic circuit with a very long logic depth further, a new logic family called feedthrough logic (FTL) is proposed in [7], where FTL concept is extended for the design of low power arithmetic circuits.

FTL is successfully employed by the authors for integrated circuits in GaAs technology in [8]. Furthermore, the problems associated with dynamic logic in [1] is eliminated by FTL [7].

The total power dissipated in a generic CMOS digital gate is given by [9]

$$P_{total} = P_{static} + P_{dynamic} + P_{short\,circuit}$$
$$= V_{dd} I_l + V_{dd} F_{clk} \sum_i V_{i\ swing} C_{i\ load} \alpha_i + V_{dd} \sum_i I_{i\,sc}$$

Where F_{clk} denotes the system clock frequency, $V_{i\,swing}$ is the voltage swing at node i, $C_{i\,load}$ is the load capacitance at node i, α_i the activity factor at node i, $I_{i\,sc}$ is the short circuit current and I_l is the leakage current.

In this paper we propose a novel circuit design that further improves feedthrough logic [7]. The proposed circuit uses one additional PMOS transistor. the simulation results show that the power consumption of the proposed circuit reduces by approximately 40% when compared with FTL [7]. It can also be used in domino like cascaded stage.

II. CONVENTIONAL HIGH SPEED STRUCTURE (HS0)

The high speed structure (HS0) in [7] is shown in Fig. 1. It consists of a NMOS reset transistor (M2) and a pull up PMOS load transistor (M1). M1 and M2 are controlled by the clock signal (CLK). The basic principle of operation is briefly described here. During CLK =1 (reset phase), the output node (OUT) is pulled to ground through M2. When CLK =0 (evaluation phase), M2 is turned off and M1 conducts. The output node conditionally evaluates to either logic high or low level depending upon input (IN) to M3. If the IN=0, the output node is pulled towards V_{DD}, otherwise it remains at low. In standard domino logic [1] the output is charged to V_{DD} which cause cascading problem and high dynamic power dissipation but here the output is reset to low during reset phase. This eliminates the requirement of inverter for cascading these logic blocks. This logic is faster because the output makes transition from V_{TH} to V_{OH} or V_{OL} only [7], but it suffers from more power consumption due to the fact that V_{OL} is not 0 V.

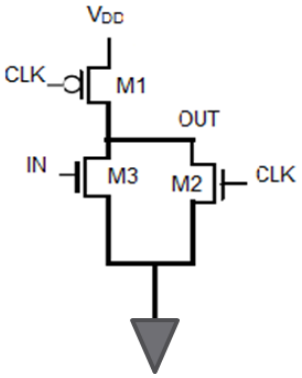

Fig. 1. HS0 Structure in [7]

III. PROPOSED CIRCUIT

The proposed circuit for low power is shown in Fig. 2. It consists of an additional PMOS transistor (M4) in series with M1. The transistor M4 increases the total resistance in the path from V_{DD} to output. Due to ratio logic V_{OL} reduces as compared to HS0 [7]. This reduction in V_{OL} helps in reducing the dynamic power consumption

During the reset phase the proposed HS0 circuit operation is same as HS0 [7]. During evaluation phase if the input (IN) is logic-1 then the output node pulled down to logic low i.e. V_{OL}. This V_{OL} is small as compared to V_{OL} of HS0 [7], as a result the power consumption of proposed HS0 reduces.

IV. FULL ADDER DESIGN USING PROPOSED HS0

In this section we present the design of a basic sum and carry cell for the full adder using proposed HS0 logic. Fig.3. shows the implementation of $\overline{sum}$ and Fig. 4. shows $\overline{c_{out}}$ of the adder. An 8-bit ripple carry adder is designed by using these basic sum and carry cell.

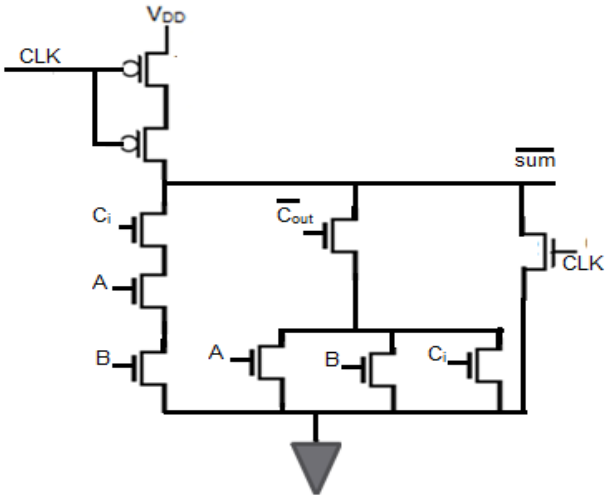

Fig. 3. Sum cell

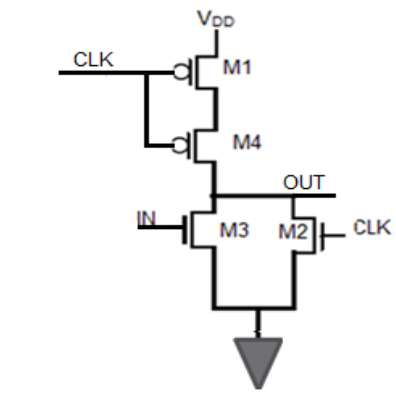

Fig. 2. Proposed HS0

V. SIMULATION RESULTS AND COMPARISONS

We have used 0.18 µm CMOS process technology model library from UMC, using the parameter for typical process corner at 25^0C. Power supply V_{DD} is constant for all simulations and is equal to 1.8 V. Circuits are simulated in HSPICE simulator. To compare the proposed structure against the existing HS0 structure [7], the behavior of a long chain (10) of inverters and 8-bit ripple carry adders are simulated. Table I. shows the dynamic power comparison for 10 stages of inverter designed by proposed HS0 shown in Fig.5, and existing HS0 in [7] for 10 fF capacitive load at 100 MHz.

Fig. 6. Show the plot of output voltage from the 1st stage of inverter to the 10th stage of inverter at 10 fF capacitive loads. The output voltage falls to a lower voltage V_{OL} which is less than the V_{OL} in [7].

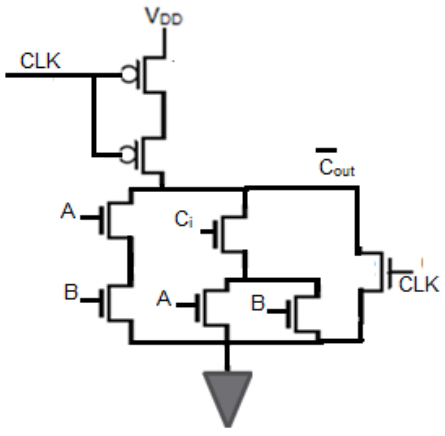

Fig. 4. Carry cell

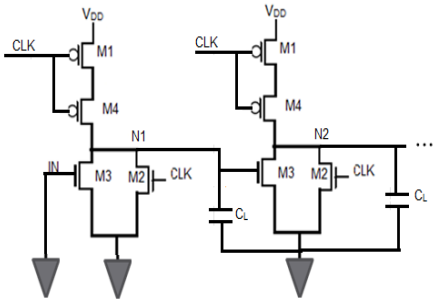

Fig. 5.Long chain of inverters designed by proposed HS0 (10-stage)

An 8-bit ripple carry adder is designed by using the sum and carry cell shown in Fig. 3 and Fig. 4. Table II. illustrates the propagation delay and dynamic power comparison for the 8-bit ripple carry adder designed by the proposed structure and existing HS0 in [7]. The simulation result indicates that power consumption for the proposed adder is very low as compared to the existing adder in [7].

TABLE I. SIMULATION RESULTS FOR DYNAMIC POWER FOR THE PROPOSED CIRCUIT IN FIG.5 AND THE EXISTING HS0 STRUCTURE IN [7]. (10-INVERTER)

Logic family	**Power(µW)**
HS0 in [7]	268
Proposed HS0	151

TABLE II. SIMULATION RESULTS FOR DYNAMIC POWER FOR AN 8-BIT RIPPLE CARRY ADDER DESIGNED BY PROPOSED CIRCUIT AND THE EXISTING HS0 STRUCTURE IN [7]

Logic family	**Power(µW)**	**t_p (ns)**
HS0 in [7]	601	0.507
Proposed HS0	335	0.690

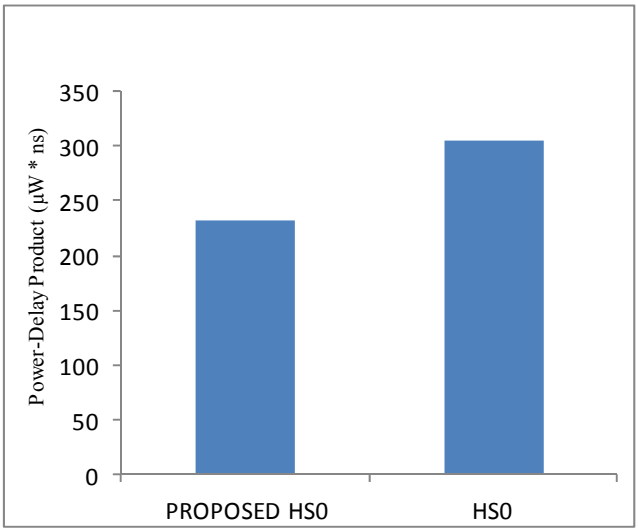

Fig.7. Power delay poduct of proposed structure and existing HS0

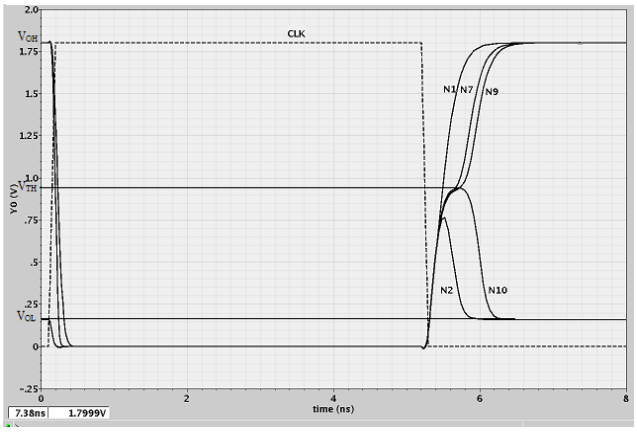

Fig. 6. Plot of the output voltages from 1st stage (N1) to 10th (N10) stage of inverters.

The power delay product is shown in Fig.7. The PDP chart confirms that the proposed structure has less PDP as compared to HS0 in [7].

In Fig.8. The propagation delays of both structures are shown with respect to output load capacitance C_L. The gap between proposed structure and HS0 in [7] increases with increase in C_L. The proposed circuit is slower as compared to HS0.

The effect of C_L on dynamic power for both structure are shown in Fig.9. C_L is varies from 1 fF to 20 fF. The dynamic power dissipation of the proposed structure is less as compared to HS0.

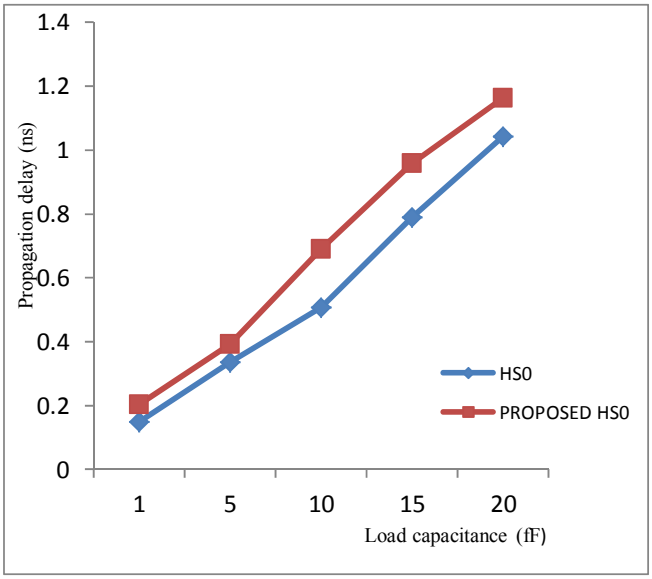

Fig.8. Effect of output load on propagation delay of proposed structure and existing HS0

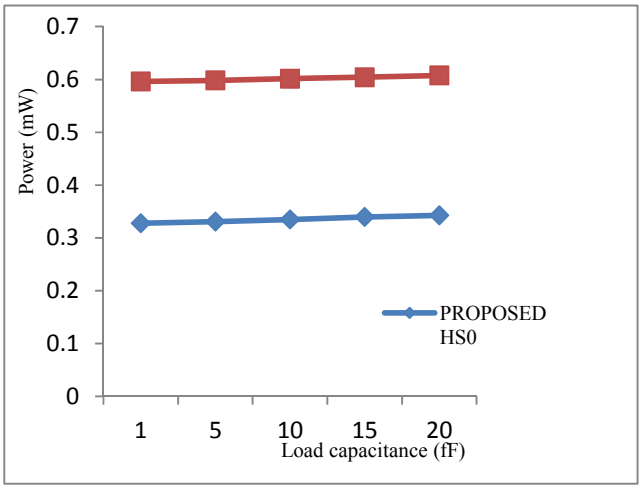

Fig.9. Effect of output load capacitance on dynamic power dissipation of proposed structure and existing HS0 .

VI. CONCLUSION

In this paper, we proposed a low power dynamic circuit. The proposed circuit is simulated in 0.18 µm CMOS process technology from UMC. The proposed circuit when compared with the recently proposed FTL scheme has 40% less dynamic power consumption. The simulation for a 8-bit ripple carry adder is also carried out in this work. The simulation result confirms that for a given load and at same frequency of operation the power delay product of the proposed circuit improves than that of existing HS0 structure. The proposed circuit can be used for design of a low power processor where low power consumption is of primary importance.

ACKNOWLEDGMENT

The authors acknowledge to DIT (Ministry of Information & Communication Technology) for the financial support for carrying out this research work.

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