Design of LC VCO for optimal figure of merit performance using CMODE

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***Abstract*— FOM (Figure Of Merit) is a novel performance yardstick of VCOs. Designing LC VCO circuit with desired specifications is highly time consuming and tedious job. In this paper CMODE (Combining Multi objective Optimization with Differential Evolution) optimization technique is used to design an LC VCO of optimal FOM with a target frequency of 2.5 GHz. The design parameters of LC VCO are obtained from the CMODE algorithm used in the MATLAB environment to optimize FOM. By using these parameters the LC VCO circuit is designed and synthesized in 90 nm CMOS technology in the Cadence Spectre Analog Design Environment(ADE). This VCO achieves phase noise of -119.7 dBc/Hz at 1 MHz offset while consuming 515 uW power with a tuning range of 10.53%. The FOM is obtained to be -190.26 dBc/Hz at 1 MHz offset. Hence the best performance index meeting the desired specifications is obtained in a single run of the algorithm.**

Keywords-FOM; LC Tank; Combining Multi-objective Optimization with Differential Evolution (CMODE), Tail current source.

I. INTRODUCTION

LC VCOs are ubiquitous in PLLs, which are integrated part of RFIC design, play an important role in Bluetooth integrated Wireless Local Area Network (WLAN), and WiMAX LTE(Long Term Evolution). The performance indices of the VCO can strongly affect the performance of the afore said applications. Due to their low phase noise wide tuning range, LC VCOs are extensively used in RF transceivers. Due to its low power consumption it can be used in 2.5 GHz Industrial Scientific Medical (ISM) bands where very low power devices are required.

The oscillator power consumption can be a significant portion of the total power consumption of a system. So over-all power consumption can be reduced by minimizing the power consumption of the VCO. But there exist a several number of tradeoffs among the important parameters like power, noise, frequency, gain in RFIC designs. FOM is a quantity to measure the performance of a device relative to its alternatives. Due to the tradeoff between the power and phase noise for a particular frequency of oscillation a standard FOM as mentioned in (5) can be taken in to consideration.

Many researchers have proposed different LC VCO designs for achieving low phase noise but the power consumption is very high[1][2][3]. In this paper we propose an optimization technique which finds design parameters of an differential CMOS LC VCO with low phase noise and very low power consumption. In section II the architecture and general theory of LC VCO has been discussed. In section III the algorithm of optimization technique, CMODE [4] has been described. In section IV the practical design specifications for an LC VCO has been discussed. In section V the simulation results pertaining proposed optimal design have been shown and compared with the results of some recent papers. The last section summarizes the utility and relevance of the CMODE optimization technique in the field of RFIC design.

II. THEORY OF VCO DESIGN

A. *Architecture of LC VCO*

The schematic of 2.5GHz LC VCO is shown in Fig.1. The complementary cross-coupled LC VCO [2] is employed in this design with the help of two varactors [5] by which the VCO frequency is adjustable.

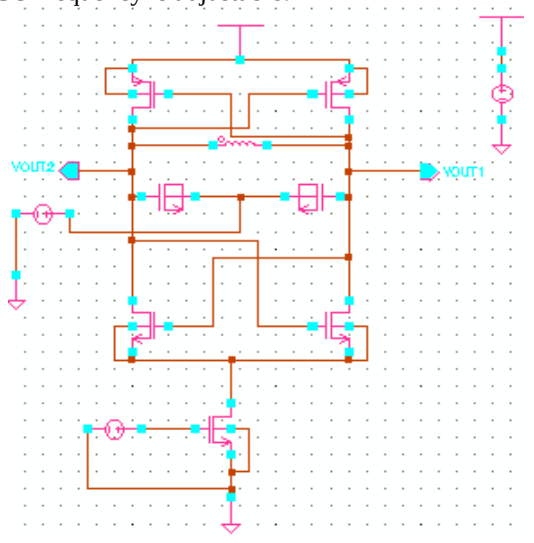

Fig-1

The cross-coupled VCO operates as switch during oscillating, and two cross-coupled pairs work on the saturation when oscillation is stable. It is possible to compensate the loss of the tank with less current consumption by using a PMOS pair here. Furthermore by observing the symmetry properties of oscillating waveform

and making sure the trans-conductance of PMOS and NMOS transistors to be equal, it is possible to reduce the up-conversion of $1/f$ noise of the devices around the carrier, thus to lower the phase noise.

B. Frequency of oscillation and Tuning Range

The tuning range of a VCO is required to be in excess of a certain minimum percentage of the centre frequency ω_0 (frequency of oscillation). The LC tank is made tunable by implementing the *'C'* of the LC tank using varactors (variable capacitor) shown in Fig:1. The varactor is designed to be adjustable over some range $C_{tank\text{-}min}$ to $C_{tank\text{-}max}$. The frequency of oscillation for an ideal tank is,

$$\omega_0 = \frac{1}{\sqrt[2]{LC}}$$

Taking in to consideration all the parasitic capacitances of the NMOS pair of the VCO shown in fig.1, the frequency of oscillation can be derived as,

$$\omega_0 = \frac{1}{\sqrt[2]{L(C + C_{gs} + 4C_{gdo})}} \sqrt[2]{1 - \frac{R^2 (C + C_{gs} + 4C_{gdo})}{L}} \quad (1)$$

The tuning range of the VCO is defined as,

$$(\omega_{max} - \omega_{min}) / \omega_0$$

Here it can be seen that the transistor capacitances more or less simply add to the tank capacitance, *C*, requiring a decrease in *C* compared to the ideal case for a given ω_0.

C. Phase noise analysis

The sources from where the noise is contributed in the circuit include LC Tank, CMOS cross coupled pair and tail current source [6]. Thermal and flicker noise are the main constituent of the overall noise. By up conversion and down conversion these noises go in to the output phase noise. Generally $1/f_2$ region consists of thermal noise and $1/f_3$ region consists of flicker noise. However Tail current source produces a large amount of noise.

According to original Leeson's phase noise formula [7],

$$L(\Delta\omega) = 10\log\left\{\frac{4FKTR}{V_0^2}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_1 / f^3}{|\Delta\omega|}\right)\right\} \quad (2)$$

Or,

$$L(\Delta\omega) = 10\log\left\{F\frac{KT}{2P_{sig}}\frac{\omega_0}{Q\Delta\omega}\right\} \quad (3)$$

Where Q is the loaded quality factor of the LC-tank, $\Delta\omega$ is the frequency offset, ω_0 is the oscillating frequency, P_{sig} is the average signal power, $\Delta\omega_{1/f3}$ is the corner frequency [8] between $\omega_{1/f2}$ and $\omega_{1/f3}$ portion of the phase noise spectrum, *F* is the device noise factor. For CMOS oscillator, the *F* term [1]can be expressed as:

$$F = 1 + \frac{K_1 \gamma I_{bias} R}{V} + K_2 \gamma g_{bias} R \quad (4)$$

Where K_1, K_2 are constants. γ is a FET noise factor (2/3 for long channel and more than that for short channel devices), g_{bias} refers to the current source trans-conductance and R is the tank resistance. V is the output voltage swing.

D. Figure Of Merit

The performance of VCOs is difficult to compare as they feature different center frequencies, power consumption and phase noise over different offset frequencies. A standard formula for Figure Of Merit has been mentioned here,

$$FOM = 10\log_{10}\left[PN\left(\frac{\Delta\omega}{\omega_0}\right)^2\right]\left(\frac{P_d}{0.001}\right) \quad (5)$$

Where,

$$PN = \left\{\frac{4FKTR}{V_0^2}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_1 / f^3}{|\Delta\omega|}\right)\right\}$$

P_d= Power dissipated

The performance of the VCO is regarded to be better with a more negative value or higher absolute value of FOM.

III. Optimization Technique For LC VCO Design

Optimization problem having more than one objective and constraints adds more complexity. The LC VCO design problem we considered in this paper is to determine the values of the design parameters that optimize the multiple objective measures while satisfying different constraints. Combining Multi-objective Optimization with Differential Evolution (CMODE) is an efficient optimization technique in which the design parameters for optimal performance can be obtained for a given set of constraints. In this work the optimization of the LC VCO circuit is carried out by using CMODE with desired frequency of oscillation. The optimization problem is mainly focused on the sizing of the transistors, inductor and varactors in the circuit to meet the targeted frequency of oscillation with minimal FOM described in (5) within the process constraints.

CMODE Algorithm

Inputs:

N_p: Population size

λ: Number of candidates/agents to take part in DE operation

k: The generation gap for implementing the infeasible solution replacement mechanism

Max_FES: Maximum number of function evaluations

Output: $\vec{x}^*$*:* The best solution of the final population

All the steps have been mentioned briefly below.

1. **Initialization**

- An initial population of size N_P can be randomly generated from the decision space *S*.
- $P_{(t)}=\{\vec{x}_1, \vec{x}_2, \ldots, \vec{x}_{Np}\}$ where *t* denotes the generation number.

- The f and G value of each candidate in initial population can be calculated. Objective function values of the candidates are $f(\vec{x}_1)$, $f(\vec{x}_2)$, ...$f(\vec{x}_{Np})$ and their degree of constraint violations are $G(\vec{x}_1)$, $G(\vec{x}_2)$, ...$G(\vec{x}_{Np})$.
- Set FES(Number of function evaluations)= N_p
- Set A(Archive which is used to store the infeasible candidate which has lowest degree of constraint violation)=Φ
- Initialize t(Generation number) to 1

2. Population evolution model

- Randomly choose λ candidates from population $P_{(t)}$ as set Q
- Now $P_{(t)}= P_{(t)}- Q$
- By using mutation and crossover techniques in DE explained earlier an offspring is created from each candidate in Q. So λ offspring (set C) can be produced.
- The f and G value of each candidate in C are to be evaluated.
- Now FES gets updated to $FES+ \lambda$.
- Make a set R consisting of identified non dominated candidates from C.
- Assume there exists m non dominated candidates denoted as $\vec{x}_1$, $\vec{x}_2$, ..., $\vec{x}_m$
- Consider there are n candidates in Q dominated by $\vec{x}_1$. *If* $n \geq 1$, then one of the dominated candidates chosen at random can be replaced by $\vec{x}_1$
- Now the remaining non dominated candidates of R can continue the same process for the updated Q progressively.
- $P_{(t)}= P_{(t)}U\ Q$

After combining the updated Q with $P(t)$, the update of $P(t)$ is also achieved.

3. Archiving infeasible solution and replacement

- If R does not have any feasible solution, then $A = A\ U\ \vec{x}'$ Where $\vec{x}'$ is the infeasible individual with the lowest degree of constraint violation in R.
- If $mod(t,k)=0$, then the infeasible solution replacement mechanism can be executed and $A=\varphi$.

Every k generations, all of the infeasible candidates in A are used to replace the same number of individuals in P(t).

4. Now set *t=t+1*

5. Stopping criterion: If $FES \geq Max\_FES$ is satisfied then the process will be stopped and the best solution $\vec{x}^*$ in P(t) will be the output. Otherwise the process will restart from step 2.

IV. Design Of Optimal LC VCO

Using the CMODE optimization technique a simple LC VCO as depicted in Fig-1 of 2.5 GHz frequency of oscillation constrained by gpdk090 process technology library has been designed. The simulation has been carried out in Cadence Spectre ADE and the FOM is found out to be -190.26 dBc/Hz at 1 MHz offset. Here the following constraints are satisfied where the phase noise and power consumption are minimized simultaneously. The design considerations are stated as follows,

Minimize: *FOM*
Constraints:

$2.2\ GHz < f_{osc} < 2.5GHz$
$V_{Tank}\ swing \geq V_{dd} = 1.8\ V$
$1um < W_n < 5um$
$100nm < L < 120nm$
$5um < W_p < 10um$
$1um < W_{nbias} < 5um$
$Loop\ gain \geq 2$
$0.1\ nH < L < 10\ nH$
$0.1\ pF < C < 10\ Pf$
$5 < Q < 10$
$V_{dd} = 1.8\ V$

Where W and L are the width and length of the transistors. Q is the quality factor of the inductor. To optimize the phase noise and power simultaneously the proposed optimization technique provides the proper value of the design variables mentioned above using the necessary design equations mentioned below.

- Trans conductance of NMOS,

$$g_m = \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd0})}{L}$$

- Figure Of Merit as mentioned in (5).
- Maximum power dissipation, $P_{dc}=V_{supply}\ I_{bias}$
- Oscillation Frequency as mentioned in (1)

V. Simulation Results

The results obtained from the simulation of the LC VCO design in CADENCE SPECTRE ADE shows that the power consumption has drastically been reduced compared to the latest papers as shown in table-1. The phase noise is also considerably good where the FOM is found to be very good.

The phase noise gets automatically increased while the power consumption is reduced. So there is a tradeoff between the power consumption and phase noise. Hence the equation of FOM has been taken up for optimization in this work so that a standard performance comparison can be done irrespective of the phase noise and power consumption.

The transient analysis, phase noise curve and the tuning range has been shown in figure 2-4 respectively.

As in the constraints, the loop gain is mentioned to be more than or equal to 2, the amplitude of the output transient curve is more than 1.8 V which is double of the

control voltage. The mid frequency of this VCO is measured to be 2.42.

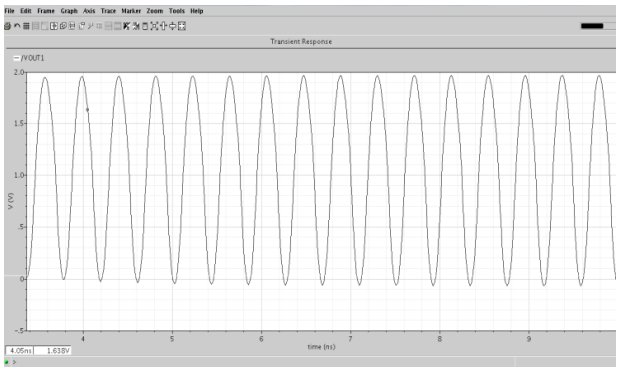

Fig-2

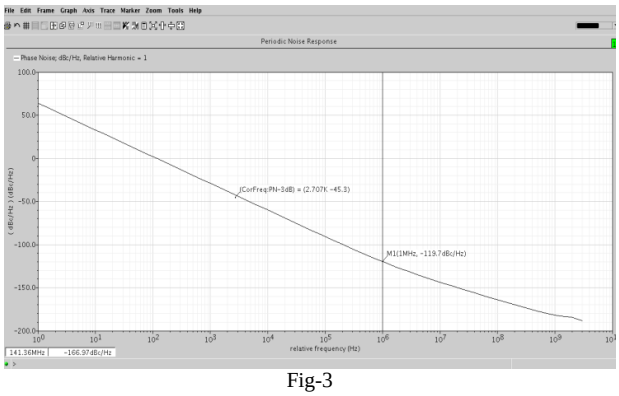

Fig-3

The phase noise is found to be -119.7 dBc/Hz at 1 MHz offset frequency and a very good tuning range of 10.53 is achieved.

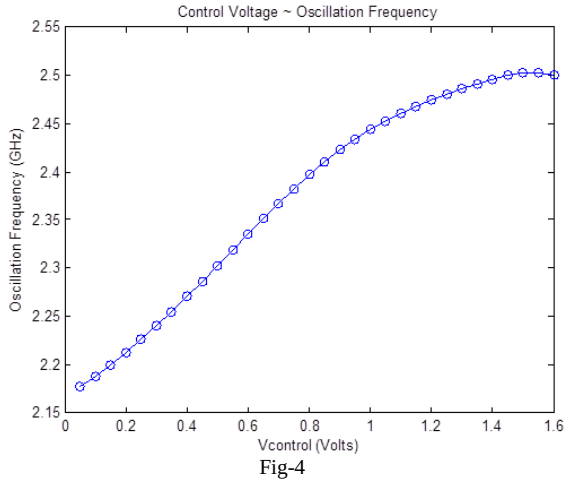

Fig-4

A brief description of the performance summary and comparison with published work has been mentioned in Table-1. The power consumption is noted to be best among all others. The reason of very low power consumption is the candid selection of optimum values for V_{bias}, *L and C* of the LC VCO by CMODE guided by power cap and other constraints.

TABLE I. COMPARISION

Ref.	**Freq.** (GHz)	**V_{dd} (V)**	**P_{dc}** mW	**L(Δω)** dBc/Hz @ 1MHz	**Tuning Range (%)**	**FOM (dBc/Hz)** @1MHz
[1]	2.5	1.8	5.4	-128.7	11	-
[2]	2.4	1.8	3.99	-130.5	-	-
[3]	2.72	1.2	0.812	-123.2	8	-192.7
This work	2.42	1.8	0.515	-119.7	10.53	-190.26

VI. CONCLUSION

Here the design of optimal CMOS LC VCO using CMODE optimization technique in the constrained environment is presented. The performance index FOM mentioned in (5) is minimized using this technique. The optimized design parameters found out from the technique are used in the CADENCE SPECTRE Analog Design Environment for circuit behavior simulation and synthesis. The LC VCO performance indices, phase noise and power consumption are measured to be -119.7 dBc/Hz at 1 MHz offset and 515.68 uW respectively. The measured output frequency of oscillation is observed to be 2.4227 GHz which is close to the desired frequency of 2.5 GHz and has a tuning range of 10.53%. The FOM value at 2.42 GHz is found to be -190.26 dBc/Hz at a offset frequency of 1 MHz. This work can be extended in several other dimensions such as the chip area and tuning range as performance indices for optimization. The used technique provides the optimal design parameters in a single run which saves lot of time and design cost. So by using this technique the time to market and NRE cost can be minimized.

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