CLASS-C POWER AMPLIFIER DESIGN FOR GSM APPLICATION

Lopamudra Samal,
Electronics Communication Department,
National Institute of Technology,
Rourkela, INDIA
Email:lopamudrasamals@gmail.com

Prof K. K. Mahapatra,
Electronics Communication Department,
National Institute of Technology,
Rourkela, INDIA
Email:kkm@nitrkl.ac.in

Raghu Ram
Electronics Communication Department
National Institute of Technology,
Rourkela, INDIA
Email:raghu88.ram@gmail.com

Abstract- **This paper presents a Class C Power Amplifier (PA) design with better efficiency for Global System for Mobile communications (GSM) application. This design is implemented in 90nm CMOS technology, which consumes low power (around 1 Watt). This designed circuit is simulated and validated for different frequencies in between 935-960 MHz; this frequency range usually adopted in GSM applications. This circuit has efficiency of 50% and output gain is 23.15 dB.**

Key words-Class-C power amplifier; CMOS technology; GSM

I. INTRODUCTION

A power amplifier is always a final block in the transmission path of a transceiver. It amplifies a signal to sufficient power level that ensures a transmitted signal to propagate across some distance and be received at the receiver end like in GSM or similar application. Power amplifiers are used at different places which have a lot of applications.

CMOS technology reduces integration cost; hence it is used in building many integrated systems. It is also better than other options when it comes to large scale integration. However, CMOS is poor for RF circuits. It has poor current drive and large associated parasitic capacitances [1]. The dilemma of integrating the power amplifier within CMOS arises because of these technological limitations that severely limit the efficiency of power amplification. At the cost of linearity, greater levels of amplification are achieved. The primary distinction between these power amplifier classes is the fraction of the RF cycle for which the transistor conducts. For class A PAs, the transistor is conducting for the entire RF cycle, whereas for class B PAs it is ON for half the RF cycle, and for less than half the RF cycle for class C PA. Class A, AB, and B amplifiers may be used as linear PAs, whereas class C is more nonlinear in nature [4].

The class C amplifier is biased below its turn-on voltage and the input drives the device on for a small portion, which is less than half of the input cycle. This results into a pulsed current in the device. This current is filtered to extract the fundamental frequency component, which is then passed to the resistive load. The output waveform is thus at the fundamental frequency. The efficiency of class-C power amplifier varies from 50% to 85%.

In this paper, a Class-C amplifier is design and discussed along with the actual implementation using CMOS technology within the Cadence environment. It consumes low power and improves the efficiency of the Mobile communications. Section II discusses about the design of class C power amplifier and section III deliberates the simulation results. Conclusions are brought out in section IV.

II. DESIGN OF CLASS-C PA

A. Operating principle of Class-C PA

The operating point of the transistor is located in the cutoff region. The dc component of the gate-to-source voltage V_{GS} is less than the transistor threshold voltage V_t. Therefore, the conduction angle of the drain current (2θ) is less than 180°. Voltage and current waveforms in the Class-C PA are shown in Fig. 1.

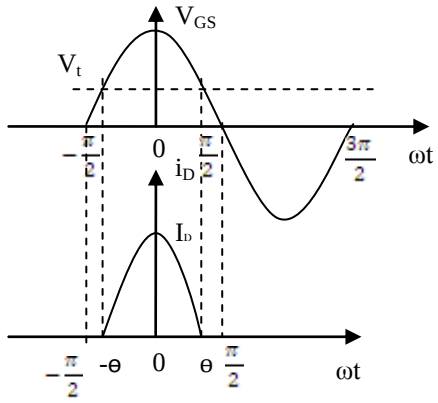

Figure 1. Waveforms in Class-C RF power amplifier

The only difference is the conduction angle of the drain current, which is determined by the operating point. The drain current waveform for any conduction angle θ (at some places the conduction angle is represented as "Y") is given by

$$i_D = \begin{cases} I_{DM}\dfrac{\cos\varpi t - \cos\theta}{1-\cos\theta} & for -\theta < \varpi t < \theta \\ 0 & for \theta < \varpi t < 2\pi - \theta \end{cases} \quad (1)$$

Where, I_{DM} is the maximum drain current. Class-C PA has the highest drain efficiency. If the conduction angle shrinks towards zero, the efficiency approaches 100% [7]. But Class-C PA has more distortion than other linear PAs. This

disadvantage must be overcome. Lot of work has been done to improve the linearity of PAs [8-11].

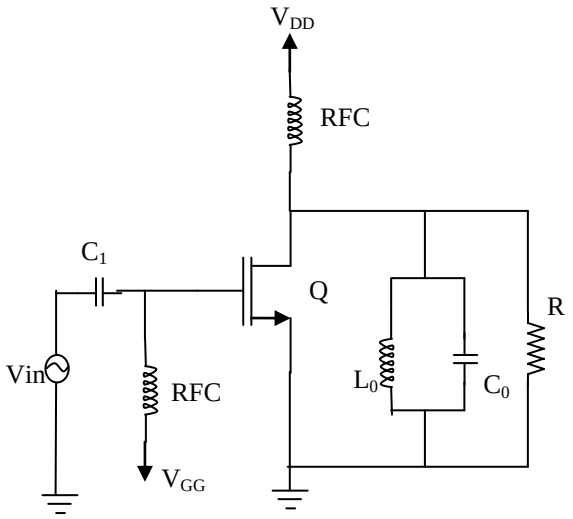

Figure 2. Single-ended Power Amplifier (Class C)

The efficiency of a power amplifier is increased from 50% for a class-A power amplifier to 78% for a class-B power amplifier with the conduction angle decreased from 360° to 180°. It is observed that efficiency greater than 78% can be achieved if the condition angle is further reduced to a level smaller than 180°. The resultant power amplifier is categorized as class-C. In fact, the circuit topologies can be the same for class-A, class-AB, class-B and class-C PAs. The transistor in a class-A, class-AB, class-B and class-C power amplifiers is operated as a current source. The major difference associated with these four types of power amplifier is the biasing condition. With the reduction in condition angle, the efficiency is traded-off with the linearity from class-A to class-C PAs. The price of achieving high efficiency is the poor linearity performance. Moreover, although the efficiency can approach 100% with conduction angle trends to zero, the output power will be zero since there is no drain current at all. Fig. 2 shows the circuit diagram of a single ended class-C power amplifier circuit diagram. Class-C amplifier is the one biased so that the output current is zero for more than one half of an input sinusoidal signal cycle. A tuned circuit or filter is a necessary part of the class-C amplifier. In the circuit radio frequency choke *(*RFC*)* is also used. The amplifier's efficiency is a measure of its ability to convert the dc power of the supply into the signal power delivered to the load. The efficiency can be represented by

$$\eta = \frac{\text{Signal power delivered to load}}{\text{DC power Supplied to output circuit}} \qquad (2)$$

The efficiency of power amplifier can be defined in terms of conduction angle Y.

$$Y = \arccos\left(-\frac{I_{dq}}{I_{dd}}\right) \qquad (3)$$

The dc current is

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_D(\varpi t)\, d\varpi t$$

$$= \frac{1}{\pi}(I_{dq}.Y - I_{dd}.\sin(Y))$$

$$= \frac{I_{dd}}{\pi}\left(\sin(Y) - Y\cos(Y)\right) \qquad (4)$$

The output voltage (V_{out}) in term of Y is

$$V_{out} = \frac{I_{dd}.R}{2\pi}\left[2Y - \sin(2Y)\right] \qquad (5)$$

The output power is

$$P_o = \frac{V_{out}^{\ 2}}{R} \qquad (6)$$

The dc power is

$$P_{dc} = V_{cc}.I_{dd} \qquad (7)$$

And the maximum output voltage V_{OMAX} is

$$V_{OMAX} = V_{DD} \qquad (8)$$

From the above equations the maximum efficiency is

$$\eta = \frac{P_{OMAX}}{P_i} = \frac{2Y - \sin(2Y)}{4(\sin(Y) - Y\cos(Y))} \qquad (9)$$

Here P_{OMAX} is the maximum output power and P_i is input power.

A. Design Process

In designing of the power amplifier, consideration was put into some specifications. Like for GSM transmission the Frequency range is in between 935-960 MHz Power consumption of the circuit is around 1 Watt. A load of 50 Ω is modelled as a RLC tank. Normally the load is a transmitting antenna. CMOS technology is used for developing the circuit. Fig. 3 represents the power amplifier design process. In this process first the optimum R_{LOAD} is determined then all the devices were selected accordingly. Then the network is selected for which the simulation takes place. If the output doesn't meet the desirable requirements, necessary changes are made in device selection. The other stapes will be followed at the end and all the parameters for the power amplifier circuit are decided.

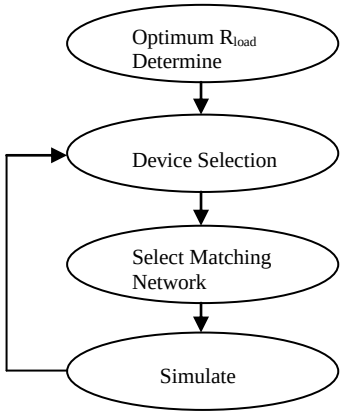

Figure 3. The power amplifier design process

Circuit Diagram

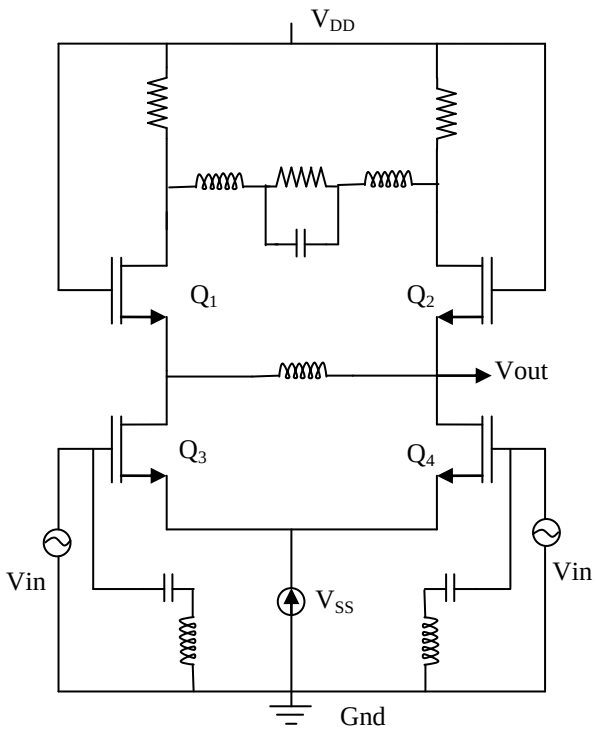

Figure 4. Circuit design used for implementation of power amplifier

The circuit diagram of Class-C PA is shown in fig. 4. In this circuit four FET are used named as Q_1, Q2, Q3 and Q_4. Same input (Vin) is given to Q_3 and Q_4 then output (Vout) is taken from the shorted drain and source terminal of Q_4 and Q_2 respectively. Here a constant current source (Vss) is provided to the source terminal of the transistors Q_3 and Q_4 and the transistors Q1 and Q2 are forced to be in saturation. The output is given to the antenna which behaves as a load for the circuit.

Since silicon MOS is a poor current drive technology, we can optimize the performance of the circuit either by increasing the amplitude of the input signal or by increasing the device size. The second option is limited by the fact that the PA must be integrated on the transceiver chip. We can therefore boost the output current by having the amplitude of the input signal amplified by previous stages. This can lead to increased power consumption by the pre-amplification stage. To have greater output with the same input, a differential structure is recommended. In a differential structure, two transistors are used, with their sources connected and feeding to a tail current source. The drain of each transistor is loaded with equal load impedance. The transistors are driven with a signal which consists of a common mode signal and a differential mode signal. The differential configuration leads to higher efficiency. The configuration is immune to common-mode signals and prevents any noise from the power supply. The voltage swing is doubled at the output, leading to greater gain. This leads to use of smaller devices. The differential configuration also gives the frequency of substrate injection.

The cascade structure enhances the small signal output resistance. It also reduces the impact of Miller capacitance, by reducing the gain across the feedback capacitor of the MOS device. The cascade structure also helps to insulate the output node from the input node, which in turn reduces the system noise.

III. SIMULATION & RESULTS

The above circuit is simulated for three different frequencies such as 935 MHz, 947 MHz and 960 MHz to ensure fully desired operability. A plot of the input and output (I/O) signal frequencies are shown after running a transient analysis. Fig. 4, Fig. 5, and Fig. 6 show these plots of simulations run at 935 MHz, 947 MHz, and 960 MHz respectively. All these figures show the desired output frequency. Proving that the output frequency is almost same as the input frequency assures that the output circuitry is conjugately matched to achieve resonance, and essentially deliver maximum driving power across the load. The period of the output waveform is measured from peak to peak values using markers. The output frequency can be found by calculation as time period is inversely proportional to frequency. The results of the simulation are shown in Table 1.

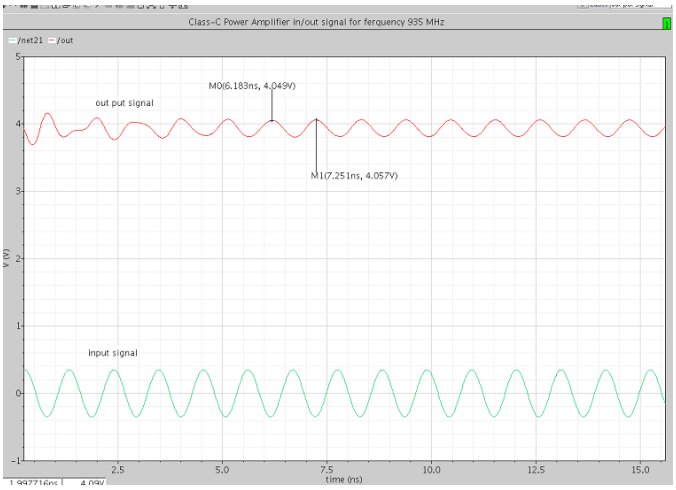

Figure 5. I/O response for simulation at 935MHz

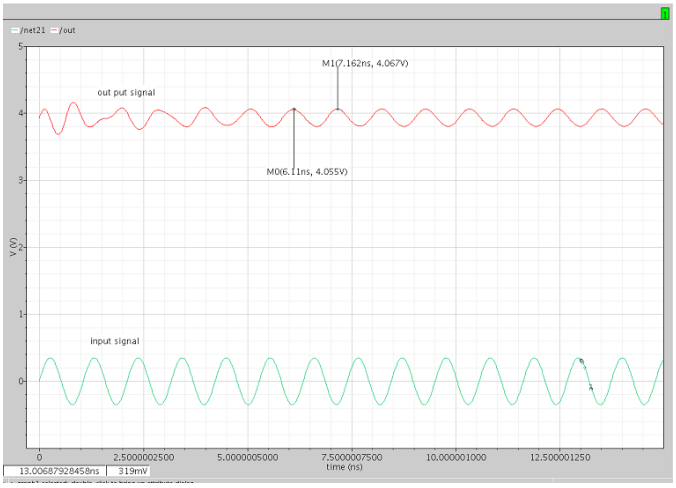

Figure 6. I/O response for simulation at 947MHz

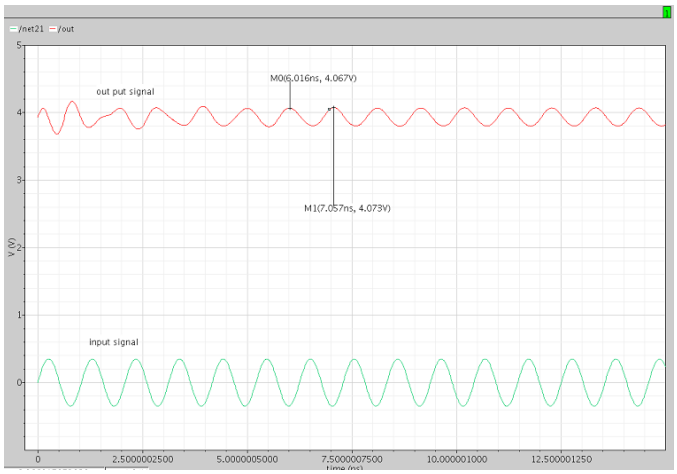

Figure 7. I/O response for simulation at 960MHz

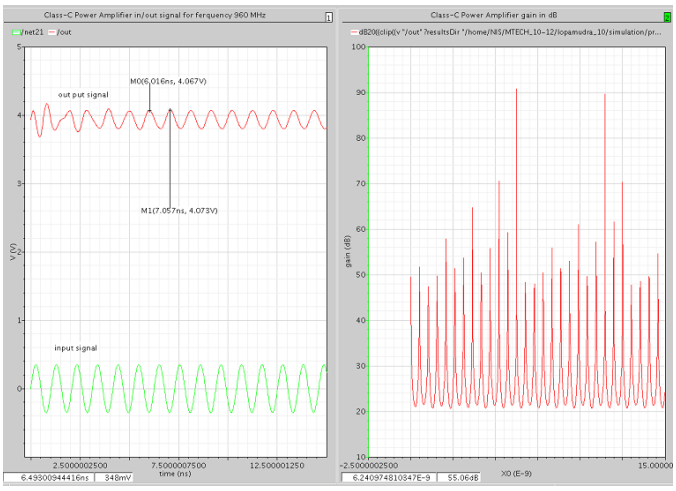

Figure 8. Gain calculation of power amplifier

A. *Observation*

The above circuit is created using the Cadence software with simulations run in the analog environment. The frequency band of interest stretches from 935 MHz to 960 MHz, as standard with GSM communication. Three simulations are performed at 935 MHz, 947 MHz, and 960 MHz to ensure fully desired operability. A plot of the I/O signal frequencies are shown after running a transient analysis. Fig. 5, Fig. 6, and Fig. 7 show these plots of simulations run at 935 MHz, 947 MHz, and 960 MHz, respectively. In all the simulated output figures the desired output frequencies are obtained. Proving that this frequency is same as the input frequency assures that the output circuitry is conjugately matches to achieve resonance, and essentially delivers maximum driving power across the load. The period of the output waveform is measured from peak to peak values using markers. The output frequency can then be found. Table-1 shows these results.

Table-1

Simulation frequency(MHz)	Period at Load, T (ns)	Frequency at Load, 1/T(MHz)
935	1.068	936.33
947	1.052	950.5
960	1.041	960.61

The achieved gain is derived from the waveforms of Fig. 8. The signal being injected into the power amplifier has amplitude of 350mV. Consistently at all frequencies the signal amplitude at the load is measured approximately at 4V. The following equation allows the gain in dB to be calculated with the given information. Therefore, the achievable gain of the power amplifier is 23.15dB. On average this value should range from 20dB to 30dB.

$$Gain = 20 \times \log\left(\frac{V_{OUT}}{V_{IN}}\right) dB \qquad (10)$$

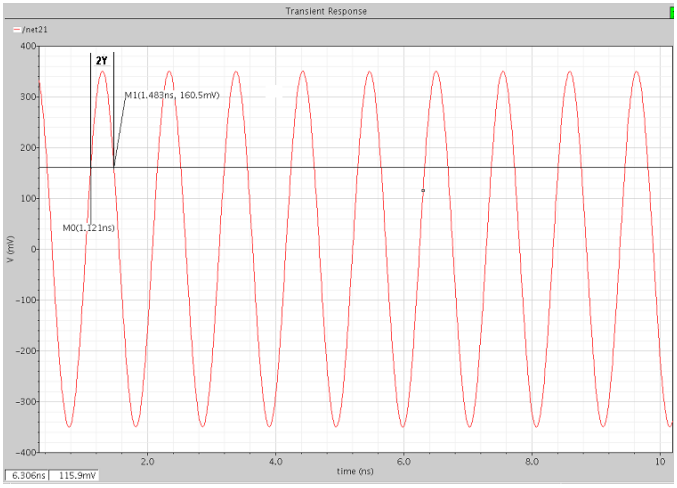

Figure 9. Efficiency measured by conducting state (arbitrary plot)

The efficiency of the PA is very important in wireless communication systems, mainly when they are employed in mobile devices. In this case, higher efficiency means longer battery lifetime which translates directly into user comfort. For nonportable applications, efficiency is also important as heat dissipation is often an issue. Power added efficiency is calculated to measure the performance Class-C PA. This value is determined from the derived efficiency from the conducting state of the input transistors, M2 and M4. This method was chosen because of the visible degraded linearity present in the output signal waveforms of Fig. 5, Fig. 6, and Fig. 7 from the changing conducting state. It was of interest to see the correlation between these apparent nonlinearities and the effect on efficiency. Fig. 9 compares the input signal waveform relative to the threshold voltage of the transistors. When the input voltage is greater than threshold the transistor is in a conducting state. For any period this time that the previous holds true is referred to as 2Y. The following equation can determine efficiency (η).

$$\eta = \frac{2Y - \sin 2Y}{4(\sin Y - Y\cos Y)} \qquad (11)$$

The efficiency using the above procedure is found to be 50%. On average, the class-C amplifier is able to achieve anywhere from 50% to 85% efficiency.

IV. CONCLUSION

A Class-C power amplifier circuit design is simulated and verified in 90nm CMOS technology (cadence environment). The efficiency is calculated to be 50% and gain is 23.15 dB. Normally the efficiency of the Class-C power amplifier varies from 50% to 85% and the gain varies between 20dB to 30dB. On sizing the transistor the gain and efficiency will increase. The input and output frequency of the Class-C power amplifier is almost same in the simulated circuit which is desirable. This efficiency would have significantly increased. As well as, a higher measure of linearity would have been apparent in simulation. Another area of improvement would be to add another stage of amplification for better results. This circuit can be used in GSM applications and some other applications like FM radio transmission.

References

[1] Ramakrishna Sekhar Narayanaswami, "RF CMOS class-C power amplifier for wireless communications," *PhD Dissertation*, UCB, 2001

[2] Marian k. Kazimierczuk, "RF power amplifiers," *A John Wiley and Sons*, Ltd., Publication, 2008

[3] R. Sekhar Naraynaswami, "RF CMOS class power amplifiers for wireless communications presentation," University of California, 1998.

[4] R. Gupta and D. Allstot, "Parasitic aware design and optimization of CMOS RF integrated circuits," *IEEE RFIC Symposium*, pp. 325-328, June 1998.

[5] Thomas Lee, "The design of CMOS radio-frequency integrated circuits," 2004

[6] B. Razavi, "RF micro-electronics," *Prentice Hall*, 1998.

[7] Thomas H. Lee, "The design of radio-frequency integrated circuits," 2nd edition, Cambridge University Press, 2004.

[8] Christian Fager, José Carlos Pedro, Nuno Borges de Carvalho, Herbert Zirath, Fernando Fortes, and Maria João Rosário, "A comprehensive analysis of IMD behavior in RF CMOS power amplifiers," *IEEE journal of solid-state circuits*, vol. 39, no. 1, January 2004.

[9] Nuno Borges de Carvalho and Jos´e Carlos Pedro, "Large-and small-signal IMD behavior of microwave power amplifiers," *IEEE transactions on microwave theory and techniques*, vol. 47, no. 12, December 1999.

[10] Sanghoon Kang, Byounggi Choi, and Bumman Kim, "Linearity analysis of CMOS for RF application," *IEEE transactions on microwave theory and techniques*, vol. 51, no. 3, March 2003.

[11] Jongchan Kang, Jehyung Yoon, Kyoungjoon Min, Daekyu Yu, Joongjin Nam, Youngoo Yang, and Bumman Kim, "A highly linear and efficient differential CMOS power amplifier with harmonic control," *IEEE journal of solid-state circuits*, vol. 41, No. 6, June 2006