A Low Power Circuit Technique for Feedthrough Logic

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Abstract—**This paper presents the design of a low power dynamic circuit using a new CMOS domino logic family called feedthrough logic. The proposed circuit has very low dynamic power consumption compared to the recently proposed circuit techniques for the dynamic logic styles. The proposed circuit has been simulated at 0.18 µm, 1.8 V CMOS process technology. Intensive simulation results in Cadence environment shows that the dynamic power reduces approximately by 40% for 10-stage of inverters and 4-bit ripple carry adder in comparison to existing feedthrough logic. The problem of requirement of output inverter and non- inverting logic are also completely eliminated in the proposed design.**

***Keywords*—CMOS logic circuits, feedthrough logic (FTL), low-power, adder.**

I. INTRODUCTION

Dynamic logic circuits as compared to static CMOS [1,2] offer more advantages in terms of speed and area but the major drawback with this logic is its excessive power dissipation due to the switching activity and clock; furthermore, it suffers from charge redistribution and requirement of an additional output inverter. In order to reduce excessive power dissipation of dynamic logic circuit, various techniques like dual supply voltages [3] and dual threshold voltage (V_T) [4] have been proposed in the literature.

To improve the power consumption of dynamic logic circuit with a very long logic depth further, a new logic family called feedthrough logic (FTL) is proposed in [5], where FTL concept is extended for the design of low power arithmetic circuits.

The dynamic power dissipated in a generic CMOS digital gate is given by [6]

$$P_{dynamic} = V_{dd} F_{clk} \sum_{i} V_{i\ swing} C_{i\ load} \alpha_i$$

Where V_{DD} is the supply voltage, F_{clk} denotes the system clock frequency, $V_{i\ swing}$ is the voltage swing at node i, $C_{i\ load}$ is the load capacitance at node i, α_i the activity factor at node i.

The rest of this section is organized as follows. The operation of existing HS0 is described in section II. Section III presents the design of novel circuit for low power. Simulation results and comparisons are discussed in section IV. Section V concludes with some final remarks and comments.

II. CONVENTIONAL HIGH SPEED STRUCTURE (HS0)

The high speed structure (HS0) in [5] is shown in Fig. 1. It consists of an NMOS reset transistor (M2) and a pull up PMOS load transistor (M1). M1 and M2 are controlled by the clock signal (CLK). The basic principle of operation is briefly described here. During CLK =1 (reset phase), the output node (OUT) is pulled to ground through M2. When CLK =0 (evaluation phase), M2 is turned off and M1 conducts. The output node is preconditioned to a voltage value V_{TH} between V_{OH} and V_{OL}, thus doing a partial evaluation before IN is valid. If the IN=0, the output node is pulled towards V_{DD} otherwise it remains at low. Since the output is reset to low, the inverter requirement is eliminated for cascading these blocks. This logic is faster because the output makes transition from V_{TH} to V_{OH} or V_{OL} only [5], but it suffers from more power consumption due to the fact that V_{OL} is not 0 V.

III. PROPOSED CIRCUIT

The proposed novel circuit for low power is shown in Fig. 2. It consists of an additional PMOS transistor (M4) in series with M1. The transistor M4 helps in reduction of V_{OL} as compared to HS0 in [5]. The voltage that appears at the source of M4 is less than that of V_{DD} The series combination of M1 and M4 increases the total resistance in the path from V_{DD} to OUT, as a result V_{OL} reduces. This reduction in V_{OL} helps in reducing the dynamic power consumption and facilitates the improvement in noise margin.

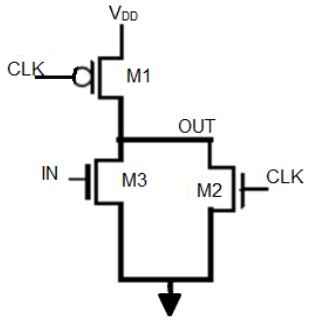

Fig.1 HS0 Structure in [5]

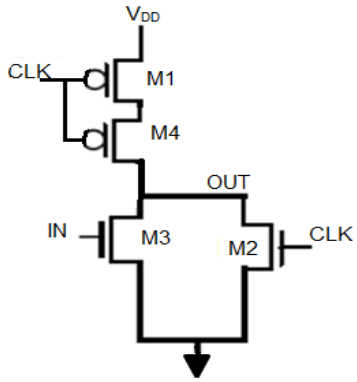

FIG. 2 PROPOSED HS0

IV. SIMULATION RESULTS AND COMPARISONS

We have used 0.18 µm CMOS process technology model library from UMC, using the parameter for typical process corner at 25^0C. Power supply V_{DD} is constant for all simulations and is equal to 1.8 V. Circuits are simulated in HSPICE simulator. To compare the proposed structure against the existing HS0 structure in [5], the behaviour of a long chain of inverter and 4-bit ripple carry adder are simulated. The values of dynamic power for a 10 stages of inverter with 10 fF capacitive loads in all output nodes are shown in Table II. It also shows the dynamic power comparison of 10-stage inverter in [5] and the proposed structure.

A full adder cell is designed by using the proposed HS0 structure. Table III. shows the dynamic power comparison for a 4-bit ripple carry adder designed by proposed logic and the existing structure in [5].

Fig. 3. shows the plot of output voltage from the 1st stage of inverter to the 10th stage of inverter at 10 fF capacitive loads. The output voltage falls to a lower voltage V_{OL} which is less than the V_{OL} in [5].

Table I. Simulation results for dynamic power for the proposed HS0 in Fig. 2 and the existing HS0 in [5]

Logic family	Power(µW)
HS0 in [5]	28.2
Proposed HS0	16.8

TABLE II. SIMULATION RESULTS FOR DYNAMIC POWER FOR THE PROPOSED CIRCUIT AND THE EXISTING HS0 STRUCTURE IN [5]. (10-INVERTER)

Logic family	Power(µW)
HS0 in [5]	268
Proposed HS0	151

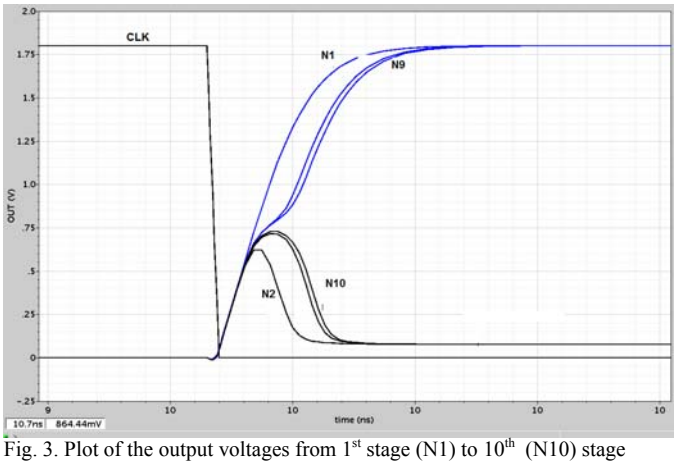

Fig. 3. Plot of the output voltages from 1st stage (N1) to 10th (N10) stage of inverters.

TABLE III. SIMULATION RESULTS FOR DYNAMIC POWER FOR AN 4-BIT RIPPLE CARRY ADDER DESIGNED BY PROPOSED CIRCUIT AND THE EXISTING HS0 STRUCTURE IN [5]

Logic family	Power(µW)
HS0 in [5]	306
Proposed HS0	167

V. CONCLUSIONS

In this paper, we proposed a novel low power dynamic circuit. The proposed circuit is simulated in 0.18 µm CMOS process technology from UMC. The proposed circuit when compared with the recently proposed FTL scheme has 40% less dynamic power consumption. The simulation for a 4-bit ripple carry adder is also carried out in this work. The proposed circuit can be used for design of a low power processor where power consumption is of primary importance.

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