Design of CMOS Ring Oscillator Using CMODE

Prakash Kumar Rout, Debiprasad Priyabrata Acharya
Department of Electronics and Communication Engineering
National Institute of Technology, Rourkela, Orissa, India

Abstract— **The design of optimal analog and mixed signal (AMS) very large scale integrated circuits (VLSI) with lesser design cycle time is a challenging task for the integrated circuit (IC) designers. Voltage Controlled Oscillator (VCO) is a radio frequency integrated circuit (RFIC) having wide range of applications. This paper presents a new approach to design a ring oscillator (RO) with optimum performance with only one design cycle. The optimal figure of merit performance for a RO with a constraint of achieving a desired centre frequency is observed using a new technique which combines multi-objective optimization with differential evolution (CMODE). The RO is designed by considering the design parameters extracted from constrained CMODE in Cadence Virtuoso analog design environment (ADE) using gpdk090 library. The simulation results are compared with the CMODE predicted indices and are observed to be in good agreement with it. In this work RO circuits with 9 stages of inverters are considered to be designed for 2 GHz centre frequency with the limitations imposed by gpdk090 library. Results of exhaustive simulation and experimental studies for these ROs are presented here to verify the reduced design cycle time and superior performance offered by the proposed design methodology.**

Index Terms: **Analog and mixed signal (AMS) VLSI circuit, CMOS Ring oscillator (RO), Combining Multi-objective Optimization with Differential Evolution (CMODE).**

I. INTRODUCTION

CMOS Ring Oscillator (RO) is an integral part of phase locked loops (PLL).The increasing demand for bandwidth, places stringent requirements on the spectral purity of oscillators..These oscillators due to their integral nature are used in many applications such as integral frequency synthesis [1, 2], clock and data recovery in communication systems [3] and on chip clock distribution [4]. The design of an efficient RO circuit operating at radio frequencies with optimal performance is quite challenging for an RFIC designer. The performance of a RO is characterized by a number of performance measures such as operating frequency, figure of merit, tuning range and area. These performance indices are guiding measures for designers to size the transistors and bias the circuit. In the semiconductor industry an analog IC designer puts lots of manual efforts to perform circuit sizing for a particular circuit to meet the required specifications.

After many design cycles even if the circuit performance improves it is not guaranteed that the designed circuit will yield the optimal performance. To overcome such problem geometric programming [5], evolutionary algorithms [6,7, 8] have been proposed for automatically giving the circuit metrics for design. Practically the evolutionary algorithms like Genetic Algorithm (GA) [9], Particle Swarm Optimization (PSO) [10] can be used to determine the design parameters of all transistors in the RO for achieving the single objective of minimizing either phase noise or power consumption. These algorithms are incapable of attaining the optimization of multiple objective functions all at a time. To the best of our knowledge the consideration of both phase noise and power consumption simultaneously to obtain a desired frequency of the RO with the technological feature size constraint has not been reported in literature. Also a more practical model of power consumption for a RO and its design in accordance with that is not available.

The RO design problem we considered in this paper is to determine the values of the design parameters that optimize the objective measure while satisfying different constraints. Combining Multi-objective Optimization with Differential Evolution (CMODE) [11] is an efficient optimization technique which is applied here to optimize the FOM of the ring oscillator (RO) circuit with the frequency of oscillation of ring oscillator being constrained to suffer minimum deviation from the desired frequency. The optimization problem is mainly focused on the sizing of the transistors in the circuit to meet the targeted oscillation frequency with optimization in terms of power consumption and phase noise within the process constraints. CMODE technique is used to achieve the targeted 2 GHz frequency of oscillation with design parameters constrained by CMOS process technology library gpdk090. A case of nine stage RO circuit is considered here for the design and validation of the newly proposed technique.
The remaining part of the paper is organized as follows. The next section of the paper describes about the CMODE. Section III of this paper elaborates our problem formulation for optimal design of the RO circuit. In section IV the design and synthesis environment of the RO has been outlined. The results of different case studies are analyzed in section V. Finally the finding of the study has been concluded in section VI.

II. COMBINING MULTI-OBJECTIVE OPTIMIZATION WITH DIFFERENTIAL EVOLUTION (CMODE)

Z. Cai and Y. Wang have recently proposed a method known as CMODE [11] which combines multi-objective optimization with differential evolution to deal with constrained optimization problems. The algorithm takes

population size (Np), number of candidates/agents to take part in DE operation (λ), the generation gap for implementing the infeasible solution replacement mechanism (k) and maximum number of function evaluations (Max_FES) as the inputs and produces the best solution of the final population ($\vec{x}^*$) as the output.

The CMODE algorithm is briefly outlined as follows.

1. Initialization

- An initial population of size N_P can be randomly generated from the decision space S.

$P_{(t)}=\{\vec{x}_1, \vec{x}_2, ..., \vec{x}_{Np}\}$ where t denotes the generation number.

- The f and G value of each candidate in initial population can be calculated.

Objective function values of the candidates are $f(\vec{x}_1), f(\vec{x}_2), ...f(\vec{x}_{Np})$ and their degree of constraint violations are $G(\vec{x}_1), G(\vec{x}_2), ...G(\vec{x}_{Np})$.

- Set FES(Number of function evaluations)=N_p
- Set A(Archive which is used to store the infeasible candidate which has lowest degree of constraint violation)=Φ
- Initialize t(Generation number) to 1

2. Population evolution model

- Randomly choose λ candidates from population $P_{(t)}$ as set Q
- Now $P_{(t)}= P_{(t)}- Q$
- By using mutation and crossover techniques in DE explained earlier an offspring is created from each candidate in Q. So λ offspring (set C) can be produced.
- The f and G value of each candidate in C are to be evaluated.
- Now FES gets updated to $FES+ \lambda$.
- Make a set R consisting of identified non dominated candidates from C.
- Assume there exists m non dominated candidates denoted as $\vec{x}_1, \vec{x}_2, ..., \vec{x}_m$
- Consider there are n candidates in Q dominated by $\vec{x}_1$. *If* $n \geq 1$, then one of the dominated candidates chosen at random can be replaced by $\vec{x}_1$
- Now the remaining non dominated candidates of R can continue the same process for the updated Q progressively.
- $P_{(t)}= P_{(t)} U Q$

After combining the updated Q with $P(t)$, the update of $P(t)$ is also achieved.

3. Archiving infeasible solution and replacement

- If R does not have any feasible solution, then $A = A\ U\ \vec{x}'$ Where $\vec{x}'$ is the infeasible individual with the lowest degree of constraint violation in R.
- If $mod(t,k) = 0$, then the infeasible solution replacement mechanism can be executed and $A = \Phi$.

Every k generations, all of the infeasible candidates in A are used to replace the same number of individuals in $P(t)$.

4. Now set $t = t + 1$

Stopping criterion: If $FES \geq Max\_FES$ is satisfied then the process will be stopped and the best solution $\vec{x}^*$ in $P_{(t)}$ will be the output. Otherwise the process will restart from step 2.

The CMODE algorithm is selected to get the design parameters for a nine stage ring oscillator having with the FOM to be optimized with the center frequency being constrained to remain as close to 2 GHz as possible with the restriction of minimum feature size of the transistors dictated by the fabrication process.

III. PROBLEM FORMULATION FOR CMOS RING OSCILLATOR CIRCUIT

The CMOS ring oscillator circuit consists of a series of CMOS inverters connected in a closed loop as shown in the Figure 1. There has to be an odd number of inverter stages connected for generation of proper oscillations. Figure 2 depicts a transistor level diagram of a CMOS inverter used in each stage of RO.

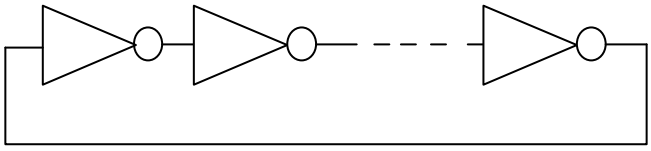

Figure 1.Simplified structure of a ring oscillator

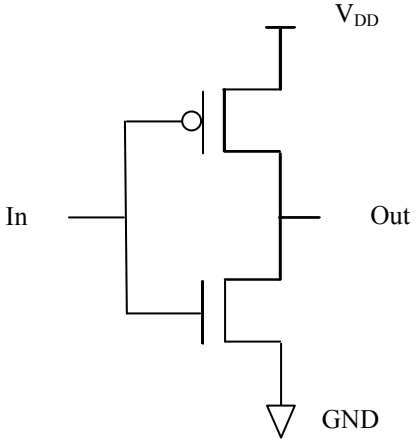

Figure 2. The CMOS Inverter Schematic used as a stage of ring oscillator

The oscillating frequency f_{osc}mainly depends on the current flowing through the transistors of the inverter stages which in turn depends on the aspect ratio of the devices [12]. More precisely $f_{osc}$is given by

$$f_{osc} = \frac{1}{\eta * N * (t_r + t_f)} = \frac{I_D}{\eta * N * C_{tot} * V_{DD}} \quad (2)$$

Where I_D is the current flowing through the transistors in the inverter stages, N is the number of stages, C_{tot} is the total capacitance, V_{DD} is the supply voltage, t_r is the rise time, t_f

is the fall time and η is a characteristic constant which varies between 0.7 to 0.9 for CMOS ROs of different stages.

The total capacitance C_{tot} is given by

$$C_{tot} = \frac{5}{2} C_{ox}(L_p W_p + L_n W_n) \quad (3)$$

where C_{ox} is the oxide capacitance per unit area, L_p, L_n are length of the PMOS and NMOS devices respectively and W_p, W_n are width of the PMOS and NMOS devices respectively.

In a ring oscillator CMOS inverters are the circuit blocks which consume power. The total power dissipated is attributed to static and dynamic components where static part is purely due to leakage current which is very much negligible. The dynamic power dissipation is due to the short circuit or crowbar current and the switching current. Taking the crowbar current and charging and discharging of each node to a maximum value of q_{max}into account, the average power dissipation [15] in a N stage oscillator circuit is given by

$$P_{avg} = \eta V_{DD} I_{avg} = \eta N V_{DD} q_{max} f_{osc} \quad (4)$$

Where $q_{max} = C_{tot} * V_{DD}$ (5)

$$I_{avg} = N C_{tot} V_{DD} f_{osc} \quad (6)$$

Phase noise is a continuous stochastic process indicating random accelerations and decelerations in phase as an oscillator orbits at a nominally constant frequency in steady state. The contributions to phase noise mainly come from white noise, control voltage noise and flicker noise [15].

The expression for total phase noise [15] of the circuit is

$$\mathcal{L}\{\Delta f\} = \frac{8}{3\eta} \frac{kT}{P_{avg}} \frac{V_{DD}}{V_{char}} \frac{f_{osc}^2}{\Delta f^2} \quad (7)$$

where $V_{char} = {}^{\Delta V}/_{\gamma}$ (8)

Δf is the offset frequency from the carrier at which the phase noise is measured, ΔV is the gate over drive voltage, k is Boltzmann Constant, T is absolute temperature and γ is a coefficient which is 2/3 for long channel devices in saturation [15].

The figure of merit FOM is a quality performance measure of a ring oscillator which has been proposed in [16] and is defined as follows

$$FOM = 10\, log_{10}\left[\mathcal{L}\{\Delta f\} \frac{\Delta f^2}{f_{osc}^2} \frac{P_{avg}}{1\, mW}\right] \quad (9)$$

The model equations described above are used in the CMODE technique to find out the design parameters of CMOS ring oscillator circuit bestowed with optimal FOM to achieve a frequency of oscillation as close to 2 GHz as possible. CMODE yields width and length of the transistors of CMOS inverter in the RO which corresponds to the minimal FOM that in turn optimal tradeoff of phase noise and power consumption. The optimization problem can be precisely described as,

$$\left.\begin{array}{ll} minimize & FOM \\ & f_{osc} = 2\ GHz \\ subject\ to & W_{min} < W < W_{max} \\ & L_{min} < L < L_{max} \end{array}\right\} \quad (12)$$

Where the FOM is given by equation (9) and W_{min}, L_{min}, W_{max} and L_{max} are the minimum and maximum values of width and length of transistors respectively. The minimum values are fixed by the CMOS gpdk090 process library and the maximum value is provided by the designer keeping in view of the performance parameters of the ring oscillators. This limits the search space of the algorithm thereby providing the feasible design parameters for optimal performance.

IV. DESIGN AND SYNTHESIS ENVIRONMENT OF CMOS RO

The CMODE algorithm is selected to get the design parameters for a ring oscillator having a single objective of figure of merit to be optimized with the centre frequency being constrained to remain as close to 2 GHz as possible. CMODE algorithm for the CMOS RO problem is written in MATLAB where the figure of merit is the objective function as described in (10). In the algorithm the frequency of oscillations is constrained to remain within a specified limit. The W and L of the transistors are also restricted within minimum and maximum values. The minimum value is decided by the minimum feature size of CMOS gpdk090 process library. In this work three different sets of values of parameters for nine stage ring oscillator are considered as three cases for design.

From the dimensions of NMOS the aspect ratio of the PMOS is obtained by assuming $\mu_n W_n = \mu_p W_p$ to make the waveforms symmetric to the first order. The length of both PMOS and NMOS devices are considered to be equal, i.e. $L_n = L_p = L$.

The design entry of the circuits is carried out in the schematic editor of CADENCE Virtuoso Analog Design Environment using gpdk090 library. For performance analysis these circuits are simulated in the Spectre simulator of CADENCE tool. The transistor sizes obtained as above for a set of specifications are used to design the required RO circuit. The first RO is designed for nine stages of CMOS inverters. Three sets of design parameters for optimal 9-stage CMOS RO obtained from constrained CMODE are considered for design and synthesis so as to verify the effectiveness of the proposed technique.

V. ANALYSIS OF RESULTS

Out of many optimal solutions obtained from the constrained CMODE for 9 stage CMOS RO three sets are considered for the design, synthesis and verification.

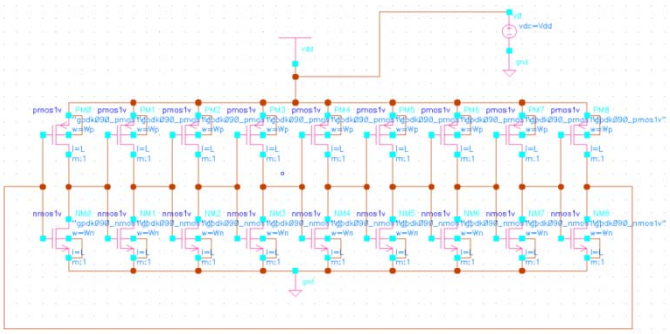

Figure 3: Schematic diagram of 9 stage Ring Oscillator

The values of design parameters i.e W_n W_p and L of both NMOS and PMOS transistors obtained from CMODE for each set are presented in table 1. The FOMs of the RO predicted by constrained CMODE are the optimal tradeoffs of the phase noise at 1 MHz offset frequency and power consumption. The predicted FOMs by CMODE and experimentally measured FOMs obtained from simulations using Cadence Virtuoso Analog Design Environment (ADE) are found out to be in very good agreement with each other which is clearly justified by the negligibly small difference between them as enumerated in table 1.The desired frequency of oscillation of the RO which was set as a constraint for CMODE was 2 GHz. The frequencies of oscillation observed from simulations in Cadence Virtuoso ADE are 2.00004618 GHz , 2.00123123 GHz and 2.00137624 GHz for set-I , set-II and set-III respectively which are very close to the desired frequency of oscillation and which establishes the better constraint handling capability of CMODE . The predicted and observed values of FOMs, synthesized frequencies and their differences are listed in table 1. The direct phase noise and power consumption measurements from CADENCE tool for the respective sets are depicted in figures 5 and 6 respectively. The traditional hit and trial method of design rarely attains such precision in frequency with the optimal figure of merit that in turn optimal phase noise and optimal power consumption. Such a high precision with optimal performance is achieved due to application of CMODE which performs a global optimization in the constrained environment.

Table 1: Design Parameters and performance of a five stage ring oscillator

(9-Stage RO , Center Frequency-2 GHz)								
Design Set	Predicted by CMODE				Measured using CADENCE Virtuoso ADE		Difference	
	W_n (nm)	W_p (nm)	L (nm)	Figure of Merit	Frequency (GHz)	Figure of Merit	Frequency (GHz)	Figure of Merit
I	223.654	372.756	173.638	-162.9059	2.00004618	-162.8113	0.00004618	-0.0946
II	200.260	333.766	173.602	-162.9019	2.00123123	-162.7923	0.00123123	-0.1096
III	187.748	312.913	173.618	-162.9035	2.00137624	-162.7939	0.00137624	-0.1096

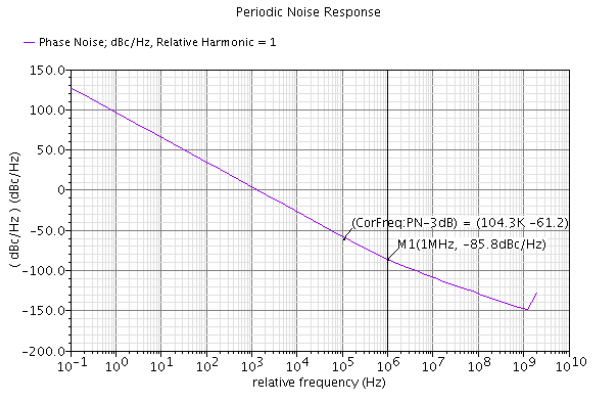

Figure 4: The Phase Noise measurement for set-I of 9-stage RO

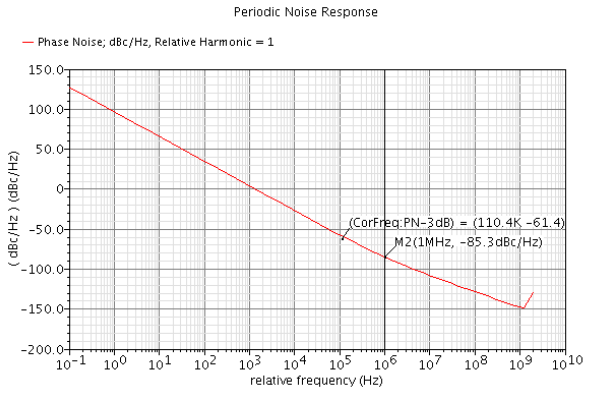

Figure 5: The Phase Noise measurement for set-II of 9-stage RO

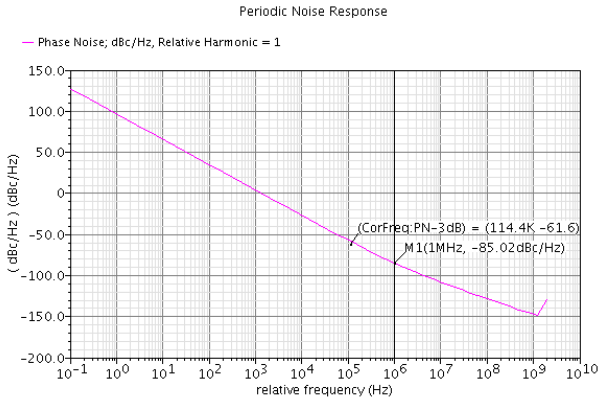

Figure 6: The Phase Noise measurement for set-III of 9-stage RO

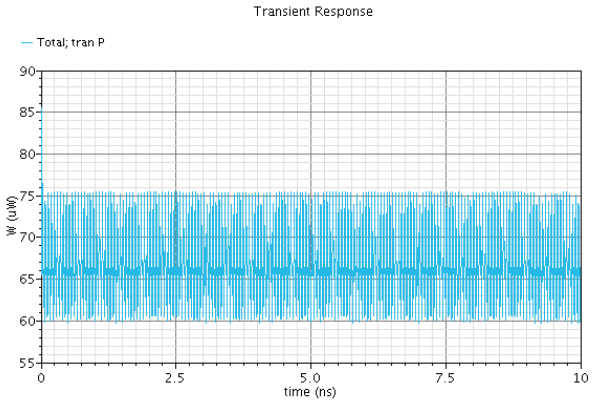

Figure 7: The Power measurement for set-I of 9-stage RO

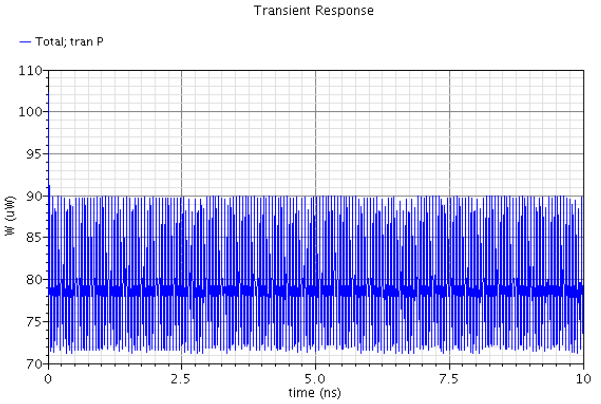

Figure 8: The Power measurement for set-II of 9-stage RO

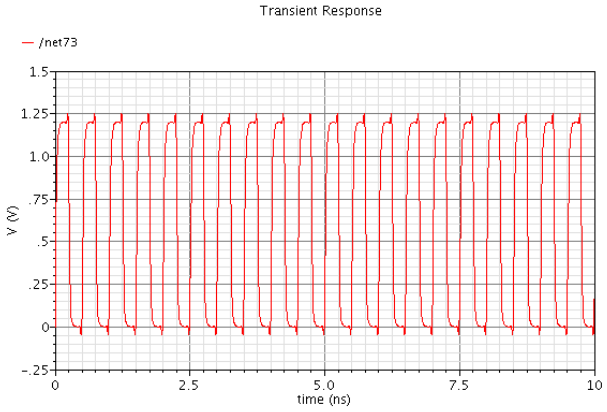

Figure 10: The Waveform for set-I of 9-stage RO

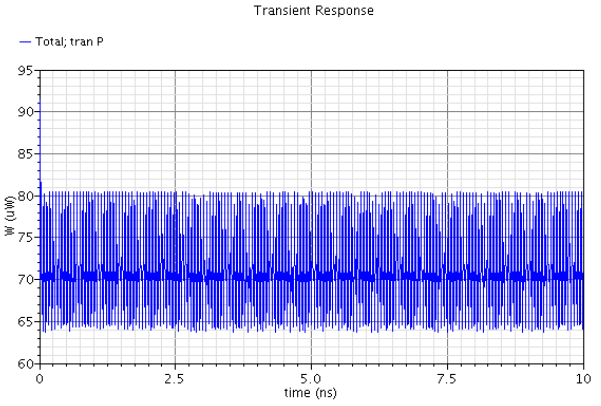

Figure 9: The Power measurement for set-III of 9-stage RO

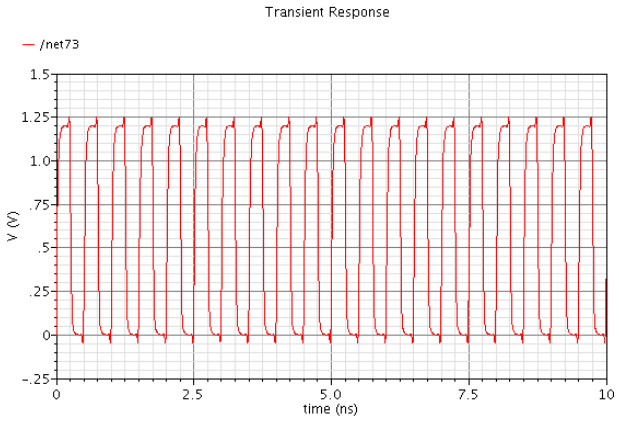

Figure 11: The Waveform for set-II of 9-stage RO

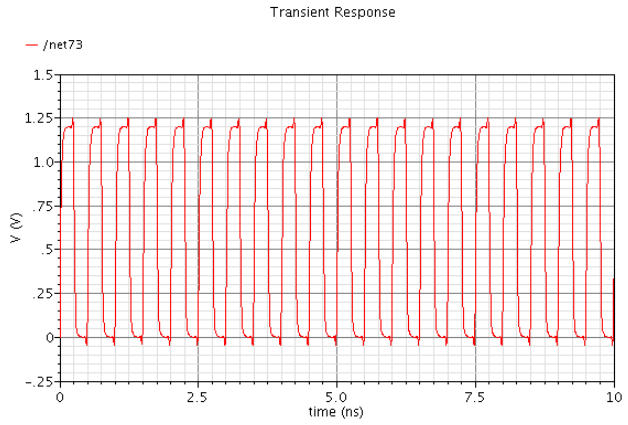

Figure 12: The Waveform for set-III of 9-stage RO

VI. CONCLUSION

The use of CMODE for design of CMOS ring oscillator in the constrained environment is presented here. The design parameters for each case found from the technique are used in the CADENCE Virtuoso analog design environment for circuit behavior simulation and synthesis. The RO performance index FOM is estimated from Virtuoso ADE. The measured values are found to be in very good agreement with the predicted values of FOM. The measured RO frequency is also observed to have very little deviation from the desired frequency of 2 GHz. This finding is verified by extensive simulation measurements for ROs with nine stages and three case studies for this RO. The analog VLSI circuits being a full custom design has wide scope in many levels of optimization. The method would be of great benefit to the designer in industry due to saving of design time which in turn reduces the non recurrent engineering (NRE) cost of the IC.

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