A New Ultra Low-Power and Noise Tolerant Circuit Technique for CMOS Domino Logic

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***Abstract*— Dynamic logic style is used in high performance circuit design because of its fast speed and less transistors requirement as compared to CMOS logic style. But it is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. A small noise at the input of the dynamic logic can change the desired output. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and consuming very less power as compared to other proposed circuit. In this paper we have proposed a novel circuit for domino logic which has less noise at the output node and has very less power-delay product (PDP) as compared to previous reported articles. Low PDP is achieved by using semi-dynamic logic buffer and also reducing leakage current when PDN is not conducting.**

***Keywords*— Dynamic logic, domino logic, Delay, diode-footed domino, noise tolerance, power consumption, robustness, technology scaling, semi-dynamic logic**

INTRODUCTION

The rapid advancement of VLSI circuit is due to the increased use of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled with technology. Due to larger number of devices per chip the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore noise pulses known as cross-talk can be generated leading to logic failure and delay of the circuit [1]. Again, when supply voltage is scaled the threshold voltage of the device needs to be scaled to preserve the circuit performance, which leads to increase in the leakage current of the device.

Due to high speed and low device count especially compared to complementary CMOS, dynamic-logic circuits are used in a wide veriety of applications including microprocessors, digital signal processors and dynamic memory [2]. Dynamic circuit contains a pull-down network (PDN) which realizes the desired logic functions. According to the basic theory, the dynamic logic circuit will precharge at every clock cycle. As the the clock signal frequency is high, the circuit is introduced with a lot of noise which consume extra power and slows the circuit.

In this paper we propose a new circuit technique which can reduce the noise of dynamic logic dramatically. This circuit increases speed and decreases the power dissipation of the circuit as compared to other domino logic styles.

PROBLEM STATEMENT

Figure 1 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging PMOS gets ON and the dynamic node is connected to the VDD and gets precharge to VDD. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period when all the inputs are at logic 0, the dynamic node should be at logic 1. But the wide fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the subthreshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at ant gate input, the keeper may not be able to restore the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent upon V_{GS}. So in the presence of noise impulse the gate voltage increases, which leads to increase in V_{GS} and the dynamic node gets wrongly discharged.

As noise of domino gates is now more important than the area, energy dissipation and delay issues, so recently several techniques have been proposed [6,7] to reduce the noise of dynamic circuits. All the techniques have reduced the noise sensitivity but there are many drawbacks with area, power dissipation and delay.

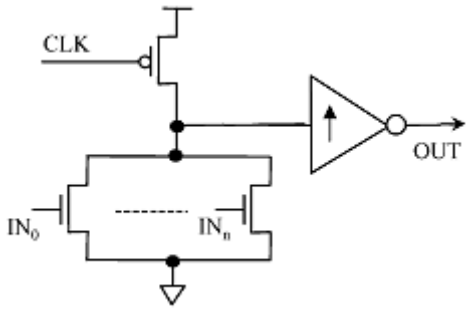

Figure 1. A typical footless Domino OR gate

BACKGROUND AND RELATED WORK

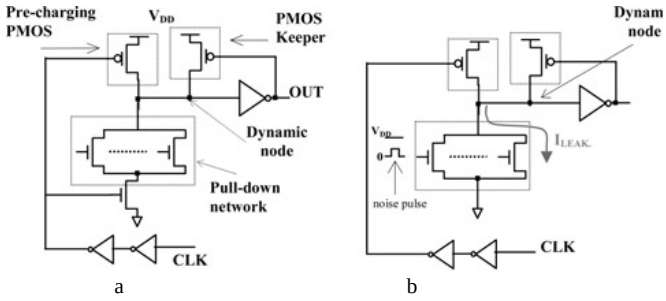

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Figure 2. Standard domino OR gate
a Footed scheme
b Footless scheme

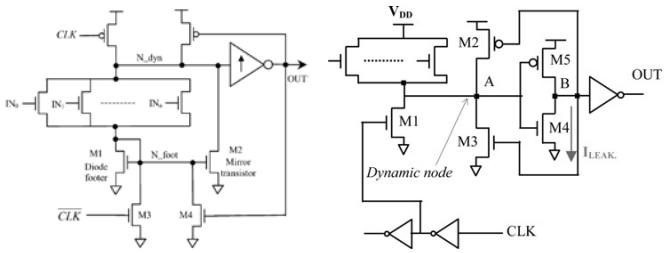

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Figure 3. Previous works showing OR gate
a. Diode footed Domino [6]
b. Domino circuit in scheme [7]

To compensate the leakage current at the dynamic node a week transistor called keeper transistor is used. Keeper transistor prevents the charge loss and keeps the dynamic node at strong high when PDN is OFF. In the first domino proposal [3] the gate of the keeper transistor is tied to ground, therefore the keeper is always on. If at the beginning of evaluation the pull-down network (PDN) turns on, the dynamic node tends to discharge through the PDN. However, the keeper is injecting charge to the dynamic node as it is always on. This is called contention. Furthermore, a potential DC power consumption problem is generated. To alleviate the potential DC power consumption problem a feedback keeper was proposed in Figure. 2a [4, 5].

In [6], this Diode-Footed domino an NMOS transistor is there in a diode configuration i.e. gate and drain terminals connected together in series with the evaluation network, as shown in Figure 3a. A diode connected transistor is exploited in this design in which the leakage flowing through the PDN in the evaluation phase causes the voltage drop across the diode transistor. Which makes the V_{GS} negative and leakage reduces. The performance degradation can be compromised by the mirror network. By varying the size of mirror, noise immunity can be made. But when we compare it with standard footless domino this scheme is very slow. Also the inverse clock increases the capacitive load of the clock driver.

In [7], the circuit based on a pull up network constitutes only the NMOS transistors as depicted in Figure 3b. This style doesn't have precharge PMOS transistors. When the clock is low i.e. at the precharge stage M1 is switched on the dynamic node is pre-charged to 0 V. When clk is high i.e. at evaluation phase M_1 is off and the pull up network conditionally can charge the dynamic node. When one or more input signals are there the dynamic node has to charge up to V_{DD}, but due to the absence of pull up network it only charges to V_{DD}-V_{TH}. This drop is compensated by the PMOS M_2.The noise is decreased by NMOS pull up network also the leakage thru pull up network charge dynamic node. But again it needs an inverting clock which increases the capacitive load. Also it uses extra inverter like structure which increases the area and complexity of circuit.

NOVEL APPROACH

A. Circuit Analysis:-

The proposed novel domino circuit scheme is shown in Figure 4. Transistor M_4 is used as stacking transistor. Due to voltage drop across M_4, gate-to-source voltage of the NMOS transistor in the PDN decreases (stacking effect [10]). The proposed circuit differs from [6] as it has additional evaluation transistor M5 with gate connected to the CLK. In [6], when M_4 has voltage drop due to presence of noise-signals, M_3 starts leaking that causes the circuit to dissipate power and also makes it less noise robust. The purpose of M_5 in proposed scheme causes the stacking effect and makes gate-to-source voltage of M_3 smaller (M_3 less conducting). Hence circuit becomes more noise robust and less leakage power consuming. But for performance degrades because of stacking effect in mirror current path. This can be increased by widening the M_2 (high W/L) to make it more conducting.

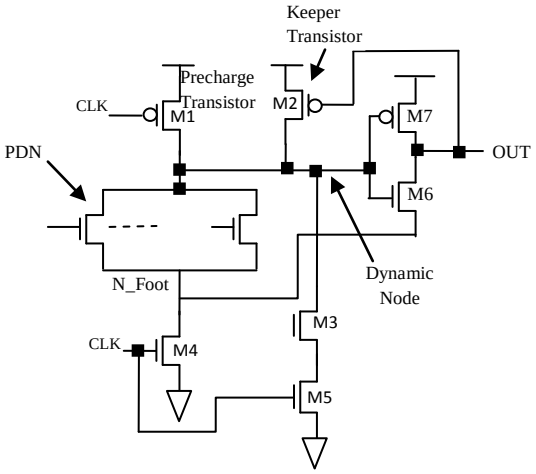

Figure 4. Proposed Circuit

B. Noise Analysis:-

When the PDN is OFF and the N_Dyn is at high voltage and the N_Foot is at low voltage. The high level of dynamic node makes the gate of the NMOS M6 of the buffer V_{DD} and the low level of N_Foot makes the source of the M_6 to 0. This makes M_6 ON and the voltage of buffer output will be same as the voltage of N_Foot. It can be easily verified that if the NMOS transistor of the buffer can always be turned off, the pulses propagating to the output can be avoided [8].

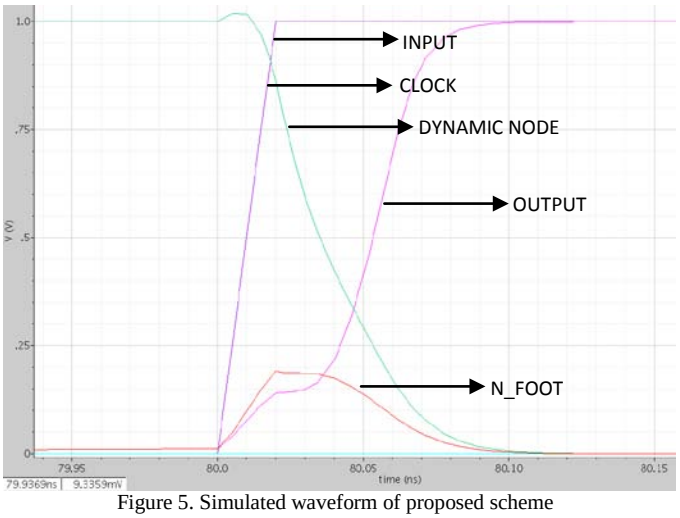

Figure 5. Simulated waveform of proposed scheme

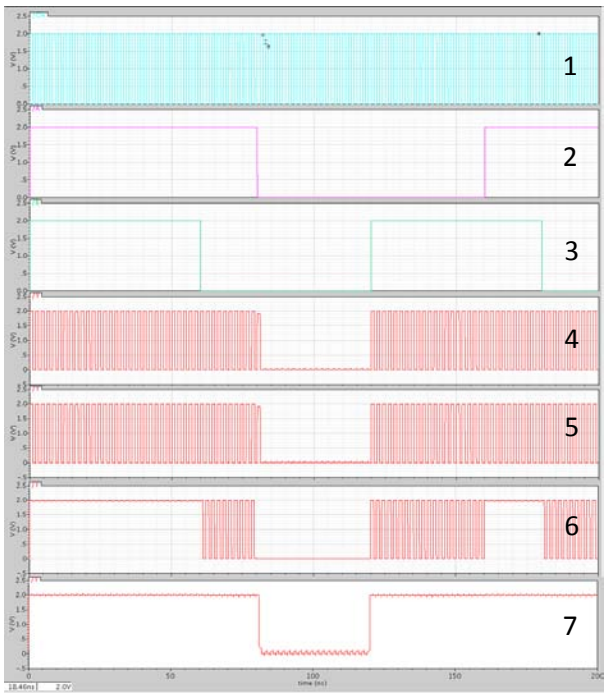

Figure 6. Waveform simulated for the OR gate
1. Clock Input
2. Input A
3. Input B
4. Output for basic circuit
5. Output for [6]
6. Output for [7]
7. Output for Proposed circuit

In the evaluation period, when the NMOS clock transistor M_4 is ON, N_Foot gets discharged to 0. When the PDN is ON the N_Dyn also gets discharged to ground. This makes the V_{GS} of buffer NMOS M_6 to 0 as $V_{GS}=V_G-V_S=0$. This makes the NMOS OFF and the buffer output gets completely charged through PMOS M_7.

During precharge the dynamic node will get charged to high, when the PDN is ON the voltage of the N_Foot is nearly same as N_Dyn, as the NMOS M_4 is OFF. The V_{GS} of the buffer NMOS will be $V_G - V_S < V_{TH}$ which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_Dyn node. This makes the output of buffer LOW.

C. Power Analysis:-

The proposed structure uses the semi-dynamic buffer structure. So the output node OUT has no pulses in the precharge stage as shown in Figure 6. In the figure the 1st waveform shows the clock the second and third wave form shows the inputs of the 2 inputs or gate. The 4th waveform shows the output plotted for the basic domino gate. The 5th and 6th waveform shows the outputs of the two reference circuit structures. The last or the 7th waveform shows the output of the proposed circuit.

It can be seen that the 4, 5 and 6 waveforms contains the pulses in the precharge period, but the proposed output does not contain such pulses, which means the buffer does not get on and off frequently, so the current through the buffer reduced sufficiently then the counterpart.

If there many pulses the buffer gets ON and OFF frequently. The power consumption of the logic circuit in conventional circuit is given by [8]

$$P_{avg\,1} = K.V_{DD}{}^2.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{dyn} \quad (1)$$

In which, $r = T_{on} / (T_{on}+T_{off})$;

T_{on} is the time when input logic is on,
T_{off} is the time when input logic is off.
K is the probability of the state that the input logic change in a unit time.
C_{dyn} is the capacitor in node N_dyn
V_{noise} is the pulse in node N_dyn

Power consumption of the buffer in conventional stage is given by

$$P_{avg\,2} = K.V_{DD}{}^2.(C_{load} + C_{buffer}) + r.f.V_{DD}.V_{noise}.(C_{load} + Cbuffer \quad (2)$$

As $C_{load} \gg C_{buffer}$, equation 2 becomes

$$P_{avg\,2} = K.V_{DD}{}^2.C_{load} + r.f.V_{DD}.V_{noise}.C_{load} \quad (3)$$

$$P_{avg} = K.V_{DD}{}^2.(C_{load} + C_{dyn}) + r.f.V_{DD}.V_{noise}.(C_{load} + C_{dyn}) \quad (4)$$

In the proposed logic the power is given by

$$P_{prop} = K.V_{DD}{}^2.C_{load} + r.f.V_{DD}.V_{noise\_p}.C_{load} \quad (5)$$

So the finally the amount of power which the proposed circuit saves is

$$P_{avg} - P_{prop} = K.V_{DD}{}^2.(C_{load} + C_{dyn}) + r.f.V_{DD}.V_{noise}.(C_{load} + Cdyn - K.VDD2.Cload - r.f.VDD.Vnoise\_p.Cload$$

Power saved due to semidynamic logic is

$$P_{saved} = K.V_{DD}{}^2.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{load} \quad (6)$$

As $V_{noise} \gg V_{nois\,e_p}$

Table: 1 Power delay comparison of the Proposed Circuit with previous reported articles

Supply Voltage in Volt	Parameters	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [6]	Scheme on paper [7]	Proposed Scheme
1	Delay	1.57 E-11	2.40 E-11	4.109 E-8	1.23 E-9	1.04 E-9	3.3 E-11
	Power	3.33 E-5	3.32 E-5	5.6 E-6	4.58 E-5	5.6 E-8	1.42 E-8
0.9	Delay	1.78 E-11	2.69 E-11	4.10 E-8	1.28 E-9	1.05 E-9	3.86 E-11
	Power	2.39 E-5	2.39 E-5	9.6 E-6	3.20 E-5	8.58 E-8	1.56 E-8
0.8	Delay	2.08 E-11	3.13 E-11	4.111 E-8	1.32 E-9	1.06 E-9	4.64 E-11
	Power	1.62 E-5	1.62 E-5	2.8 E-5	2.20 E-5	1.49 E-8	4.80 E-8
0.7	Delay	2.52 E-11	3.82 E-11	4.00 E-8	1.35 E-9	1.09 E-9	5.89 E-11
	Power	1.01 E-5	1.01 E-5	1.14 E-5	1.39 E-5	1.39 E-8	3.10 E-8
0.6	Delay	3.29 E-11	5.04 E-11	4.01 E-8	1.42 E-9	1.15 E-9	6.10 E-11
	Power	5.56 E-6	5.56 E-5	1.4 E-5	7.81 E-5	1.44 E-8	2.37 E-8
0.5	Delay	4.90 E-11	7.73 E-11	4.16 E-8	1.58 E-9	1.31 E-9	1.28 E-10
	Power	2.44 E-6	2.46 E-5	1.4 E-5	3.50 E-5	3.1 E-8	5.55 E-8

Table: 2 Power-delay-product comparison of the Proposed Circuit with previous reported articles

Supply Voltage in Volt	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [6]	Scheme on paper [7]	Proposed Scheme
1	5.23E-16	7.97E-16	2.3E-13	3.94E-14	5.82E-17	4.69E-19
0.9	4.25E-16	6.43E-16	3.94E-13	4.1E-14	9.01E-17	6.02E-19
0.8	3.37E-16	5.07E-16	1.15E-12	2.9E-14	1.58E-17	2.23E-18
0.7	2.55E-16	3.86E-16	4.56E-13	1.88E-14	1.52E-17	1.83E-18
0.6	1.83E-16	2.8E-15	5.61E-13	1.11E-13	1.66E-17	1.45E-18
0.5	1.2E-16	1.9E-15	5.82E-13	5.53E-14	4.06E-17	7.1E-18

SIMULATION AND COMPARISON OF RESULTS

The circuits were simulated with using Cadence Specter using 90 nm technology using 1 V. The circuit was being compared with the OR gate previous techniques. The OR gate was implemented because it is a typical example of wide pull-down network. The proposed circuit was being implemented for OR gate and being compared with the OR gate of other reference circuits and also investigated with different values of fan-in. It was found that the proposed circuit performs better than the previous proposed circuits.

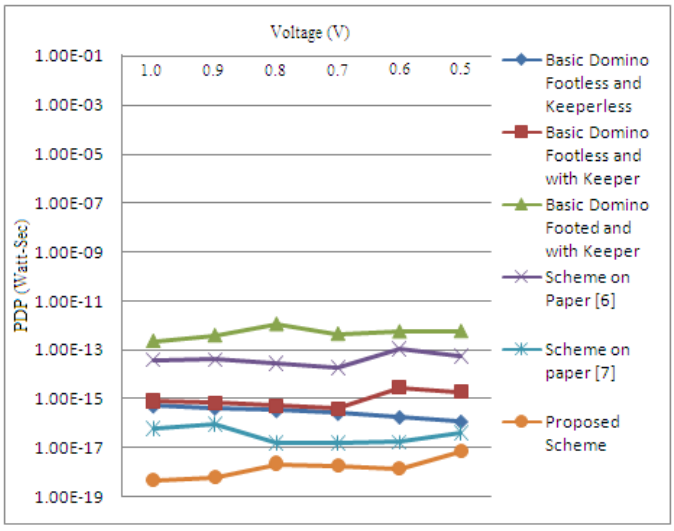

Figure 7. PDP Plot for the proposed scheme with the other schemes by reducing V_{DS} from 1 V to 0.5 mV

Table 3. Comparasion of the proposed circuit by number of transistors

Circuit type	Scheme on Paper [6]	Scheme on paper [7]	Proposed Scheme
Number of Extra transistor used	12	11	9
Use of Inverting clock	Yes	Yes	No

The PDP (Power-Delay Product) was calculated and simulated plotted using cadence spectre. Table 1 shows the power and delay of all the reference circuits, the basic circuits and the proposed circuit. Table 2 compares the power-delay product of the circuits. When compared to the other circuits it can be seen that the PDP can be reduced 100 times in the proposed circuit. This can also be viewed in the graph shown in figure 7. The proposed circuit shows advantage in having less number of transistors as compared to the previous Table 3. As compared to the basic domino the proposed circuit contains only 3 extra transistors where the other circuits contain more number of extra transistors with the disadvantage of having the inverting clock.

CONCLUSION

In this paper, we have proposed a high-speed and low-power domino logic circuit, which also have noise-tolerance in the output node. The simulation was done with 90 nm and 1 V CMOS process. The results have shown that the proposed scheme can work with very high speed and also consuming

very low power, which reduces the PDP of the circuit exponentially. Proposed circuit also shows noise efficiency because the noise of the output buffer dramatically improved as compared to previous work. Also the circuit is flexible for wide variety of dynamic logic styles and adequate for large fan-in gates.

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