Carbon Nanotube Interconnects for VLSI Design-A state of the art

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In recent times CMOS processes are scaled down to nanometer regime. While scaling is a desirable feature for VLSI design, new problems have evolved particularly for interconnects. Issues like electro migration, increasing resistivity, lithography limitations and the speed/delay of the copper interconnect have driven the need to find alternate interconnects. In order to mitigate such problems, changes in materials used for on-chip interconnects have been sought. This type of phenomena occurred earlier too when transition from Aluminum to copper took place. Currently Carbon nano tubes (CNTs) have emerged as a potential candidate to supersede copper interconnects because of their ballistic transport and ability to carry large current densities in the absence of electro migration. Moreover, this material provides extremely desirable properties of high mechanical strength, thermal stability and high thermal conductivity which are absolute requirements in case of interconnects. This investigation evaluates the potential use of CNTs as interconnects in IC design. This paper primarily focuses on the relative interconnect delay compared to copper and also the associated electrostatic discharge (ESD) problem. The resistance of copper interconnects, with extremely low cross-sectional dimensions in current and forthcoming technologies is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of highly resistive diffusion barrier layer. The steep rise in parasitic resistance of copper interconnects poses serious problems for interconnect delay especially when wire traverses long distances. Moreover, when a chip is connected to a board, there is unknown (potentially large) static voltage difference. Equalizing potentials requires (large) charge flow through the pads. Recently system on chip and embedded processors are used extensively, network on chip is the next technology. Therefore, it is also equally important to find out suitable alternative material for interconnects for VLSI design.

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