PLL with PI, PID and Fuzzy Logic Controllers based Shunt Active Power Line Conditioners

Karuppanan P and KamalaKanta Mahapatra

***Abstract*-- This paper presents a novel Phase Locked Loop (PLL) circuit in conjunction with Proportional Integral (PI) or Proportional Integral Derivative (PID) or Fuzzy Logic Controller (FLC) based shunt Active Power Line Conditioners (APLC) for the power-quality improvement such as current harmonics and reactive power compensation due to the non-linear/unbalanced loads. The shunt APLC system is implemented with three phase current controlled Voltage Source Inverter (VSI) and is connected at the point of common coupling for compensating the current harmonics by injecting equal but opposite filter currents. The compensation process is based on PLL synchronization with PI or PID or fuzzy logic controller. These controllers are capable of controlling dc-side capacitor voltage and estimating reference currents. Hysteresis Current Controller (HCC) is used to generate switching signals for the voltage source inverter. Extensive simulation studies under different non-linear and unbalanced load conditions are conducted, this simulation results analysis reveals that the APLC system performs perfectly with PI, PID and fuzzy logic control strategy. A comparative assessment of the three different controllers has been disclosed.**

***Index Terms*-- active power line conditioners (APLC), PLL synchronization, PI, PID, Fuzzy logic controller (FLC), hysteresis current controller (HCC).**

I. INTRODUCTION

AC power supply feeds different kind of linear and non-linear loads in commercial and industrial applications. The non-linear loads produce harmonics and reactive power related problems in the utility systems. The harmonic and reactive power cause poor power factor and distort the supply voltage at the customer service point [1-3]. Conventionally passive filters are used to compensate the lagging power factor of the reactive load and suppress the harmonic problems, but these passive filters are having some drawbacks; such as resonance, large in size, weight, and are limited too few harmonics. The different configurations of static VAR compensators (SVCs) are used for solving power quality issues; but some SVCs produce lower-order harmonics themselves and response time of some SVCs may be too long to be acceptable for fast-fluctuating loads [4-7]. Recently, Active Power Filters (APF) or Active Power-Line Conditioners (APLC) is developed for compensating harmonics and reactive power simultaneously. The active power filter topology can be connected in series for voltage harmonic compensation and in parallel for current harmonic compensation. Most of the industrial applications need current harmonic compensation, so the shunt active filter is popular than series active filter. The shunt active power filter has the ability to keep the mains current balanced and sinusoidal after compensation regardless of whether the load is non-linear and balanced or unbalanced [8-12].

The controller is the heart or primary component of the APLC system. Conventional PI and PID controllers are used to extract the fundamental component of the load current thus facilitating reduction of harmonics and simultaneously controlling dc-side capacitor voltage of the voltage source inverter. Recently, fuzzy logic controllers are used in power electronic system, drive applications and active power filters [13-17]. The phase locked loop controller can operate satisfactorily under highly distorted system, so a PLL in conjunction with one of these controllers is used.

This paper describes the feasibility of PI, PID and fuzzy logic controller along with PLL synchronization controller based shunt active power filter for the harmonics and reactive power mitigation due to the non-linear and unbalanced loads. The fundamental component of the reference current is extracted from load current using PI or PID or fuzzy logic controller methods and dc-side capacitor voltage of the inverter is continuously maintained constant. The voltage source inverter switching signals are generated from hysteresis band current control techniques. The proposed concept for shunt APLC system is validated through extensive simulation under different load conditions. A comparative assessment of PI, PID and FLC has been done.

II. PROPOSED CONTROL STRATEGIES

A) PI-Controller:

Fig 1 shows the block diagram of the proposed PI control scheme for the active power filter. The DC side capacitor voltage is sensed and compared with a reference voltage. This error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as

Karuppanan P, Research Scholar, Department of Electronics and Communication, National Institute of Technology, Rourkela, India-769008 (e-mail: karuppanan1982@yahoo.co.in).

KamalaKanta Mahapatra, Professor, Department of Electronics and Communication, National Institute of Technology, Rourkela, India-769008 (e-mail: kkm@nitrkl.ac.in).

978-1-4244-7781-4/10/$26.00 ©2010 IEEE

input for PI controller. The error signal is passed through Butterworth design based Low Pass Filter (LPF). The LPF filter has cutoff frequency at 50 Hz that can suppress the higher order components and allows only fundamental components. The PI controller is estimate the magnitude of peak reference current $I_{\max}$ and control the dc-side capacitor voltage of voltage source inverter. Its transfer function is represented as

$$H(s) = K_P + \frac{K_I}{s} \quad (1)$$

Where, [K_P =0.7] is the proportional constant that determines the dynamic response of the Dc-side voltage control and [K_I =23] is the integration constant that determines it's settling time. The proportional integral controller is eliminating steady state error in the DC-side voltage.

B) PID Controller:

Fig 1 shows the block diagram of the proposed Proportional Integrator Derivative (PID) control scheme of an active power filter. The error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PID controller. The error signal is passed through LPF; that can suppress the higher order components and pass only the fundamental component.

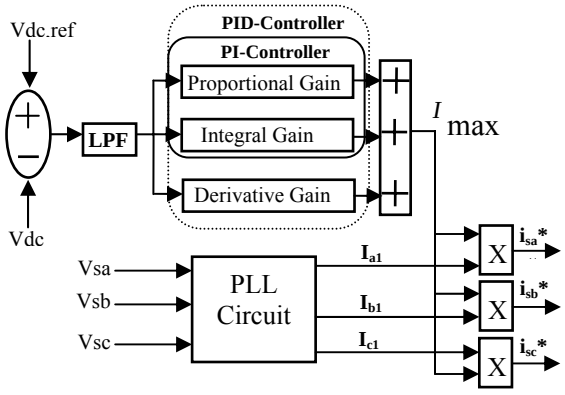

Fig 1 Blok diagram of the PLL with PI and PID Controller

The PID controller is a linear combination of the P, I and D controller. Its transfer function can be represented as

$$H(s) = K_P + \frac{K_I}{s} + K_D(s) \quad (2)$$

where, K_P is the proportional constant that determines the dynamic response of the Dc-side voltage control, K_I is the integration constant that determines it's settling time and K_D is the derivative of the error representing the trends. The controller is tuned with proper gain parameters [K_P =0.7, K_I =23, K_D =0.01] for estimating the magnitude of peak reference current $I_{\max}$ and control the dc-side capacitor voltage of inverter. The peak reference current multiplied with PLL output determines the desired reference current.

C) Fuzzy Logic Controller:

Fuzzy logic control is deduced from fuzzy set theory in 1965; where transition is between membership and non membership function. Therefore, limitation or boundaries of fuzzy sets can be undefined and ambiguous; FLC's are an excellent choice when precise mathematical formula calculations are impossible. Fig 2 shows block diagram of the fuzzy logic control scheme. In order to implement the control algorithm of a shunt active power filter in a closed loop, the dc capacitor voltage V_{DC} is sensed and then compared with the desired reference value $V_{DC,ref}$. The error signal $\left(e = V_{DC,ref} - V_{DC}\right)$ is passed through Butterworth design based LPF with a cut off frequency of 50 Hz; that pass only the fundamental component. The error signal $e(n)$ and integration of error signal is termed as $ce(n)$ are used as inputs for fuzzy processing. The output of the fuzzy logic controller limits the magnitude of peak reference current $I_{\max}$. This current takes care of the active power demand of the non-linear load and losses in the distribution system. The switching signals for the PWM inverter are generated by comparing the actual source currents $\left(i_{sa}, i_{sb}, i_{sc}\right)$ with the reference current $\left(i_{sa}^*, i_{sb}^*, i_{sc}^*\right)$ using the HCC method.

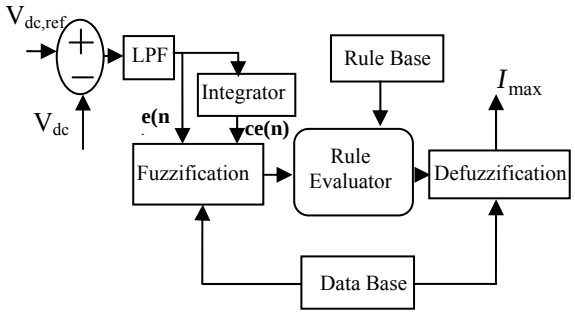

Fig 2 Fuzzy logic controller

Fuzzification:

Fuzzy logic uses linguistic variables instead of numerical variables. In a control system, error between reference signal and output signal can be assigned as Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (ZE), Positive small (PS), Positive Medium (PM), Positive Big (PB). The triangular membership function is used for fuzzifications. The process of fuzzification convert numerical variable (real number) to a linguistic variable (fuzzy number).

Rule Elevator:

Conventional controllers like PI and PID have control gains which are numerical values. Fuzzy logic controller uses linguistic variables instead of the numerical values. The basic fuzzy logic controller operation uses the following fuzzy set rules to control the system

AND -Intersection: $\mu_{A\cap B} = \min[\mu_A(X), \mu_B(x)]$

OR -Union: $\mu_{A\cup B} = \max[\mu_A(X), \mu_B(x)]$

NOT -Complement: $\mu_A = 1 - \mu_A(x)$

Defuzzification:

The rules of fuzzy logic controller generate required output in a linguistic variable (Fuzzy Number), according to real world requirements; linguistic variables have to be transformed to crisp output (Real number). This selection of strategy is a compromise between accuracy and computational intensity.

Database:

The Database stores the definition of the triangular membership function required by fuzzifier and defuzzifier.

Rule Base:

The Rule base stores the linguistic control rules required by rule evaluator (decision making logic). The rules used in this proposed controller are shown in table 1.

Table 1 Rule base table

ce(n) / e(n)	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	MN	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The output of the fuzzy controller is estimating the magnitude of peak reference current $I_{\max}$. This current $I_{\max}$ comprises active power demand of the non-linear load and losses in the distribution system. The peak reference current is multiplied with PLL output for determining the desired reference current.

D) PLL Synchronization:

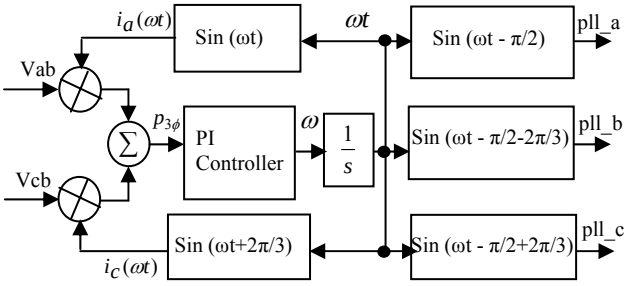

Fig 3 synchronizing PLL circuit

The phase locked loop circuit takes care of distorted and unbalanced voltages [6]. The block diagram of the PLL-synchronizing circuit shown in Fig 3; it determines automatically the system frequency and the fundamental positive sequence components of three phase line voltages $Vab\ (Vab = Vsa - Vsb)$ and $Vcb\ (Vcb = Vsc - Vsb)$. The outputs of the PLL synchronizing circuit are pll_a, pll_b, pll_c of the three phase templates. This algorithm is based on the three-phase instantaneous active power expression, it's written as

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c \qquad (3)$$

The current feedback signals $i_a(\omega t) = \sin(\omega t)$ and $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ is built up by the PLL circuit and time integral output ω is calculated using a proportional integral controller. It is having unity amplitude and $i_c(\omega t)$ leads by 120^0 compared to $i_a(\omega t)$. The PLL synchronizing circuit can reach a stable point of operation when the input $p_{3\phi}$ of the PI controller has a zero average value ($p_{3\phi} = 0$) and has minimized low-frequency oscillating portions in three phase voltages. Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and the phase angle of the supply voltage at fundamental frequency is reached. At this condition, the currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing outputs are set as

$$pll_a = \sin(\omega t - \pi/2) \qquad (4)$$

$$pll_b = \sin(\omega t - \pi/2 - 2\pi/3) \qquad (5)$$

$$pll_c = \sin(\omega t - \pi/2 + 2\pi/3) \qquad (6)$$

Therefore the PLL output signals pll_a, pll_b, pll_c and the distorted/unbalanced source voltages Vsa, Vsb, Vsc of the power supply are measured and which are in phase with the fundamental component. The PLL output multiplied with PI or PID or fuzzy logic controller output (peak current $I_{\max}$) and determines the required reference current.

E) Hysteresis current controller (HCC):

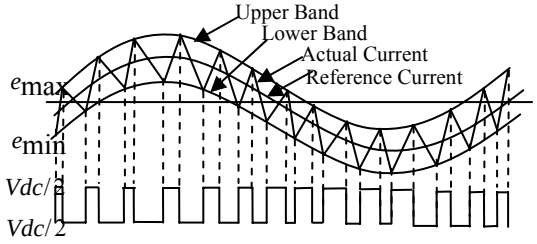

Fig 4 Diagram of hysteresis current control

HCC is utilized independently for each phase and directly generates the switching signals for three-phase voltage source inverter. An error signal $e(t)$ is the difference between the desired current $i_{ref}(t)$ and the actual current $i_{actual}(t)$. If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned OFF and the lower switch is turned ON. As a result, the current start to decay that is shown in Fig 4. If the error current crosses the lower limit of the hysteresis band, the lower switch of the inverter arm is turned OFF and the upper switch is turned ON. As a result, the current gets back into the hysteresis band. The switching performance as follows

$$S = \begin{cases} 0 & if\ i_{actual}(t) > i_{ref}(t) + h \\ 1 & if\ i_{actual}(t) < i_{ref}(t) - h \end{cases} \qquad (7)$$

Here the hysteresis band limit h=0.5. The interface inductor between inverter and PCC suppresses the harmonics caused by the switching operation of the inverter.

III. SIMULATION RESULT AND ANALYSIS

Three phase shunt APLC system is connected in the distribution network at the point of common coupling through filter inductances and operates in closed loop. The active power filter comprises six IGBTs with freewheeling diodes, a dc capacitor, RL-filter, compensation controller (PLL synchronization with PI or PID or fuzzy logic controller) and switching signal generator (hysteresis current controller) is shown in the Fig 5.

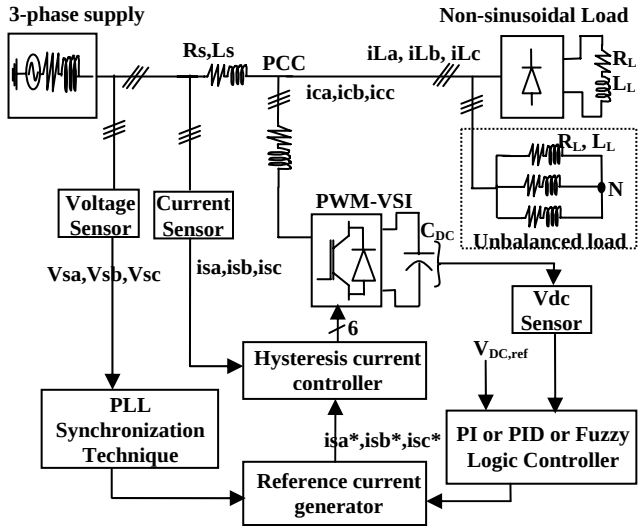

Fig 5 Structure of the shunt APLC system

The three phase source is connected with the non-linear load. The instantaneous source current $i_s(t) = i_L(t) - i_c(t)$ and the instantaneous source voltage are $v_s(t) = V_m \sin \omega t$ can be measured. The nonlinear load current will have a fundamental component and harmonic current components, which can be represented as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n) \qquad (8)$$

If the active power filter provides the total reactive and harmonic power, $i_s(t)$ will be in phase with the utility voltage and would be sinusoidal. At this time, the active filter must provide the compensation current $i_c(t) = i_L(t) - i_s(t)$ Therefore, the active power filter estimates the fundamental component of the load current and compensates the harmonic current and reactive power.

The performance of the proposed PI, PID and fuzzy logic control with PLL circuit strategy is evaluated through simulation using Matlab/Simulink power tools. The system parameters values are; Line to line source voltage is 440 V; System frequency (f) is 50 Hz; Source impedance of R_S, L_S is 1 Ω; 0.1 mH; Filter impedance of R_c, L_c is 1 Ω; 1 mH; Unbalanced $R_{L,}$ $L_{L,}$ values are 10 Ω, 50 Ω, 90 Ω and 10 mH respectively. Diode rectifier $R_{L,}$ L_L load: 20 Ω; 100 mH; DC side capacitance (C_{DC}) is 1200 μF; Reference voltage ($V_{DC,\,ref}$) is 400 V; Power devices used are IGBTs with diodes.

Case 1: Proportional Integral controller:

The three phase unbalanced RL load is connected in parallel with diode rectifier load to the three phase ac mains and active power filter is connected in parallel at the PCC for suppressing the harmonics and reactive power. The unbalanced RL load current is shown in 6 (a). The six-pulse diode rectifier load current is shown in Fig 6 (b)The source current after compensation is presented in Fig 6 (c) that indicates that the current becomes sinusoidal. The shunt active filter supplies the compensating current that is shown in Fig 6(d). This system achieves power factor correction as shown in Fig 6(e).

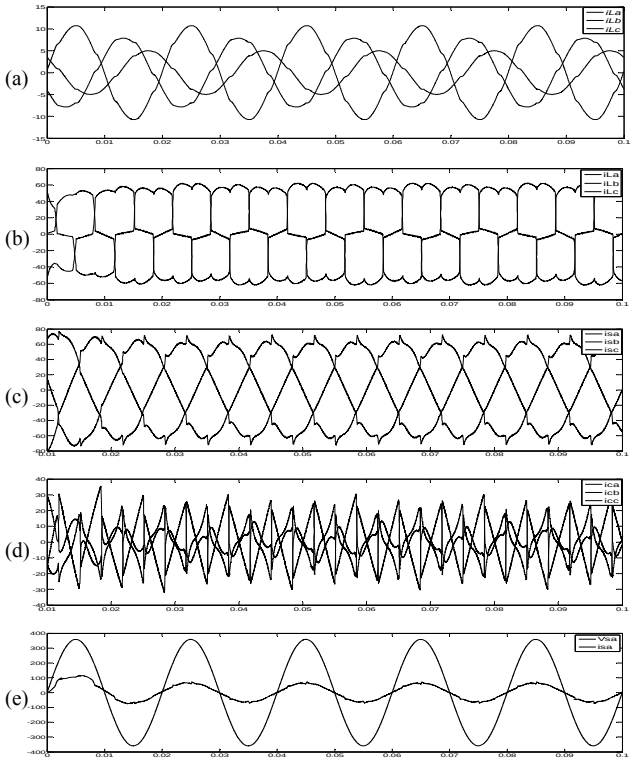

Fig 6 Simulation results for PI-controller based 3-phase APF under Non-linear with Unbalanced load condition (a) unbalanced RL- load current (b) source currents before compensation (c) Source current after compensation (d) Compensation current and (e) unity power factor

The dc side capacitance voltage (Cdc) and its settling time are controlled by PI-controller; this controller reduces the ripple and makes settling time less; these are plotted in Fig 7 for both non-linear *(t= 0.25s)* and non-linear with unbalanced load *(t=0.037s)*

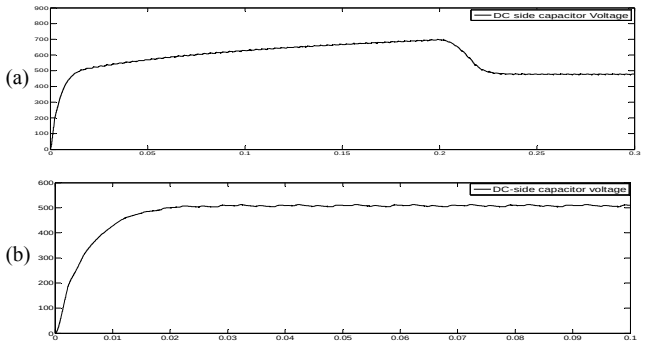

Fig 7 the DC side capacitor voltage settling time controlled by PI-controller (a) non-linear (t=0.25s) and (b) Non-linear with unbalanced load (t=0.037s)

The Fast Fourier Transform (FFT) is used to measure the order of harmonics at the source current. The magnitude of these harmonics is plotted in Fig 8 under non-linear with unbalanced load condition.

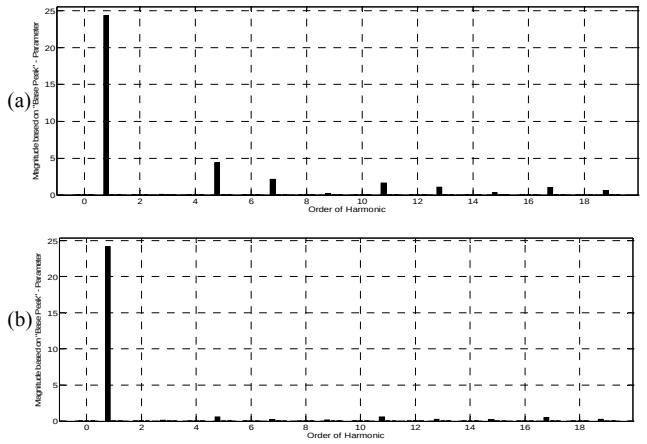

Fig 8 Order of harmonics (a) the source current without active filter (THD=22.37%), (b) with active power filter(THD=4.68%)

Case 2: Proportional Integral Derivative controller:

The PLL with PID controller simulation waveforms are verified and presented. The source current after compensation is in Fig 9 (a); that indicates the current is sinusoidal. The load current is shown in Fig 9 (b). The shunt active power filter supplies the compensating current that is shown in Fig 9(c).

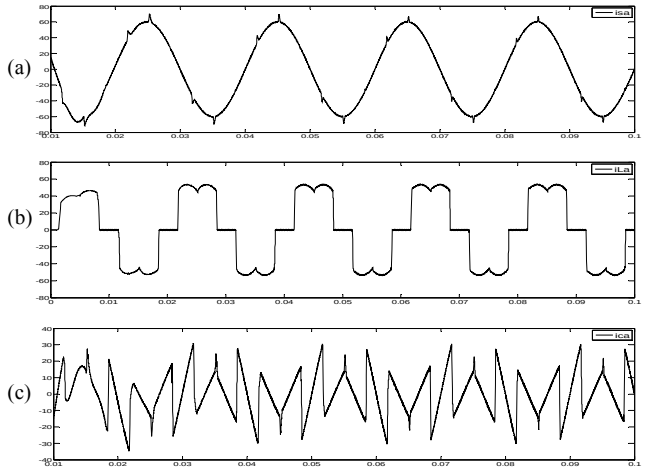

Fig 9 PID-controller based APF Simulations under non-linear load (a) Source current after active filter (b) Load currents (c) Compensation current

Case 3: Fuzzy logic controller:

PLL with FLC based APF system simulation results are verified and presented; the source current after compensation is presented in Fig 10 (a) that indicates the current is sinusoidal. The source current before compensation is shown in Fig 10 (b). The desired reference current is shown in Fig 10(c); this current is obtained from our proposed PLL synchronization with fuzzy logic controller. The shunt active power filter supplies the compensating current that is shown in Fig 10(d). The dc-side capacitance voltage (Cdc) and its settling time are controlled by FLC and is shown in Fig 10(e).

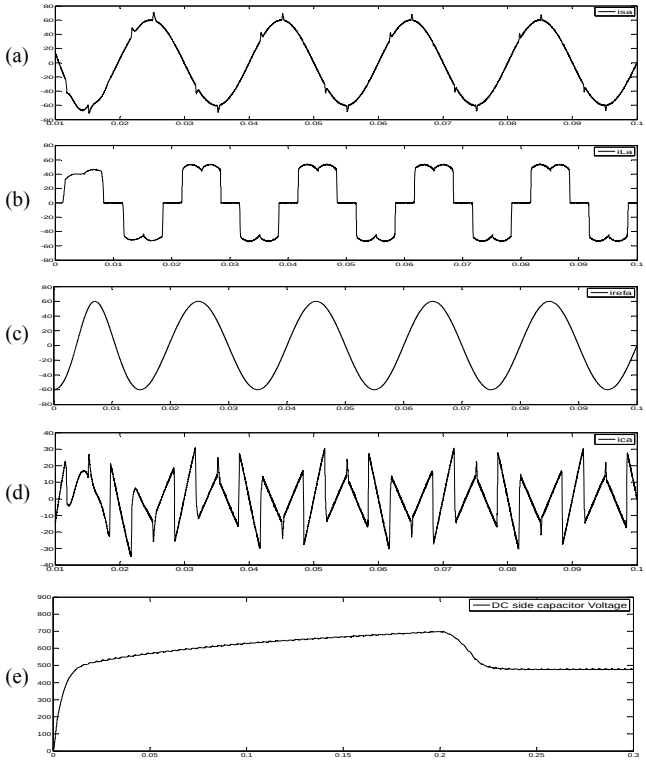

Fig 10 FLC based APF Simulation results under non-linear load (a) Source current after active filter (b) Load currents (c) Reference currents (d) Compensation current (e) DC side capacitor voltage settling time

The harmonic components evaluated using Fast Fourier Transform (FFT); that is plotted under non-linear load condition in the distribution system and is shown in Fig 11.

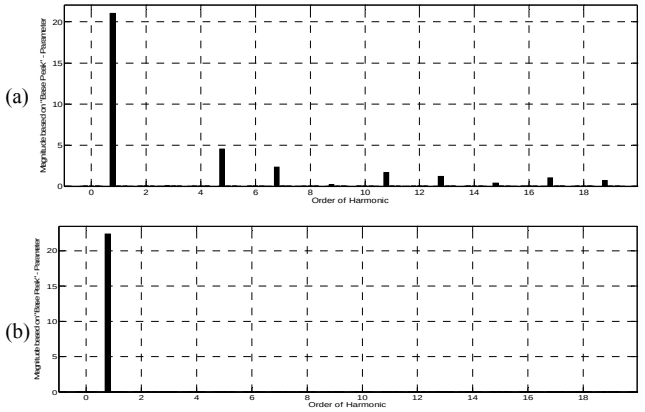

Fig 11FLC based APF; Order of harmonics (a) the source current without active filter (THD=26.79%), (b) with active power filter(THD=2.15%)

The settling time of the DC-side capacitor voltage of the inverter using PI, PID and fuzzy logic controller for different load conditions; these are presented in Table 2

Table 2 comparison of PI, PID and FLC for DC voltage settling time

Load conditions	V_{DC} settling time in seconds		
	PI	PID	FLC
Non-linear load	0.25s	0.23s	0.23s
Non-linear with Unbalanced load	0.037s	0.033s	0.029s

The THD before and after compensation with PI, PID and FLC control based APF are presented in Table 3 that facilitates comparison among these controllers.

Table 3 THD comparison of PI, PID and FLC Techniques

Load conditions	Source Current(I_S) without APF	Source Current(I_S) with APLC		
		PI	PID	Fuzzy logic
Non-linear load	26.79%	2.42%	2.36%	2.15%
Non-linear with Unbalanced load	22.37%	4.68%	4.54%	4.41%

The simulation is done for various non-linear and unbalanced load conditions. PI, PID and fuzzy logic controller with PLL synchronizing control based compensator filter makes the source current balanced and sinusoidal after compensation. FFT analysis of the active filter confirms that the THD of the source current is in compliance with IEEE-519 and IEC 61000-3 harmonic standards.

IV. Conclusions

The investigation demonstrates that a PI or PID or fuzzy logic controller is conjunction with the PLL synchronizing circuit as the controller for APLC facilitates improving power quality. The PI or PID or FLC ensures that the dc-side capacitor voltage is nearly constant with small ripple besides extracting fundamental reference currents. The PLL synchronizing circuit assists the active filter to function even under distorted voltage or current conditions. The shunt APLC system is implemented with voltage source inverter and is connected at PCC for filtering the current harmonics and compensating the reactive power. The inverter gate control signals are derived from hysteresis band current controller. The performance of a PI, PID and fuzzy logic controlled APLC system is verified and compared under non-linear and unbalanced loads with various parameters that are presented graphically. This approach brings down the THD of the source current that is in compliance with IEEE-519 and IEC 61000-3 required harmonic standards.

V. Acknowledgment

The authors would like to acknowledge to Ministry of Communication and Information Technology (MCIT), Govt. of India for the financial support.

VI. References

[1] Hirofumi Akagi, Edson hirokazu watanabe and Mauricio Aredes "Instantaneius power theory and applications to power conditioning" IEEE-press chapter 3-4,pp.19-107, 2007

[2] Bhim Singh, Kamal Al-Haddad & Ambrish Chandra, "A New Control Approach to 3-phase Active Filter for Harmonics and Reactive Power Compensation"-IEEE Trans. on Power Systems, Vol. 46, No. 5, pp. 133 – 138, Oct-1999

[3] Abdelmadjid Chaoui, Jean Paul Gaubert, Fateh Krim, Gerard Champenois "PI Controlled Three-phase Shunt Active Power Filter for Power Quality Improvement"- Electric Power Components and Systems, 35, pp.1331–1344, 2007

[4] Leszek S. Czarnecki "Instantaneous Reactive Power p-q Theory and Power Properties of Three-Phase Systems"- IEEE Trans on Power Vol. 21, No. 1, pp 362-367 Jan- 2006

[5] Luis F.C. Monteiro, Jose C.C.Costa, Mauricio Aredes, and Joao L.Afonso "A Control Strategy for Unified Power Quality Conditioner" Brazilan power electronics conference-july-2005

[6] Brod D.M, Novotny D.M "Current control of VSI-PWM Inverter"-IEEE TransonIndustryAppl,Vol.21,pp.562-570, 1985.

[7] Karuppanan P and Mahapatra, Kamala Kanta "Shunt Active Power Line Conditioners for compensating harmonics and reactive power" IEEE conference on Environment and Electrical Engineering, pp. 277 – 280, May 2010

[8] Zainal Salam, Tan Perng Cheng and Awang Jusoh "Harmonics Mitigation Using Active Power Filter: A Technological Review" ELEKTRIKA, VOL. 8, No. 2, pp.17-26, 2006

[9] K. K. Mahapatra, Arindam Ghosh and S.R.Doradla "Simplified model for control design of STATCOM using Three-Level Inverter"- IEEE Conference vol. 2, pp. 536-539- 1998

[10] Salem Rahmani, Nassar Mendalek and Kamal Al-Haddad "Experimental Design of a Nonlinear Control Technique for Three-Phase Shunt Active Power Filter" IEEE Trans on Industrial Electronics, Vol.57, No.10, pp.3364-3375, Oct-2010

[11] Fang Zheng Peng & Jih-Sheng Lai, "Generalized Instantaneous Reactive Power Theory for Three-Phase Power Systems" IEEE Trans. on Inst and Measent, Vol. 45, no. 1, pp293-297 Feb-1996

[12] Karuppanan P and Kamala kanta Mahapatra "PID with PLL Synchronization controlled Shunt APLC under Non-sinusoidal and Unbalanced conditions" National Power Electronics Conference (NPEC) Proceedings, IIT-Roorkee, June-2010.

[13] S.K. Jain, P. Agrawal and H.O. Gupta "Fuzzy logic controlled shunt active power filter for power quality improvement"-IEE proc.electr.power.appl,Vol 149, No.5, pp.317-328, Sept-2002

[14] S. Saad, L. Zellouma "Fuzzy logic controller for three-level shunt active filter compensating harmonics and reactive power" Electric Power Systems Research, pp.1337–1341 May-2009

[15] V. S. C. Raviraj and P. C. Sen "Comparative Study of Proportional–Integral, Sliding Mode, and Fuzzy Logic Controllers for Power Converters" IEEE Tran Industry Vol 33, No. 2, pp.518-524, Appl-1997.

[16] Marcelo Godoy Simoes, Bimal K. Bose, and Ronald J. Spiegel "Design and Performance Evaluation of a Fuzzy-Logic-Based Variable-Speed Wind Generation System" IEEE Trans on Industry Applications, Vol.33, No.4, pp.460-465, Aug-1997

[17] G.K. Singh, A.K. Singh, R. Mitra "A simple fuzzy logic based robust active power filter for harmonics minimization under random load variation" science direct-Electric Power Systems Research 77 pp.1101–1111, 2007

VII. Biographies

Mr.P.Karuppanan obtained B.E Degree in Electronics and Communication Engineering in 2004. He creditably completed his M.E Degree in VLSI Design in 2007. He is serving the National Institute of Technology-Rourkela, as a Research Scholar in the Department of Electronics and Communication from 2008 onwards. His focused on power quality, Analog and Digital VLSI design.

Kamala kanta Mahapatra received B.Tech degree with Honours in 1985 from University of Calicut, Master's in 1989 from Sambalpur University and Ph.D from Indian Institute of Technology, Kanpur in the year 2000 in Electrical Engineering .Currently, he is a Professor in the Electronics and Communication Engineering Department of National Institute of Technology Rourkela; he assumed this position since February 2004. He is a Fellow of the Institution of Engineers (India), His research interest includes Power Electronics, Embedded Systems, Electronic Circuits, FPGA based System design and VLSI Design.