PID WITH PLL SYNCHRONIZATION CONTROLLED SHUNT APLC UNDER NON-SINUSOIDAL AND UNBALANCED CONDITIONS

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ABSTRACT

This paper presents Shunt Active Power Line Conditioners (APLC) for compensating reactive power and harmonic currents drawn by the loads besides power factor correction. The shunt APLC is implemented with three phase PWM current controlled voltage source inverter and is connected to the point of common coupling for compensating the current harmonics. The compensation process is based on phase locked loop (PLL) synchronization and proportional integral derivative (PID) controller. These control strategies for shunt APLC makes certain that source current is sinusoidal even when the load is non-sinusoidal and unbalanced. The PWM-VSI inverter switching is done according to gating signals derived from hysteresis band current controller and the capacitor voltage is maintained constant using PID controller. The proposed shunt APLC is investigated using extensive simulation and is found to be effective in terms of THD, active filtering, reactive power compensation and V_{DC} settling time under various balanced and unbalanced load conditions

INTRODUCTION

Active power filters (APF) or active power line conditioners (APLC) have become significant for solving power quality problems [1-2]. In recent times power quality issue in industrial as well as manufacturing utilities has become a matter of serious concern due to the intensive use of power electronic equipments. Continuing proliferation of nonlinear loads is creating disturbances like harmonic pollution and reactive power problems in the power distribution lines [3-4]. The APLC can be connected in series or in parallel with the supply network for compensating harmonic and reactive power. The series active power filter is applicable to voltage harmonic compensation. Most of the industrial applications need current harmonic compensation, so the shunt active filter is popular than series active filter. Shunt APLC attempts to compensate the current harmonics of the load current by injecting opposite harmonics. The APLC is connected in parallel with the load at the point of common coupling (PCC). The APLC has the ability to keep the mains current balanced and sinusoidal after compensation regardless of whether the load is linear/non-linear and balanced or unbalanced [5]. The controller is the heart or primary component of the APF topology. Conventional PI and PID controllers are used to extract the fundamental component of the load current thus facilitating reduction of harmonics and simultaneously controlling dc capacitor voltage of the shunt APLC [6-8]. The phase locked loop (PLL) controller can operate satisfactorily under highly distorted and unbalanced system [3]. However, remarkable progress in the capacity and switching speed of power semiconductor devices such as insulated-gate bipolar transistors (IGBTs), development in the field of microelectronics technology has spurred interest in this area of APLC.

This paper presents proportional integral derivative (PID) with phase locked loop (PLL) synchronization controller based shunt active power filter for the harmonics and reactive power mitigation due to the non-sinusoidal and unbalanced loads. The PLL can operate satisfactorily under highly distorted and unbalanced system. The shunt APLC implemented with three phase PWM current controlled voltage source inverter and is connected to the ac mains for compensating the current harmonics by injecting equal but opposite current. The reference current(s) for the source are generated using PID controller and PLL controller algorithm. The PWM-VSI gate control signals are brought out from the hysteresis band current control technique. The capacitor voltage on the dc side of the inverter is continuously maintained constant with the help of PID controller. The proposed concept for shunt APLC is validated through extensive simulation under both balanced and unbalanced loads conditions.

DESIGN OF SHUNT APLC SYSTEM

Shunt APLC is connected to the point of common coupling (PCC) through filter inductances with power converter and operates in a closed loop. The three phase active filter comprises of six power transistors with diodes, a dc capacitor, filter inductor and the compensation controller (contains the PLL with PID controller and hysteresis current controller) shown in the fig 1.

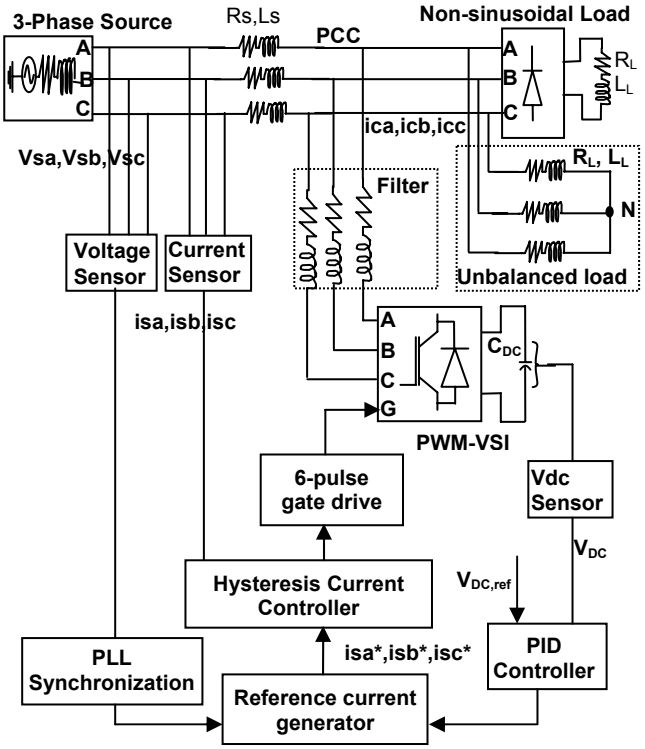

Fig 1 Shunt APLC implemented with PWM-VSI for the distribution system

The filter inductor suppresses the higher order harmonics caused by the switching operation of the power transistors. The filter provides smoothing and isolation for high frequency components and the desired current obtained by accurately controlling the switching of the inverter. Control of the current wave shape is limited by switching frequency of inverter and by the available driving voltage across the interfacing inductance [4].

Current supplied by shunt APLC:

The three phase instantaneous source current can be written as

$$i_s(t) = i_L(t) - i_c(t) \quad (1)$$

Source voltage is given by

$$v_s(t) = V_m \sin \omega t \quad (2)$$

If a nonlinear load is applied, then the load current would have a fundamental component and harmonic components, which can be written as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n)$$

$$= I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \quad (3)$$

The instantaneous load power can be multiplied from the source voltage and current and the calculation is given as

$$p_L(t) = i_s(t) * v_s(t)$$

$$= V_m \sin^2 \omega t * \cos\phi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \phi_1$$

$$+ V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right)$$

$$= p_f(t) + p_r(t) + p_h(t) \quad (4)$$

This load power contains fundamental or active power, reactive power and harmonics power. From this equation only the real (fundamental) power drawn by the load is

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos\phi_1 = v_s(t) * i_s(t) \quad (5)$$

From this equation the source current supplied by the main source, after compensation the source current should be sinusoidal is written as

$$i_s(t) = p_f(t) / v_s(t) = I_1 \cos\phi_1 \sin \omega t = I_{sm} \sin \omega t \quad (6)$$

where,

$$I_{sm} = I_1 \cos\phi_1 \quad (7)$$

The total peak current supplied by the source is

$$I_{sp} = I_{sm} + I_{sl} \quad (8)$$

If the active power filter provides the total reactive and harmonic power, $i_s(t)$ will be in phase with the utility voltage and would be sinusoidal. At this time, the active filter must provide the compensation current: $i_c(t) = i_L(t) - i_s(t)$ Therefore the APLC extracts the fundamental component of the load current and compensates for the harmonic and reactive power.

PROPOSED CONTROL SCHEME

The proposed control scheme includes reference current extraction control strategy using PLL synchronization technique with proportional integral derivative controller and PWM VSI with inner current control using hysteresis current modulator.

PID Controller

Fig. 2 shows the block diagram of the proposed Proportional Integrator Derivative (PID) control

scheme of an APLC. The DC side capacitor voltage is sensed and compared with a reference value. The error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PID controller. The error signal allows only fundamental frequency with the help of low pass filter (LPF). The LPF filter (Butterworth) has a cutoff frequency set at 50 Hz ; the fundamental power frequency. The PID controller is used to control the PWM-VSI input (dc side capacitor) voltage.

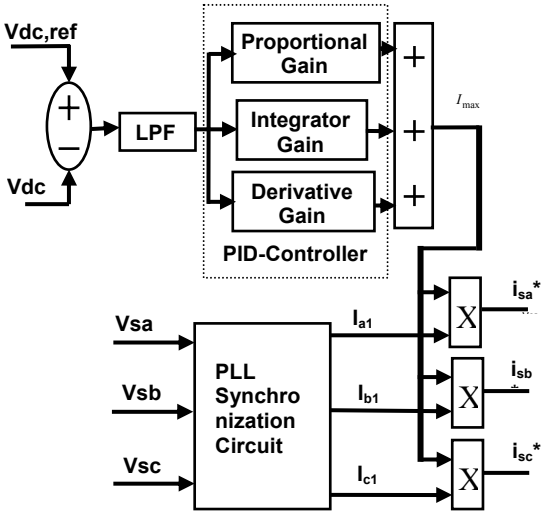

Fig 2 PID with PLL Controller block diagram

The PID controller is a linear combination of the P, I and D controller. Its transfer function can be represented as

$$H(s) = K_P + \frac{K_I}{s} + K_D(s) \qquad (9)$$

where, K_P is the proportional constant that determines the dynamic response of the DC-bus voltage control, K_I is the integration constant that determines it's settling time and K_D is the derivative of the error representing the trend. The controller is tuned with proper gain parameters [K_P=0.7, K_I=23, K_D=0.01]. The output of the PID controller is the magnitude of peak reference current $I_{\max}$. The peak reference current multiplied with PLL output determines the desired reference current.

PLL Synchronization

The PLL circuit tracks continuously the fundamental frequency of the measured system voltages (Vsa, Vsb, Vsc). The PLL design should allow proper operation under distorted and unbalanced voltage waveform [3] [6].

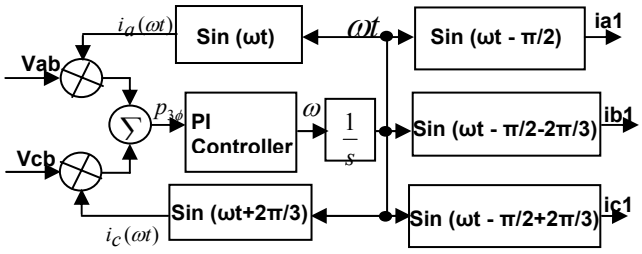

Fig 3 synchronizing PLL circuit

The PLL-synchronizing circuit shown in fig 3 determines automatically the system frequency and the inputs are line voltages $Vab\ (Vab = Vsa - Vsb)$ and $Vcb\ (Vcb = Vsc - Vsb)$. The outputs of the PLL synchronizing circuit are i_{a1}, i_{b1}, i_{c1} the three phase currents. This algorithm is based on the instantaneous active three-phase power expression, it's written by

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c \qquad (10)$$

The current feedback signals $i_a(\omega t) = \sin(\omega t)$ and $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ is obtained by the PLL circuit and time integral of output ω is calculated from the PID-Controller. It is having unity amplitude and $i_c(\omega t)$ lead to $120^0 i_a(\omega t)$ these represent a feedback from the frequency ω. The PLL synchronizing circuit can reach a stable point of operation when the input $p_{3\phi}$ of the PI controller has a zero average value ($p_{3\phi} = 0$) and has minimized low-frequency oscillating portions in three phase voltages. Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and the phase angle of the supply system voltage at fundamental frequency is reached. At this condition, the currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing output currents are defined as

$$i_{a1} = \sin(\omega t - \pi/2) \qquad (11)$$

$$i_{b1} = \sin(\omega t - \pi/2 - 2\pi/3) \qquad (12)$$

$$i_{c1} = \sin(\omega t - \pi/2 + 2\pi/3) \qquad (13)$$

Therefore the PLL output current signals i_{a1}, i_{b1}, i_{c1} and the distorted/unbalanced source voltages Vsa, Vsb, Vsc of the power supply are measured and which are in phase with the fundamental component. The PLL output multiplied with PID controller output determines the desired reference current.

Hysteresis Current Modulator

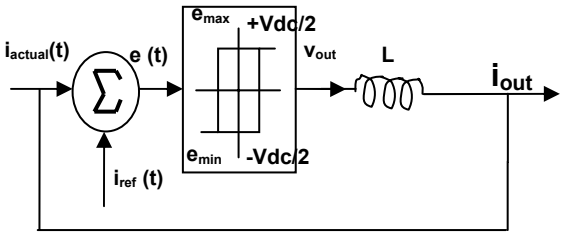

Fig 4 Diagram of hysteresis current control

The hysteresis current control (HCC) is the easiest control method to implement [7]. This error is the difference between the desired current $i_{ref}(t)$ and the current being injected by the inverter $i_{actual}(t)$ shown in fig 4. If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned off and the lower switch is turned on. As a result, the current starts decaying. If the error current crosses the lower limit of the hysteresis band, the lower switch of the inverter arm is turned off and the upper switch is turned on. As a result, the current gets back into the hysteresis band. The range of the error signal $e_{\max} - e_{\min}$ directly controls the amount of ripple in the output current from the PWM-VSI.

RESULT AND ANALYSIS

The performance of the proposed control strategy is evaluated through simulation using SIMULINK toolbox in the MATLAB. The system is investigated under balanced and unbalanced conditions. The system parameters used are; Line to line source voltage is 440 V; System frequency (f) is 50 Hz; Source impedance of R_S, L_S is 1 Ω; 0.1 mH; Filter impedance of R_c, L_c is 1 Ω; 1 mH respectively; Diode rectifier R_L, L_L load: 20 Ω; 200 mH respectively; Unbalanced three phase R_L, L_L load impedance: R1 = 10 Ω, R2 = 50 Ω, R3 = 90 Ω and 10 mH respectively; DC side capacitance (C_{DC}) is 1200 μF; Reference voltage ($V_{DC,\ ref}$) is 400 V; Power devices used are IGBT with diode.

Non-sinusoidal load condition:

The non-sinusoidal or non-linear RL load is a six-pulse diode Rectifier Bridge and is connected to main ac network. The parameters R L of the load are 20 ohms and 200 mH respectively and the simulation time is T=0 to T=0.2s. The waveform of source current after compensation is presented in fig. 5 (a); that clearly indicates that the current is sinusoidal. The six-pulse diode rectifier load current or source current before compensation is shown in fig 5 (b). The actual reference currents for three-phase are shown in fig. 5(c); this wave is obtained from our proposed PLL synchronization controller with PID controller. The shunt APLC supplies the compensating current that is shown in fig. 5(d). These current waveforms are for a particular phase (phase a). Other phases are not shown as they are only phase shifted by 120^0

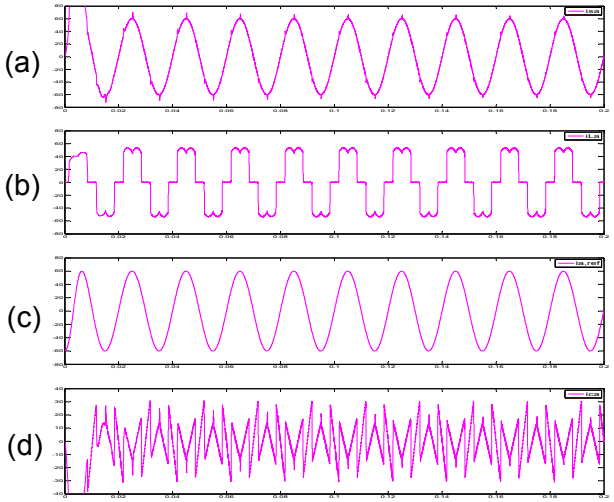

Fig.5 Simulation results for three-phase APLC under Non-sinusoidal load condition (a) Source current after APLC, (b) Load currents or source current before compensation, (c)Reference currents by the PID with PLL control algorithm and (d) Compensation current by APLC

Non-sinusoidal with Unbalanced load condition:

The three phase unbalanced RL load connected parallel with diode rectifier non-sinusoidal load in the three phase main network. The unbalanced load condition is also investigated and simulated without and with active power line conditioners. Unbalanced three phase RL load impedance are R1=10 Ω, R2=50 Ω, R3=90 Ω and 10 mH respectively and the simulation time is T=0 to T=0.2s. The unbalanced RL load current or source current before compensation is shown in 6 (a). The source current after compensation is presented in fig. 6 (b) that indicates that the current becomes sinusoidal. The shunt APLC supplies the compensating current based on the proposed controller that is shown in fig. 6(c). We have additionally achieved power factor correction as shown in fig. 6(d), a-phase voltage and a-phase current are in phase.

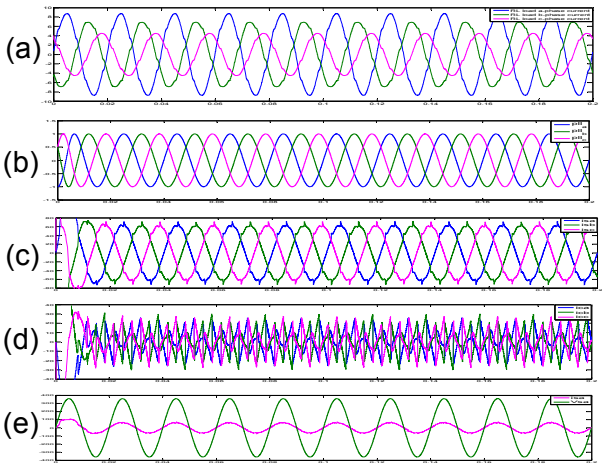

Fig.6 Simulation results for APLC under non-sinusoidal with Unbalanced load condition (a) RL Load current or Source current before APLC compensation, (b) PLL synchronization output current (c) Source current after APLC (d) Compensation current by APLC and (e) unity power factor waveforms.

DC side capacitor voltage settling time:
The dc side capacitance voltage and its settling time are controlled by PID controller. This controller reduces the ripple voltage to certain level and makes settling time low; these are shown in fig 7.

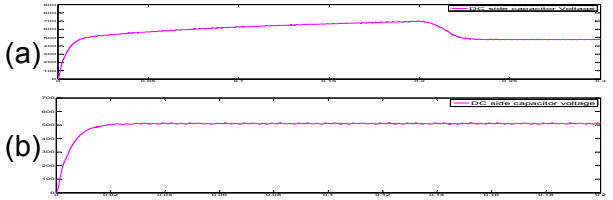

Fig 7 the DC side capacitor voltage settling time controlled by PID a) Non-sinusoidal (t= 0.23s) and b) Unbalanced load (t=0.031s)

Real and reactive power measurement
PID and PLL synchronizing controller based compensation improve the power quality. The active power and reactive power are calculated by averaging the voltage-current product at the fundamental frequency 50 Hz, are shown fig 8.

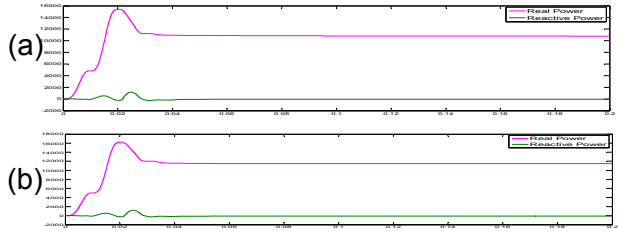

Fig 8 Active and Reactive power after APLC compensation under the (a) Non-sinusoidal load (P=10,800 kW, Q=0.035 kW) (b) Unbalanced load (P=11,500 kW, Q=0.108 kW)

The Real (P) and Reactive (Q) power are calculated and presented in the table 1.

Table 1 Real (P) and Reactive (Q) power measurement

Load Condition	Real (P) and Reactive (Q) power measurement	
	Without APLC	With APLC
Non-sinusoidal	P=9,090 kW Q= 1.297 kW	P=10,800 kW Q= 0.035 kW
Non-sinusoidal with Unbalanced	P= 10,410 kW Q= 1.222 kW	P= 11,500 kW Q= 0.108 kW

Order of harmonics plotted:
The Fourier analysis of the source current facilitates in extracting the fundamental as well as harmonics; signal f (t) is given as,

$$f(t) = \frac{a_o}{2} \sum_{n=1,2,3..}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \qquad (14)$$

The FFT results are plotted in Fig. 9 for various conditions as labeled.

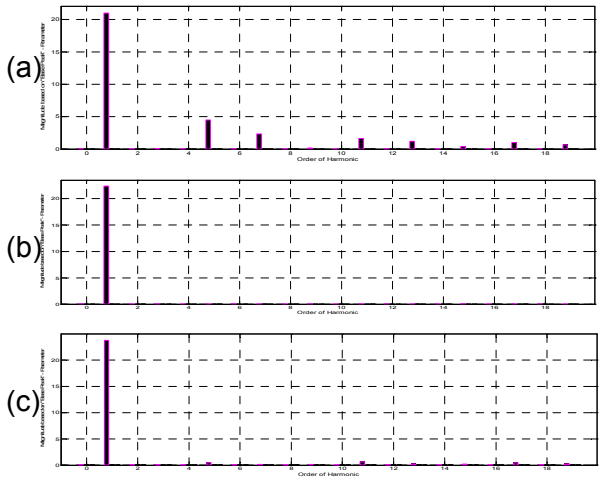

Fig 9 Order of harmonics (a) under the non-sinusoidal load condition, the source current without APLC (THD=26.86%), (b) under the non-sinusoidal condition with APLC (THD=1.49%) and (c) under the unbalanced load condition source current with APLC compensation(THD=3.74%)

Total harmonic distortion measured:
The PID controller and PLL synchronizing control based filter makes source current in the supply sinusoidal. The total harmonic distortion is measured using source current waveform. The total harmonic distortion is measured and compared, and presented in Table 2.

Table 2 FFT analysis of THD

Condition (THD)	Source Current(I_S) without APLC	Source Current(I_S) with APLC
Non-sinusoidal load	26.86 %	1.49 %
Non-sinusoidal with Unbalanced	22.98 %	3.74 %
Power factor	0.9143	0.9998

The simulation is conducted for various non-sinusoidal and unbalanced load conditions. The PID controller along with PLL controller based filter made source current balanced even if the system is unbalanced. FFT analysis confirms that the active filter brings the THD of the source current to be less than 5% that is in compliance with IEEE-519 standards for harmonic under both balanced/unbalanced conditions.

CONCLUSIONS

The investigation on proposed APLC demonstrated that PID controller maintains the dc side capacitor voltage nearly constant and also settles early even under unbalanced load conditions. This shunt active power line conditioner connected to the ac mains in parallel with the load; compensates the current harmonics and reactive power under unbalanced and non linear load conditions. The reference current(s) are generated using PID controller with PLL synchronizing control algorithm and PWM-VSI gate control signals are generated from hysteresis band current controller. The proposed shunt APLC validated using extensive simulation. The important performance parameters are presented graphically and THD is found to be 1. 49 % under balanced load conditions and 3.74 % under unbalanced a load condition that complies with IEEE 519 standards; thus the superior features of the proposed APLC are established.

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BIOGRAPHIES

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