A Novel Active Power Line Conditioners using PLL Synchronization and PI controller

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Abstract— **this paper presents Shunt Active Power Line Conditioners (APLC) for compensating reactive power and harmonic currents drawn by the loads besides power factor correction. The shunt APLC is implemented with three phase PWM current controlled voltage source inverter and is connected to the point of common coupling for compensating the current harmonics. The compensation process is based on phase locked loop (PLL) synchronization and proportional integral (PI) controller. These control strategy for shunt APLC makes certain that source current is sinusoidal even when the load is non-sinusoidal and unbalanced. The PWM-VSI inverter switching is done according to gating signals derived from hysteresis current controller and the capacitor voltage is maintained constant using PI controller. The proposed shunt APLC is investigated using extensive simulation and is found to be effective in terms of THD, active filtering, reactive power compensation and V_{DC} settling time under both transient and steady state conditions.**

Keywords— ***Active power line conditioners (APLC), phase locked loop (PLL), PI controller, Hysteresis current controller (HCC), current harmonics***

I. INTRODUCTION

Semiconductor device switches are widely employed to feed controlled ac power supply to different kind of non-linear loads such as adjustable speed drives (ASD's), furnaces, computer power supplies etc. These non-linear loads produce harmonics [1] [2]**.** The harmonics and reactive power in a distribution power system will bring about serious problems. The reactive power and harmonics also cause poor power factor and distort the supply voltage at the common coupling point (PCC). This distortion is mainly induced from the line impedance or the distribution transformer leakage inductance. Passive L-C filters are used to compensate the lagging power factor due to reactive loads and harmonics because of non-linear loads, but due to the drawbacks such as resonance, size, weight, etc; these are not accepted well in the industry. The alternative solution is an active power filters (APF) or active power line conditioners (APLC) that is being considered as an effective solution for mitigating these problems [3]. APLCs are superior to passive filters in terms of filtering characteristics and also improve the system stability by removing resonance related problems [4]. At the point of common coupling (PCC) of the utility interface, APLC can absorb/supply all the harmonics and reactive-power current generated by the nonlinear loads and finally makes the source current sinusoidal. The controller is the primary component of the active filter topology and extensive research is being conducted in recent years. PI controller and PLL controllers are used to extract the fundamental component of the load current thus facilitating reduction of harmonics and control dc capacitor voltage of the shunt APLC. Different topologies and control techniques have been proposed in the literature [1-5]. However, remarkable progress in the capacity and switching speed of power semiconductor devices such as insulated-gate bipolar transistors (IGBTs), development in the field of microelectronics and FPGA technology has spurred further interest in the area of APF for power conditioning [6-7]

This paper presents an APLC that is controlled using synchronizing PLL and PI controller. The ac source voltage(s) and the dc capacitor voltage are used for generating reference source currents with the help of the controller. A hysteresis current controller generates switching signals for the APLC to follow the reference currents within specified band-limits. APLC improves the utility supply system power factor as the ac source provides only active fundamental frequency component, also provides reactive-power compensation, harmonic compensation, and negative-sequence current/voltage compensation. It provides good compensation characteristics in steady state as well as transient states.

II. INSTANTANEOUS POWER THEORY

Active power line conditioners are connected to the PCC through filter inductances and operate in a closed loop. The active filter comprises of power transistors, power diodes, dc capacitor and filter inductor and the controller. The filter inductor and reactors also suppress the harmonics caused by the switching operation of the power transistors. Reduction of current harmonics in the load current is achieved by injecting equal but opposite current harmonic components at the point of common coupling, there by canceling the original distortion and improving the power quality of the connected power system. The block diagram of APLC consisting of PLL synchronization circuit (current reference generator), hysteresis current controller (gating signal generator) and a dc voltage control unit (PI controller) is shown in Fig 1. The output voltage of the inverter is controlled with respect to the voltage at the point of common coupling.

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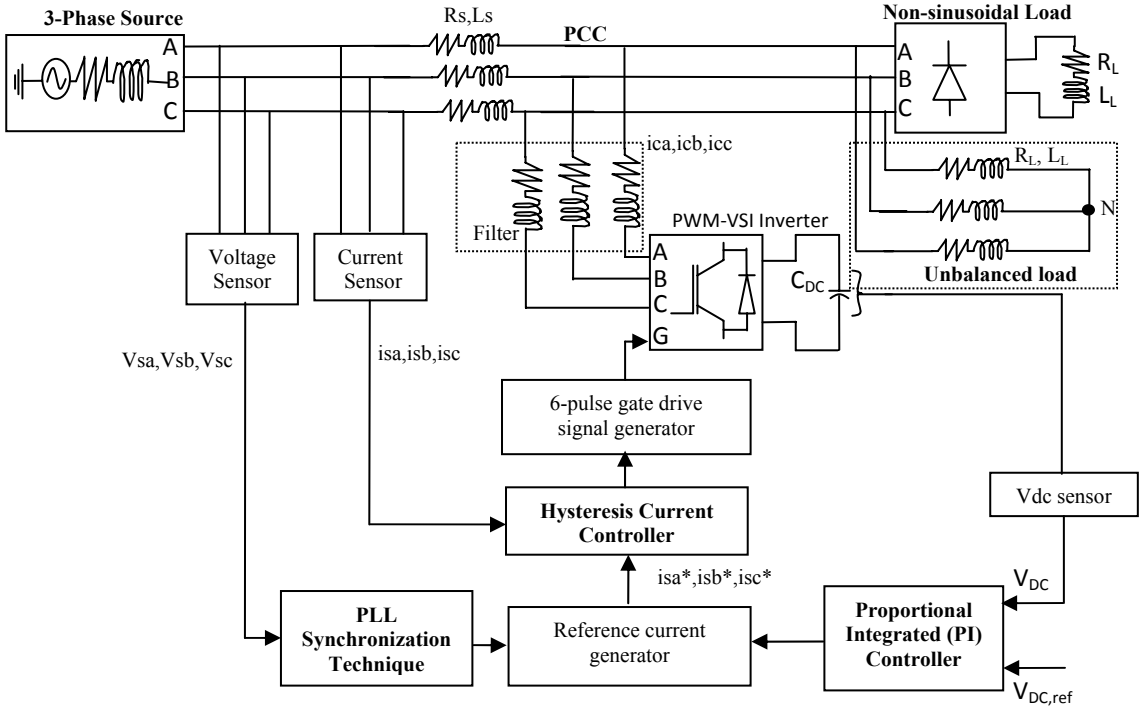

Fig 1 Shunt APLC implemented with PWM-VSI in the distribution ac network

The choice of DC side capacitor C_{DC} is governed by the amount of ripple that can be allowed on the dc side capacitor without affecting performance. The three phase instantaneous source current can be written as [4]

$$i_s(t) = i_L(t) - i_c(t) \tag{1}$$

Here the filter (harmonics) current is subtract from the load current. The source voltage is given by

$$v_s(t) = V_m \sin \omega t \tag{2}$$

If a nonlinear load is applied, then the load current will have a fundamental component and harmonic components, which can be represented as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n)$$

$$= I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \tag{3}$$

The instantaneous load power can be given as

$$p_L(t) = i_s(t) * v_s(t)$$

$$= V_m \sin^2 \omega t * \cos\phi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \phi_1$$

$$+ V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right)$$

$$= p_f(t) + p_r(t) + p_h(t) \tag{4}$$

From this equation the real (fundamental) power drawn by the load is given by

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos\phi_1 = v_s(t) * i_s(t) \tag{5}$$

From the following equation, the source current supplied by the source, after compensation is derived as

$$i_s(t) = \frac{p_f(t)}{v_s(t)} = I_1 \cos\phi_1 \sin \omega t = I_{sm} \sin \omega t \tag{6}$$

where,

$$I_{sm} = I_1 \cos\phi_1 \tag{7}$$

The total peak current supplied by the source is

$$I_{sp} = I_{sm} + I_{sl} \tag{8}$$

If the active filter provides the total reactive and harmonic power, then $i_s(t)$ will be in phase with the utility voltage and purely sinusoidal. At this time, the active filter must provide the following compensation current:

$$i_c(t) = i_L(t) - i_s(t) \tag{9}$$

The desired source currents, after compensation, can be given

$$i_{sa}^* = I_{sp} \sin \omega t \tag{10}$$

$$i_{sb}^* = I_{sp} \sin(\omega t - 120^0) \tag{11}$$

$$i_{sc}^* = I_{sp} \sin(\omega t + 120^0) \tag{12}$$

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where $I_{sp} = I_{sm} + I_{sl}$ is the amplitude of the desired source current; the phase angle can be obtained from the source voltages. This peak value of the reference current has been estimated by regulating the DC side capacitor voltage of the PWM converter.

III. SHUNT APLC SYSTEM

The proposed control system consists of reference current control strategy using PLL synchronization, DC voltage PI controller and control of PWM inverter of hysteresis current modulator:

1) DC voltage PI controller:

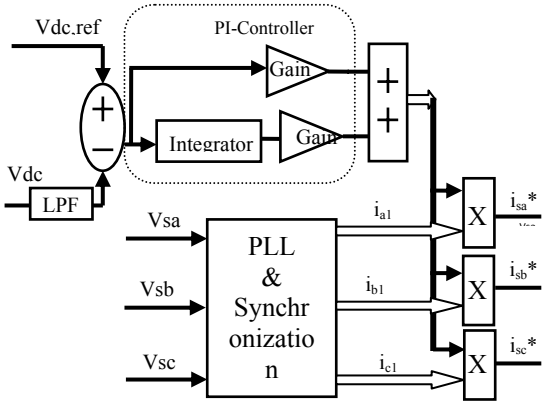

Fig 2 PI Control block diagram

Figure 2 shows the block diagram of the proposed PI control scheme for the APLC. The DC side capacitor voltage is sensed and compared with a reference value. The error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PI controller. PI controller used to control the PWM-Voltage source inverter input (dc side capacitor) voltage. Its transfer function can be represented as

$$H(s) = K_P + \frac{K_I}{s} \tag{13}$$

where, K_P is the proportional constant that determines the dynamic response of the DC-bus voltage control and K_I is the integration constant that determines it's settling time. PI controller is used to eliminate the steady state error in dc voltage. The proportional gain [K_P =0.7] and integral gain [K_I =23] are set such way that V_{dc} across capacitor is maintained nearly constant.

2) PLL and Synchronization:

The PLL circuit tracks continuously the fundamental frequency of the measured system voltages (Vsa, Vsb, Vsc). The PLL design should allows proper operation under distorted and unbalanced voltage waveform [3]. The PLL-synchronizing circuit shown in fig 3 determines automatically the system frequency and the inputs are line voltages Vab $(Vab = Vsa - Vsb)$ and Vcb $(Vcb = Vsc - Vsb)$.

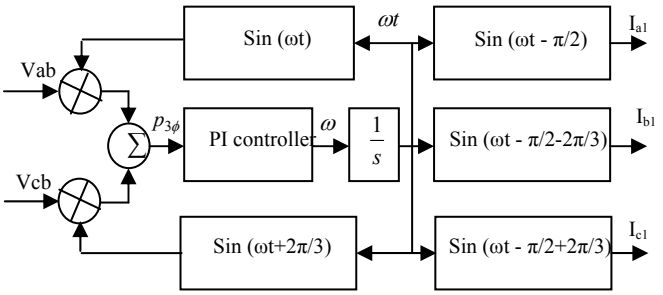

Fig 3 synchronizing PLL circuit

The outputs of the PLL synchronizing circuit are i_{a1}, i_{b1}, i_{c1} the three phase currents. This algorithm is based on the instantaneous active three-phase power expression, it's given by

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c \tag{14}$$

The current feedback signals $i_a(\omega t) = \sin(\omega t)$ and $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ is built up by the PLL circuit and time integral of output ω calculated of the PI-Controller. It is having unity amplitude and $i_c(\omega t)$ lead to 120^0 $i_a(\omega t)$ these represent a feedback from the frequency ω . The PLL synchronizing circuit can reach a stable point of operation when the input $p_{3\phi}$ of the PI controller has a zero average value ($p_{3\phi} = 0$) and has minimized low-frequency oscillating portions in three phase voltages. Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and the phase angle of the supply system voltage at fundamental frequency is reached. At this condition, the currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing output currents are defined as

$$i_{a1} = \sin(\omega t - \pi/2) \tag{15}$$

$$i_{b1} = \sin(\omega t - \pi/2 - 2\pi/3) \tag{16}$$

$$i_{c1} = \sin(\omega t - \pi/2 + 2\pi/3) \tag{17}$$

Therefore the PLL output current signals i_{a1}, i_{b1}, i_{c1} and the distorted/unbalanced source voltages Vsa, Vsb, Vsc of the power supply are measured and which are in phase with the fundamental component. The PLL output current is multiplied with PID controller output of peak reference current I_{sm} for determined the desired reference current.

3) Hysteresis current modulator:

The PWM-VSI gate control signals are derives from hysteresis band current controller. The hysteresis current control (HCC) is the easiest control method to implement [7]. An error signal $e(t)$ is used to control the switches in a PWM-VSI. This

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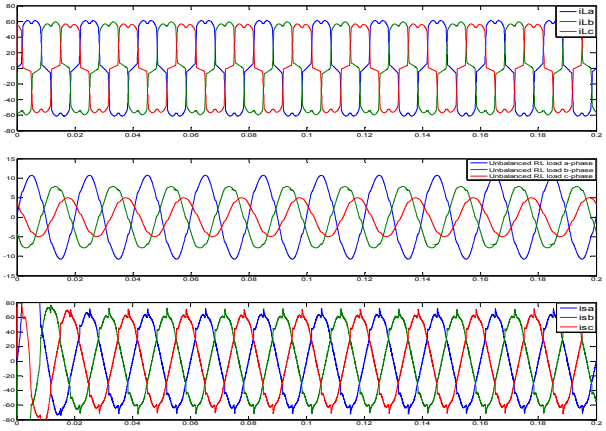
error is the difference between the desired current $i_{ref}(t)$ and the current being injected by the inverter $i_{actual}(t)$ If the error current exceeds the upper limit of the hysteresis band, the upper switch of the inverter arm is turned off and the lower switch is turned on. As a result, the current starts to decay. If the error current crosses the lower limit of the hysteresis band, the lower switch of the inverter arm is turned off and the upper switch is turned on. As a result, the current gets back into the hysteresis band. The minimum and maximum values of the error signals are derived as $e_{\min}$ and $e_{\max}$ respectively. The range of the error signal $e_{\max} - e_{\min}$ directly controls the amount of ripple in the output current from the PWM-voltage source inverter.

IV. SIMULATION RESULT AND ANALYSIS

The system parameters values are; source line to line voltage (Vs) is 440 V, System frequency (f) is 50 Hz, Source impedance of R_S, L_S is 1 Ω; 0.1 mH respectively, Filter impedance of R_c, L_c is 1 Ω; 1 mH, unbalanced RL load impedance are R1=10 Ω, R2=50 Ω, R3=90 Ω and 10 mH respectively, diode rectifier RL load in Steady state: 20 Ω; 200 mH and Transient: 10 Ω; 100 mH respectively, DC link capacitance (C_{DC}) is 1200μF, Reference Voltage (V_{DC}) is 400 V and Power devices used are IGBT/Diode.

Steady state conditions:

The three phase unbalanced RL load is connected in parallel with diode rectifier a non-linear load (R=20 Ω and L= 200 mH for steady state) in the three phase main network. Unbalanced three phase RL load impedance are R1=10 Ω, R2=50 Ω, R3=90 Ω and 10 mH respectively and the simulation time is T=0 to T=0.2s counted. The non-linear load and unbalanced RL load current or source current before compensation is shown in 4 (a) and (b) respectively. The source current after compensation is presented in fig. 4 (c) that indicates that the currents become sinusoidal. The reference currents generated using the PLL and PI controller shown in fig. 4(d). The shunt APLC supplies the compensating currents shown in fig. 4(e). The power factor correction is shown in fig. 4(f) and DC side PWM-VSI capacitor voltage settling time shown in fig 4(g).



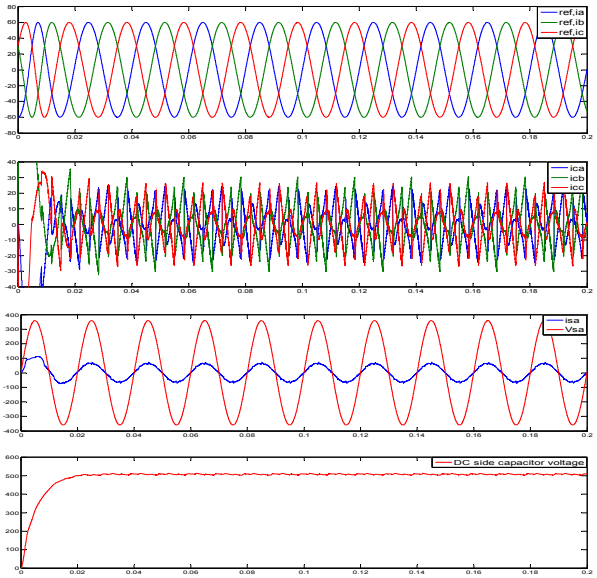


Fig.4 Simulation results for three-phase active-power-line conditioners under the steady state condition (a) source current or non-linear Load current before APF, (b)Unbalanced current before compensation, (c) Source current after APF, (d)Reference currents, (e) Compensation current by APLC, (f) source voltage per current for unity power factor and (g) DC capacitor voltage settling time (t_s=0.0.023s)

Transient conditions:

The three phase unbalanced RL load is connected in parallel with diode rectifier non-sinusoidal load (R=10 Ω and L= 100 mH for transient) in the three phase main network. The simulation is fig 5; focus on one phase (a-phase) out of three phases.

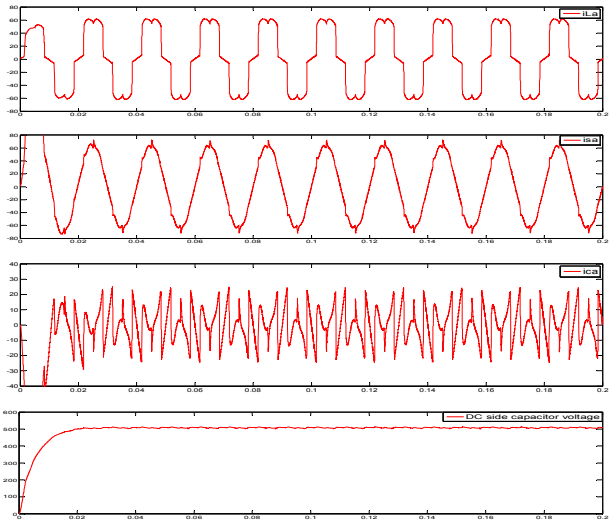


Fig.5 Simulation results for three-phase active-power-line conditioners under the transient condition (a) source current or Load current before APF, (b) Source current after APLC, (c) Compensation current by APF, and (d) DC capacitor voltage settling time (t_s=0.025s)

The active power and reactive power are calculated by averaging the voltage-current product with a running average

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window over one cycle of the fundamental frequency of 50 Hz. The APLC system reduces the reactive power, in fig 6.

$$P = \frac{1}{T}\int_{t-T}^{t} V(\omega t) \times I(\omega t)dt \quad (18)$$

$$Q = \frac{1}{T}\int_{t-T}^{t} v(\omega t) \times i(\omega t - \pi/2)dt \quad (19)$$

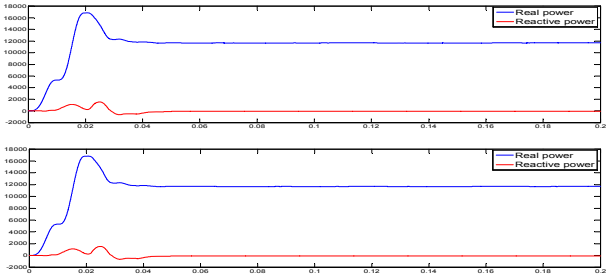

Fig 6 Active and Reactive power at diode rectifier RL load and Unbalanced load with APLC under (a) the steady state condition (P=11,690 kW, Q=0.087 kW) and (b) the transient conditions (P=11,690 kW, Q=0.092 kW)

The summarized Real (P) and Reactive (Q) power calculation under steady state and transient condition are presented in table 1. The results indicate APLC improves the power quality increases real power and reduce the reactive power.

Table 1 Real (P) and Reactive (Q) power measurement

Condition	Real (P) and Reactive (Q) power measurement	
	Without APLC	With APLC
Steady state	P=10,690 kW Q=1.229 kW	P=11,690 kW Q=0.087 kW
Transient	P=10,710 kW Q=1.234 kW	P=11,690 kW Q=0.092 kW

Total Harmonic distortion measurement (THD) of the fundamental frequency of APLC in the steady state and transient condition by PLL and PI controller. The simulation is showing without and with active power filter.

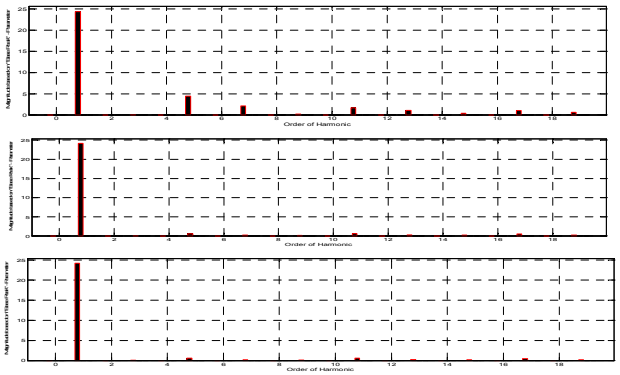

Fig 7 Order of harmonic current under the steady state and transient conditions (a) the source current without APLC (THD=26.86%) under steady state, (b) steadt state with APLC (THD=4.53 %) and (c) source current with APLC compensation(THD=4.64 %) under transient ondition.

The PI controller and PLL synchronizing control based compensator filter makes sinusoidal source current in the supply. The total harmonic distortion measured and compared both steady state and transient conditions are tabulated 2.

Table 2 FFT analysis of Total harmonic distortion (THD)

Condition	THD of Source Current(I_S) without APLC	THD of Source Current(I_S) with APLC
Steady state	22.44 %	4.53 %
Transient	22.31 %	4.64 %
Power factor	lagging	unity

The simulation is done various non-sinusoidal and unbalanced load conditions. The obtained result shows the source current and load current is having small variation in steady state and transient conditions. The PI controller with PLL synchronizing control based compensator filter makes the system balanced responsibility even if the system is unbalanced. FFT analysis of the active filter indicates the THD of the source current less than 5% into compliance with IEEE-519 standards.

V. CONCLUSIONS

Proportional-Integral controller in conjunction with PLL synchronization circuit extracts the fundamental component of the source current(s). Through extensive simulation it is observed that the performance of the shunt APLC is quite satisfactory as it reduces harmonics and reactive power components of the load current(s) resulting in sinusoidal and unity power factor source currents under both transient and steady state conditions. We observe that THD in the source current reduces significantly with the proposed APLC (from 22.44 % to 4.43 %). The APLC is in compliance to the THD requirements of the IEEE-519 standards harmonics.

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