A Novel Control Strategy for 400 Hz Aircraft Power Supply Using Resonant DC Link Inverter

Sushant kumar Pattanaik and K. K. Mahapatra

***Abstract* — This paper presents the control aspects in designing an aircraft power supply. Power supply design is done using a soft-switched Resonant DC Link Inverter (RDCLI). A novel current initialization scheme is adopted to avoid zero crossing failures. Zero-hysteresis bang-bang control is used for current control within the inverter. The power supply is designed for 400 Hz load. The soft-switched inverter provides adequate current regulator bandwidth besides reducing switching losses. The proposed solution is validated through extensive simulation.**

***Index Terms*—Aircraft System, Current Initialization Scheme, Soft-Switching Inverter, RDCLI (Resonant DC Link Inverter), ZVS (Zero Voltage Switching).**

I. INTRODUCTION

In the future, the Aircraft will tend to use electrical power rather than hydraulic, pneumatic or mechanical power. This will increase the demands on the electrical power systems, and it is an open question as to how far advanced power electronics will assist in their viable realization. The application areas most closely associated with this transition are Variable Speed Constant Frequency (VSCF) power conversion, Electro-hydraulic/-mechanical Actuation (EHAEMA), and Fuel Pumps. At the core of each is a power electronics inverter, with key functional issues being: high frequency operation, reliability, fault tolerance, power waveform quality, elevated temperature operation, and EMI regulation compliance.

One of the absolutely fundamental questions in current research and development of suitable power electronic inverter are the choice of circuit topology. In particular, the circuit can be either “hard-switched" or "soft-switched", and there are innumerable variants of both types: hence, the variant best suited to the associated application is to be determined.

A 400 Hz Aircraft power generating system is introduced which has been designed to achieve significant improvements in power density and reliability. At the heart of the new variable speed constant-frequency (VSCF) configuration is a high-frequency resonant dc link inverter designed so that all inverter switching occurs under zero-voltage conditions. Advantages include minimization of switching losses and significant reductions in power device switching and electromagnetic interference (EMI) generation.

Sushant Kumar Pattnaik is a Research Scholar and continuing M. Tech(R) at National Institute of Technology Rourkela. (Mob: 0-94370-82906, e-mail: sushantpattnaik@gmail.com).

K. K. Mahapatra is Professor at National Institute of Technology Rourkela. (Ph: 0-661-2462454, e-mail: kmaha2@rediffmail.com).

II. AIRCRAFT SYSTEMS

Objectives inherent in the design of Aircraft suitable systems are increases in reliability, power density, system flexibility, and maintainability combined with a reduction in the cost of ownership. These issues are perhaps clearer in the mergence of the power electronic conversion stage known as VSCF system. A generic VSCF system entails both a Generator and a solid-state Power Conditioning Unit (PCU). Generation and distribution of 400 Hz power has hitherto been recognized as the accepted aerospace standard for applications requiring power installation exceeding several tens of KVA. The reason of using 400 Hz (Standard practice dictates that it should be 8 times of the line frequency i.e., 50 Hz) is, if we increase the frequency, then it is obvious that flux would decrease, which is verified from the transformer equation $V = 4.44 f \phi T$. From this equation one can easily understand that if we increase the frequency, the sizes of the load that are connected across the power supply are reduced. Generally in an aircraft, there are many number of loads (motors, compressors, etc...) connected. Hence more space is created.

The advantage of high-frequency alternators is that they require fewer copper coils in order to generate the necessary electrical current. This reduction in material allows the alternator to become much smaller such that it takes up less space and weighs much less than it would otherwise.

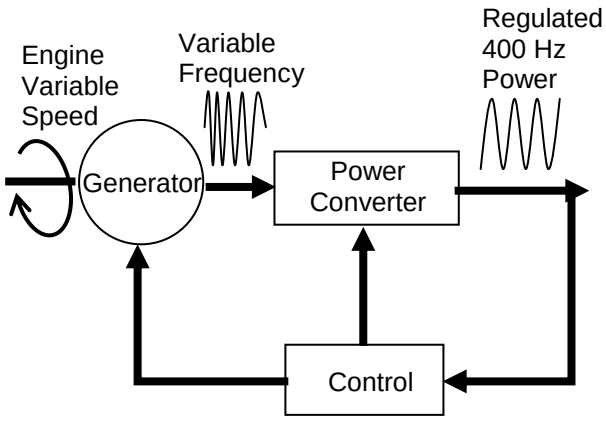

Fig. 1. VSCF Generating System Block Diagram

A common rule of thumb in airplane design says that removing one pound of weight can actually reduce the overall weight by at least five pounds because of all the

extra structure and fuel that is no longer needed to carry that pound over the range of the plane. This reduction in weight means the plane needs less fuel to travel the same distance so that the aircraft is more economical to operate. Since saving weight is so important to reducing the costs of an airplane, the use of smaller and lighter 400 Hz electrical generators is a significant advantage over 50 Hz electrical systems.

In the VSCF, the generator input is coupled directly to the raw, variable source speed of the engine drive-shaft; thus, resulting in a electrical output of variable frequency which is then fed into solid state PCU - containing both power electronics and the necessary control units. The PCU subsequently processes its variable frequency input power to generate a synthesized, 400 Hz constant frequency output.

Fig.1 shows the general topology of a DC-link type of VSCF system, in which wild frequency power is rectified and re-inverted to produce 400Hz. Fig. 2 shows the Power circuit of the Resonant DC Link Inverter. Here the capacitor (C_f) in the circuit is the energy storing capacitor. The diode-bridge and the inductor are used for pre-charging. Once charging is done, this part of the circuit is opened using a mechanical switch. The capacitor voltage is sampled through a Hall-effect Voltage transducer and this is given to the controller circuit. This signal is given to the current regulator circuit such that current regulator provides the required current. Current Initialization is carried as described in current initialization circuit for Zero Voltage Switching (ZVS) purpose [17].

III. TECHNOLOGICAL REVIEW

This section reviews the technological issues pertinent to the fundamental areas of inverter design.

A. Soft-Switching Inverter

Either the voltage over or the current through the power switching devices is clamped low or to zero during switching transient periods – refers to the use of resonant techniques. Resonant switching schemes of which there are many [4 - 7], are all capable, at least in principle, of reducing the switching losses significantly. The perceived key, generic benefits over the conventional hard-switching may be summarized as follows:

- Lower switching losses
- Shoot-through problems due to high dv/dt are reduced
- The need for snubbers disappears
- Device SOA is not a limiting factor
- Better spectral performance
- Improved device utilization
- Lower sensitivity to system and packaging parasitics.

B. Resonant DC Link Inverters

Resonant dc link inverters promise marked gains for adjustable speed drives, power supplies and active filtering applications. Among the various types of resonant links, the parallel resonant DC link is quite attractive for implementing zero voltage switching (ZVS) [3]. This is based on shunt resonance. This inverter is quite simple in the sense that it needs a minimum number of devices, it is easy to implement and requires simple control. Compared to a regular pulse width modulated (PWM) inverter this inverter requires an additional resonant inductor and a resonant capacitor. The resonant circuit is connected between dc source and the inverter so that the input voltage to the inverter oscillates between zero and to a value that is slightly greater than twice the dc bus voltage. An important consideration for successful operation of RDCLI is that there should not be any zero crossing failure, as link voltage (i.e., voltage across the capacitor C) must go to zero at the end of every resonant cycle for zero voltage switching.

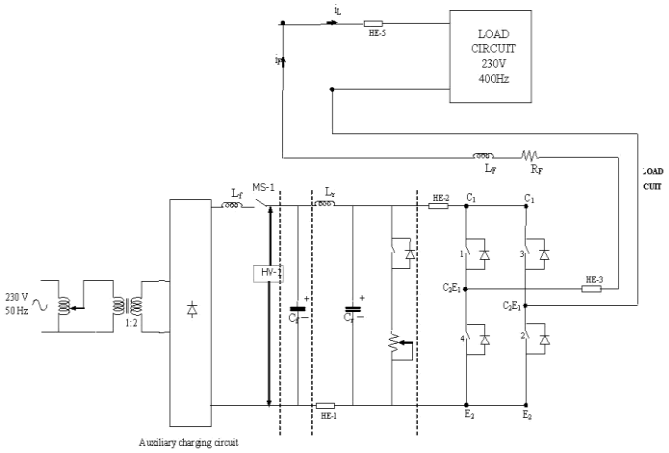

Fig. 2. Power Circuit of Resonant DC link Inverter

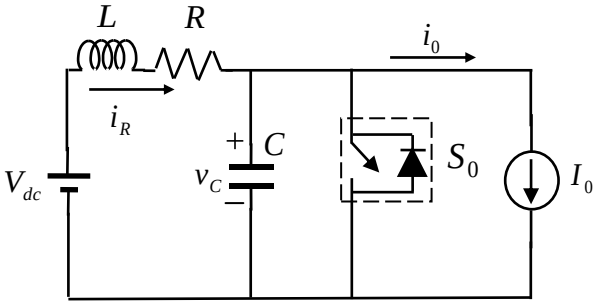

Fig. 3. Equivalent circuit of an RDCLI

This is easily achieved if the resonant inductor L has infinite Q factor. In such a case the circuit will oscillate between zero and $2V_{dc}$ with a frequency of $1/2\pi\sqrt{LC}$ Hz. However, in practice an inductor with infinite Q cannot be obtained. Even high quality inductors will have a Q factor around 150 to 200. Zero crossing of the resonant link DC voltage is mandatory in every resonant cycle for successful operation of the inverter. Failure of resonant link tends to occur because of the finite Q of the resonant circuit where the capacitor voltage tends to build up in successive resonant cycles. Therefore an appropriate initial current must be built up in the inverter which would then ensure a zero crossing of the voltage. This must be done in every resonant cycle. The built up of fixed initial inductor current is adopted to ensure zero crossing in every resonant cycle in [3]. However, the initial current is a function of the inverter input current, which depends upon the load current of the inverter. In a practical circuit, the load current would fluctuate and hence the load current seen by the resonant link can be bi-directional. Thus using a fixed initial inductor current concept would not ensure zero crossing in every resonant cycle unless this current is designed on the worst case basis. This approach however would aggravate the

voltage overshoot problem. A programmable initial current control technique for RDCLI was reported in [11-12]. This scheme is somewhat complex from the implementation viewpoint. A current prediction scheme is proposed in [8] for finding out the initial current. The functioning of the link depends on the detection of the zero crossing of the resonant capacitor. This scheme requires a sensitive detection of zero voltage crossing.

In this paper we present the control aspects of RDCLI for current initialization technique [13, 14, 17] which ensures reliable zero voltage switching and Control of current within the Inverter. The proposed method is based on state transition equation and is simple to implement.

The equivalent circuit of a RDCLI is shown in Fig. 3. This contains a resonant circuit generated by an inductor (L) and a capacitor (C) as shown in this figure. The inductor coil has a resistance (R) due to its finite Q-factor. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The switch S_0 shown in Fig. 3 represents the switch across the link. This switch is required to short the link when the voltage v_C is zero for the current i_R to build up. The current i_0 is the input current of the inverter, this act as the load current for the resonant link. It is assumed that the current i_0 remains constant during a resonant oscillation period. Therefore this current is indicated by the current source I_0.

The philosophy is to switch the device only when the voltage across it is zero. For a given set of resonant link parameters, a constant resonant oscillation period is selected. The state vector consists of link capacitor voltage (V_C) and inductor current (i_R) in Fig. 3. The capacitor voltage must be zero at the start and at the end of every resonant oscillation period for successful ZVS. With this condition, the exact initial value of the inductor current (i_R) is determined. In order to start a resonant cycle with this value of the initial current, the time duration for which the dc bus must be shorted can be calculated. Thus, the initial inductor current is generated by shorting the link and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. This forces the link capacitor voltage to return to zero after a pre-specified resonant oscillation period.

The philosophy of using this soft-switched inverter is to obtain a high current regulator bandwidth as desired. This topology would offer adequate current regulator bandwidth for compensating higher order harmonics because of high frequency switching. Furthermore, this compensator can achieve high efficiency by reducing switching losses. Moreover, the transient response is fast and the control is simple.

The control of RDCLI is different from the conventional PWM inverter. The switching of the devices is carried out when the voltage across the link is zero to achieve ZVS. The current control in this inverter is done through zero-hysteresis bang-bang control. The basic difference from the PWM schemes is the existence of pre-specified permitted switching instants. No computations are necessary for specifying a pulse width. The only decision that needs to be made is which inverter state is to be selected. This decision can be made based on current error (feedback signal). The inverter state selection is done to achieve current regulation objectives.

IV. CURRENT INTIALIZATION SCHEME

The proposed current initialization scheme [17] is explained with the help of waveform of capacitor voltage V_C and link current i_R as shown in Fig. 4. The resonant cycle starts at time t_0 and ends at time t_1. Similarly, the next resonant cycle starts at t_2 and ends at t_3. To ensure that no zero-crossing failure occurs at t_3, the current through the inductor L must be built up to the required value. The choice of the interval $(t_2 - t_1)$ depends on this requirement which, in turn, depends on the output current i_0 and the input dc voltage V_{dC} of the inverter. The instant t_2 is so chosen that the current at this instant is sufficient to bring the capacitor voltage zero again after a resonant cycle.

In this scheme the duration $(t_3 - t_2)$ is fixed at ΔT μs. Here, the initial inductor current is generated by shorting S_0 in Fig. 3, and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. Thus the link capacitor voltage would return to zero after the pre-specified resonant oscillation period ΔT. Fig. 5 shows curve (e.g., t_0 to t_1) takes the fixed pre-specified time. The state-plane trajectory where the transition along the vertical axis ($V_C \cong 0$) takes a variable time (e.g., t_0 to t_1) depending on the load current. It is to be noted that the particular value of ΔT chosen depends on the parameters of the resonant circuit. Since a resonant cycle time is much smaller than the time constant of the load circuit, the load current is assumed to be a constant current equal to I_0 over a particular resonant cycle, i.e., between $\Delta T = t_3 - t_2$.

Referring to Fig. 3, let us define a state vector as $x = \begin{bmatrix} v_c & i_R \end{bmatrix}^T$ and an input vector as $u = \begin{bmatrix} I_0 & V_{dc} \end{bmatrix}^T$. The state space equation of the circuit is then given by

$$\dot{x} = Ax + Bu \qquad (1)$$

Where the matrices A and B are given by

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & -R/L \end{bmatrix}, \qquad B = \begin{bmatrix} -1/C & 0 \\ 0 & 1/L \end{bmatrix}$$

The solution of (1) at instant t_3 based on the initial condition at instant t_2 is given by

$$x(t_3) = e^{A\Delta T} x(t_0) + \int_0^{\Delta T} e^{A(\Delta T - \tau)} Bu(\tau) d\tau \qquad (2)$$

It is to be noted that in the above equation V_{dC} is constant and I_0 is assumed to be known and constant. Also noting that capacitor voltage must be equal to zero at instant t_3, defining a row vector C as $C = \begin{bmatrix} 1 & 0 \end{bmatrix}$, we can write from (2)

$$0 = C \left[\phi x(t_2) + \theta u(t_2) \right] \qquad (3)$$

Where $\phi = e^{A\Delta T}$ and $\theta = \int_0^{\Delta T} e^{A(\Delta T - \tau)} B d\tau$.

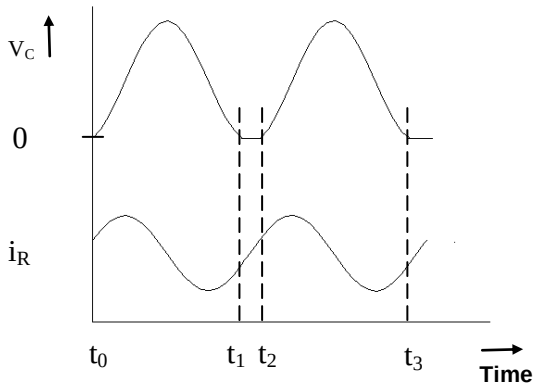

Fig. 4. Link voltage and link current waveform

Note that since *A*, *B* and ΔT are known a priori, the matrices ϕ and θ can be numerically evaluated. The state plane trajectory under this boundary value problem is shown Fig. 5 where V_C is assumed to be approximately zero when S_0 is closed. We can expand equation (3) as

$$0 = \begin{bmatrix}\phi_{11} & \phi_{12}\end{bmatrix}\underline{x}(t_2) + \begin{bmatrix}\theta_{11} & \theta_{12}\end{bmatrix}\underline{u}(t_2)$$

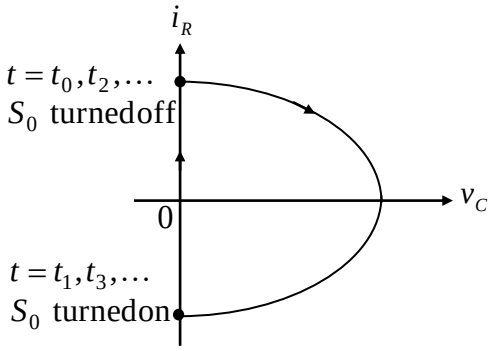

Fig. 5. State Plane Diagram of link voltage and current

Where the subscripts 11 and 12 indicate the particular elements of these matrices. Again from Fig. 4 we get $x^T(t_2) = \begin{bmatrix} i_R(t_2) & \cdot \end{bmatrix}$. Substituting in the above equation and rearranging we get

$$i_R(t_2) = -\frac{1}{\phi_{21}}\begin{bmatrix}\theta_{11} I_0 + \theta_{21} V_{dc}\end{bmatrix} \qquad (4)$$

The above value of current at instant t_2 required to ensure zero crossing of the voltage at instant t_3. Once $i_R(t_2)$ is obtained the time for which the capacitor should be shorted. The computed value of current $i_R(t_2)$, obtained from equation (4), with the actual value link current i_R. The switch S_0 is opened when these two values are equal. This ensures that the link current is built up to the required level of initial current such that the link voltage goes to zero at instant t_3, i.e., at the end of next resonant cycle. A block schematic of the implementation scheme is shown in Fig. 6 and is discussed in [17]. An elaborated strategy along with the hardware components required is discussed below.

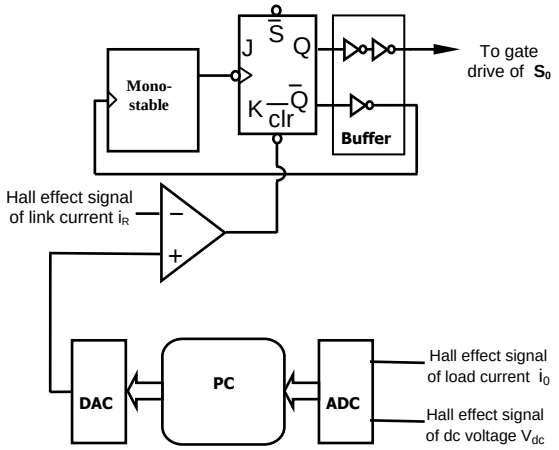

Fig. 6. Block diagram of current initialization

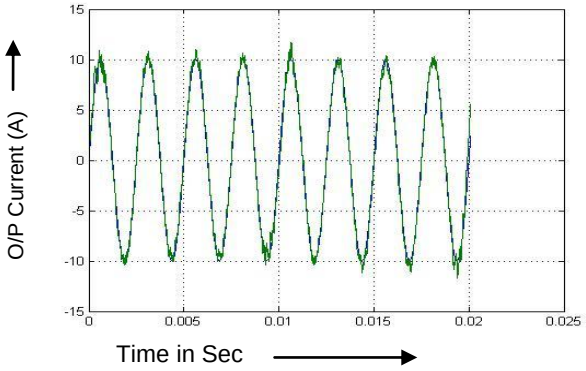

Fig. 7. Output Current Vs. Time

Parameters: L = 26μH, C = 0.94μF, V_{dc}= 400V
Load: R=0.2 Ohms, L=15mH, Voltage = 325sin(2512t)

With these values of inductor and capacitor the un-damped oscillation time is 31.1 μs. Therefore, the resonant cycle time ΔT is chosen to be 26.1 μs taking into account the finite Q-factor of the coil.

The block diagram of the proposed current initialization scheme is shown in Fig. 6. The corresponding control circuit is shown in Fig. 8. A personal computer (PC) along with its associated high-speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC) is used for the computation of the initial current from equation (4). In this equation θ_{11}, θ_{21} and ϕ_{21} are constants that are dependent on the circuit parameters and the time ΔT. These are pre-computed and stored. The load current (I_0) and the dc voltage V_{dc} are measured through Hall-effect sensors (HE-1 and HV-1 respectively in Fig. 2) at the start of every resonant cycle (e.g. t_2 in Fig. 5) and are converted through ADC. These measured values along with the constants mentioned above are used for the computation of the initial current. This process is repeated for every resonant cycle. It is to be noted that the computation here is fairly simple and can also be achieved through a hardware configuration. However, the use of PC makes the control circuit much more flexible than a hardwired circuit. Furthermore, due to the presence of the PC, the delays and tolerances of the actual circuit can also be taken into account. An accurate zero-voltage switching can be obtained in the experiment.

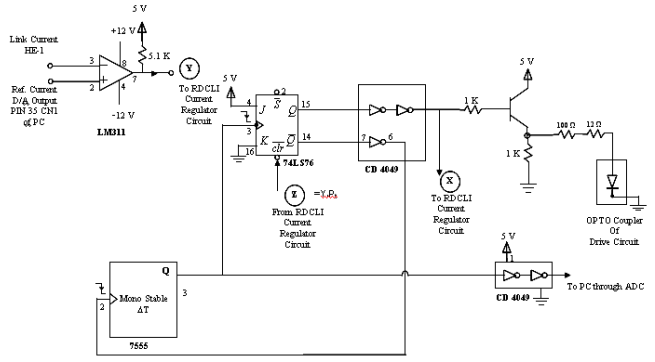

Fig. 8. Resonant dc link control circuit

As soon as the required initial current is computed in the PC, it is converted into an Analog signal through a DAC. The computation time required is much smaller than the resonant cycle time *ΔT*. This signal is then available to the comparator for comparison with the actual link current. The link current is monitored continuously through a Hall-effect current sensor (HE-1 shown in Fig. 2). Let us discuss the operation of the circuit in Fig. 8. When the link current becomes equal to the required initial current, the comparator output (Y) becomes zero. The signal Y is conditioned by protection circuit (Fig. 9) and then the output Z= Y P_t is used for clearing the J-K flip-flop (Fig. 8). Under normal condition Z = Y, as protection signal P_t = 1. Once this flip-flop is cleared, its output (*Q*) becomes zero and $\overline{Q}$ becomes one. This is then used for switching off S_0 through a buffer. Simultaneously, the inverted output ($\overline{Q}$) of the J-K flip-flop is used for triggering the mono-stable (Fig. 8) through an inverting buffer. The mono-stable timing is designed for a pulse-width of ΔT. After this time elapses, the negative going edge of the mono-stable output is used to clock the J-K flip-flop. This force the output of the flip-flop to one and consequently the shorting switch S_0 is turned on.

Through the above scheme, the zero-voltage switching is obtained. It is to be noted that during the time when S_0 is on, the switching transitions of the switches $S_1 - S_4$ take place. To ensure that the switches $S_1 - S_4$ are turned on or off only during this prescribed interval, the gating of $S_1 - S_4$ are conditioned by the output *Q* of the J-K flip-flop. Further note that the configuration of the switches $S_1 - S_4$ at a particular resonant cycle is dependent on the load connected to the output of the inverter. It is to be noted that the J-K flip-flop is cleared under two conditions. One is the usual clearing as explained already in every resonant cycle. The other is under fault condition. If there is a fault, the resonant circuit must be stopped. In that case the protection circuit gives P_t = 0 and signal Z is forced to zero. The switch S_0 is therefore opened permanently so that the link voltage and link current will gradually decay to zero due to the internal resistance of the resonant coil. The output of the mono-stable is also used for the starting ADC. When this is triggered through $\overline{Q}$, its output goes high. This is also the onset of the resonant cycle. This positive going edge (through buffer) is used as a signal to the PC interface card such that the ADC starts sampling I_0 and V_{DC}.

V. CURRENT REGULATOR CIRCUIT

The current regulator control circuit is shown in Fig. 9. The switching of the devices is synchronized to the zero crossings of the link voltage so as to obtain ZVS. The resonant dc link inverter and controller are configured to regulate its current so as to match the current reference. As mentioned earlier the mono-stable of Fig. 8 is triggered at the onset of a resonant cycle. This then goes zero after *ΔT* μs elapses. The negative going edge of the mono-stable output is used for clocking the J-K flip-flop. This force the output of the flip-flop to one and consequently the shorting switch S_0 is turned on.

The same signal is used to clock the D-flip-flop in Fig. 9 so that the synchronization is obtained. The comparator compares the actual inverter current (HE-III) with the reference of the inverter. Based on the output of the comparator, a switching decision has to be taken. This output is fed to the D input of the D latch. However, the output of the D flip-flop remains unaltered till the next sampling point is reached. The sampling point is the point when resonant link voltage goes zero. At this sampling point if the output current is lower, then a positive pulse is given to increase the output current and vice-versa. However, this pulse is not directly given as seen in Fig. 9. It is ensured that the outgoing switches are turned off first and then the incoming switches are turned on. This is achieved via mono-stable and AND gate. Therefore a change from 0 to 1 in the D Flipflop output is delayed by 1 μs where as a change from 1 to 0 in the D Flip-flop output is passed immediately.

For the protection of both resonant link and the current regulator a protection scheme is devised in this circuit. The load current is not allowed to be more than 4 A in either direction. This is done via two comparators. One comparator is set at 4 A and the other comparator is set at - 4 A. The actual current in the load circuit is compared with these references. Once the current is beyond limits of ± 4 A, one of the comparator output goes zero. This is then used for clocking a negative edge triggered J-K flip-flop. Therefore under normal conditions the $\overline{Q}$ output (P_t) of this J-K will be 1, this will go zero the moment current limit exceeds. This signal is used for blocking the gate signals. Manual resetting of the J-K flip-flop is required to clear the fault.

The signals derived for switches $S_1 - S_4$ are transmitted for gate drive circuit after being ANDed with current limit control signals. There is also a manual start/stop switch through which the circuit can be stopped at any time. The gating signals are also ANDed with the start/stop signals. Therefore under normal conditions the signals for switches $S_1 - S_4$ are passed immediately.

But under fault conditions these signals are blocked. This is achieved through AND gates. The comparator output obtained from resonant link control circuit is also ANDed with this current limit control. In the event of a fault the J-K in current initialization circuit is cleared so that the switch S_0 is opened.

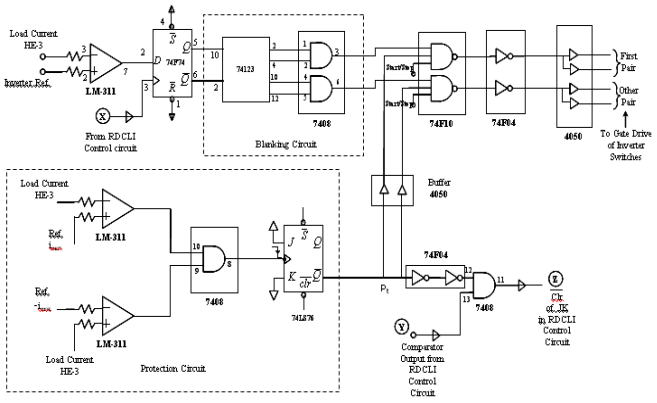

Fig. 9. RDCLI current regulator circuit

Since there is no notion of hysteresis band in this case, we will call this as zero-hysteresis bang-bang current control. Fig. 7 shows the waveform of load current that is operating at 400 Hz. It is clear that waveform is nearly sinusoidal and FFT confirms that THD is 2.2 % which satisfies IEEE specifications.

VI. CONCLUSIONS

A new current initialization scheme for resonant dc link inverter is presented in this paper. This initialization scheme is based on boundary value problem. It is shown that that this current can be predicted very accurately which in turn ensures the zero-crossing of the link voltage at a prescribed time instant. The proposed power supply is subjected to support a 400 Hz load and the performance is found to be excellent in terms of quality and THD. Zero-hysteresis bang-bang controller is used for current control within the inverter and hardware implementation of the same is presented and it is found that the proposed solution works nicely. The proposed scheme is validated through extensive simulation studies.

VII. REFERENCES

[1] S. M. Iden, A. Morris, "*High Reliability Aircraft Generator System*." Proc. of the Aerospace Technology Conference. Exp. Anaheim CA, Oct. 3-6, 1988, pp. 69-74.

[2] Jahns, T.M., De Doncker, R. W., Turnbull, F. G., Radun, A. V., and Szczesny, P. M., "*System design considerations for a high-power aerospace resonant link converter*."In Proceedings of Applied Power Electronics Conference, Boston, Feb. 1992, 665-673.

[3] Divan, "*The Resonant DC Link Converter – A New Concept in Static Power Conversion*", 1986 IEEE-IAS Annual Meeting Record, pp 648-665.

[4] Divan and G. Skibinski, "*Zero switching loss inverters for high power applications*." 1987 IEEE-IAS Annual Meeting Record, pp. 627-634.

[5] He and N. Mohan, "*Parallel DC Link Circuit – A Novel Zero Switching loss Topology with Minimum Voltage Stresses*." 1991 IEEE Transactions of Power Electronics, Vol. 6, Number 4, pp.687-694.

[6] He and N. Mohan, W Wold "*Zero Voltage Switching PWM Inverter for High Frequency DC-AC Power Conversion*" 1990 IEEE-IAS Annual Meeting Record, pp. 1215-1221.

[7] Venkataramanan and D. M. Divan, "*Pulse width Modulation With Resonant DC Link Converters*" 1990 IEEE-IAS Annual Meeting Record, VOL.II, pp. 984-990.

[8] Vijay V. Deshpande, Seshagiri Rao Doradlaand Deepakraj M. Divan, " *A Current- Prediction Scheme for PRDCL Inverter-Fed Induction Motor Drive*," IEEE Transaction on Power Electronics, Vol. 12, no.1, pp. 64- 70., 1997

[9] D. M. Divan and Giri Venkataramanan, "*Comparative Evaluation of Switching Inverter Topologies*." Proc. of the European Power Elctronics Conf., Vol. 2, pp. 13-18, 3-6 Sept. 1991.

[10] J. Flnney, T.C. Green, B. W. Williams, "*Review of the Resonant Link Topologies for Inverters*." IEE Proceedings-B, Vol. 140, No. 2, March 1993.

[11] J. S. Lai and B. K. Bose, "*An Improved Resonant DC Link Inverter for Induction Motor Drives*," Proceedings of Conf. Rec. IEEE/IAS Annual Meeting}, pp. 742-748, 1988.

[12] J. S. Lai and B. K. Bose, "*An Induction Motor Drive Using High Frequency Resonant DC Link Inverter,",IEEE Transaction on Power Electronics*, Vol. 6, no.3, pp. 504-513., 1991

[13] K. K. Mahapatra. A. Ghosh and S. R. Doradla, "*Improved active harmonic current compensation of power electronic load using resonant dc link inverter*," The Journal of Indian Institute of Science, vol. 77, pp. 585-595, Nov-Dec. 1997.

[14] K. K. Mahapatra. A. Ghosh and S. R. Doradla, "*Active harmonic current compensation of Industrial loads using resonant dc link inverter*," Proceedings of NPSC 96, pp-634-639, Allied Publishers Limited, India, 1996.

[15] White GW and Miller TJE [1995] *Soft switching in aircraft power conversion systems*, IEE Colloquium on Resonant Systems, London, 1995.

[16] T. M. Jahns, M. A. Maldonado "*A New Resonant Link Aircraft Power Generating System.*" Proc. of the 26th Intersociety Energy Conservation Engineering Conf. 1991, pp. 13-19.

[17] S. K. Pattnaik, K. K. Mahapatra "*Aircraft Power Supply Design using Soft-switched Inverter"* Proc. of Computational Intelligence, Control and Computer Vision in Robotics & Automation Conf., 2008, pp. 180-185.