Aircraft Power Supply Design using Soft-Switched Inverter

Sushant Kumar Pattnaik and K. K. Mahapatra
Department of Electronics & Communication Engineering, N.I.T. Rourkela

Abstract--**This paper describes the design of an aircraft power supply. Power supply design is done using a soft-switched Resonant DC Link Inverter (RDCLI). A novel current initialization scheme is adopted to avoid zero crossing failures. Zero-hysteresis bang-bang control is used for current control within the inverter. The designed power supply supports 400 Hz load. The soft-switched inverter provides adequate current regulator bandwidth besides reducing switching losses. The proposed solution is validated through extensive simulation.**

Index Terms--**Aircraft System, Soft-Switching Inverter, PWM (Pulse Width Modulation), ZVS (Zero Voltage Switching), RDCLI (Resonant DC Link Inverter).**

I. INTRODUCTION

In the future, the Aircraft will tend to use electrical power rather than hydraulic, pneumatic or mechanical power. This will increase the demands on the electrical power systems, and it is an open question as to how far advanced power electronics will assist in their viable realization. The application areas most closely associated with this transition are Variable Speed Constant Frequency (VSCF) power conversion, Electro-hydraulic/-mechanical Actuation (EHAEMA), and Fuel Pumps. At the core of each is a power electronics inverter, with key functional issues being: high frequency operation, reliability, fault tolerance, power waveform quality, elevated temperature operation, and EMI regulation compliance.

One of the absolutely fundamental questions in current research and development of suitable power electronic inverter are the choice of circuit topology. In particular, the circuit can be either “hard-switched" or "soft-switched", and there are innumerable variants of both types: hence, the variant best suited to the associated application is to be determined.

A 400 Hz Aircraft power generating system is introduced which has been designed to achieve significant improvements in power density and reliability. At the heart of the new variable speed constant-frequency (VSCF) configuration is a high-frequency resonant link inverter designed so that all inverter switching occurs under zero-voltage conditions. Advantages include minimization of switching losses and significant reductions in power device switching and electromagnetic interference (EMI) generation.

II. AIRCRAFT SYSTEMS

Objectives inherent in the design of Aircraft suitable systems are increases in reliability, power density, system flexibility, and maintainability combined with a reduction in the cost of ownership. These issues are perhaps clearer in the mergence of the power electronic conversion stage known as VSCF system. A generic VSCF system entails both a Generator and a solid-state Power Conditioning Unit (PCU). Generation and distribution of 400 Hz power has hitherto been recognized as the accepted aerospace standard for applications requiring power installation exceeding several tens of KVA. The reason of using 400 Hz (Standard practice dictates that it should be 8 times of the line frequency i.e., 50 Hz) is, if we increase the frequency, then it is obvious that flux would decrease, which is verified from the transformer equation $V = 4.44 f \phi T$. From this equation one can easily understand that if we increase the frequency, the sizes of the load that are connected across the power supply are reduced. Generally in an aircraft, there are many number of loads (motors, compressors, etc...) connected. Hence more space is created.

The conventional method for producing the required constant frequency power is to feed the drive (engine) output to the electrical generator via a gear-box. This transmission (electro- or hydro-mechanical) stage receives speeds over a range of 1.5:1 to 3:1 – being engine type dependent and transmits a constant speed to the generator, thus enabling the latter to generate a regulated 400 Hz power. Most aircraft in use presently still employ such Constant Speed Drives (CSDs), and variations thereof, at the heart of their Electronic Power Generating and Conditioning Systems.

In the VSCF, the generator input is coupled directly to the raw, variable source speed of the engine drive-shaft; thus, resulting in a electrical output of variable frequency which is then fed into solid state PCU - containing both power electronics and the necessary control units. The PCU subsequently processes its variable frequency input power to generate a synthesized, 400 Hz constant frequency output.

The PCUs have evolved and have been realized through two main approaches, cyclo-converter and DC-Link Inverter. Successful deployment of both approaches can be found in current aerospace applications. The cyclo-converter uses power switches to convert the varying AC input directly to the required 400 Hz output. The DC-Link has an intermediate rectifying stage which rectifies the AC input to form a Voltage DC link into an inverter stage which is designed and controlled to reconstruct, or synthesize, the required output.

Comparing the two approaches, the cyclo-converter has a higher power-switch count, greater complexity of both control

and required generator. The DC-Link, and variations thereof, is the primary solid-state alternative to the conventional CSD approach [1].

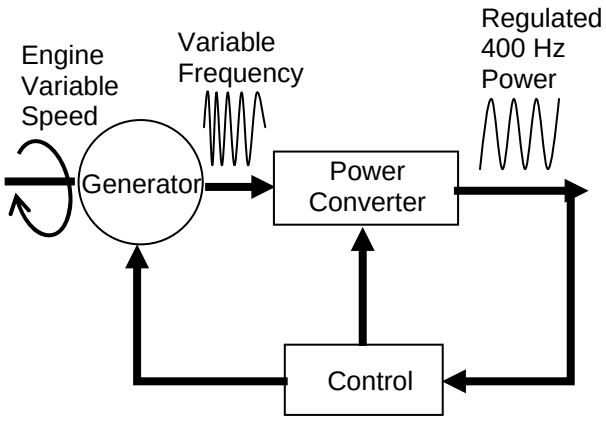

Fig 1. VSCF Generating System Block Diagram

Fig 1. shows the general topology of a DC-link type of VSCF system, in which wild frequency power is rectified and re-inverted to produce 400Hz. The constituent elements can be divided into separate entities which may then be independently situated throughout the aircraft. The DC-link VSCF also provides easy access to Variable Frequency (VF), and Fixed Frequency (FF) which, therefore, enables power to be supplied in a form – VF, DC or FF - best suited to the aircraft application; the attraction of which being further weight reduction[2].

III. TECHNOLOGICAL REVIEW

This section reviews the technological issues pertinent to the fundamental areas of inverter design i.e. choice if circuit topology. In particular, the circuit can be either "hard-switched" or "soft-switched".

A. Inverter Concepts.

A.1. Conventional

Conventional refers in particular to the DC voltage source inverter, where the inverter (DC to AC) is supplied by a fixed dc voltage and its primary power switches are subjected to hard- or stressed-switching; i.e. they have to support rated voltage and current simultaneously during the switching transient periods – hence, otherwise known as the Hard-switched Inverter. Both the synthesized ac output voltage and frequency are controlled by using pulse-width-modulation (PWM) techniques.

The major appeal of the conventional VSI is its simple power structure, minimal number of power switching devices, and very high resolution pulse width control. However, shortcomings are recognized and summarized – as follows:

- Stressful switching behavior of the power electronic devices
- During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, which results in high switching losses and stress
- Dissipative passive snubbers are added to power ckts so that the *dv/dt & di/dt* of the power devices can be reduced, and the switching loss and stress can be diverted to the passive snubber ckt.
- Switching loss is proportional to switching frequency, thus limiting the maximum switching frequency of the power converter.
- EMI due to high *di/dt and dv/dt*
- Large dc link filter
- Acoustic noise is generated because switching frequency lies in the audible range
- Reduced reliability due to higher heat-sink temperature

Pursuing the objective of increasing the switching frequency (f_s) in order to improve the output waveform quality and reduce the weight and volume of the passive components merely exacerbates, directly or indirectly, all of the listed shortcomings. An increase in f_s is only feasible if the power loss over each switching transient period can be reduced; i.e. limit the level of simultaneous current and voltage imposed on the power switches. The classical approach uses rather inefficient snubbers, but an alternative, aimed at achieving zero voltage or zero current during the switching interval – Zero Voltage or Current Switching (ZVS or ZCS) – offers greater appeal.

A.2 Soft-Switching Inverter

The advanced means of achieving soft-switching where either the voltage over or the current through the power switching devices is clamped low or to zero during switching transient periods – refers to the use of resonant techniques. Resonant switching schemes of which there are many [4]-[7], are all capable, at least in principle, of reducing the switching losses significantly. The perceived key, generic benefits over the conventional hard-switching may be summarized as follows:

- Lower switching losses
- Shoot-through problems due to high dv/dt are reduced
- The need for snubbers disappears
- Device SOA is not a limiting factor
- Better spectral performance
- Improved device utilization
- Lower sensitivity to system and packaging parasitics.

This simple topology however has few drawbacks. These are higher device voltage stresses (when the output voltage is greater than twice the dc input voltage), zero crossing failure unless the initial current in the resonant inductor is built properly. The voltage overshoot problem can be overcome by using actively clamped RDCLI [4]. Through clamping it is possible to limit the voltage stresses of the inverter devices to 1.3 to 1.8 times the dc voltage. The actively clamped RDCLI circuit however has few disadvantages. The link frequency varies with variation in the dc link voltage. This manifests itself in large current jumps. This topology increases losses due to introduction of the clamping circuit. The additional

clamping device increases the complexity of the power circuit and the control circuit. Moreover, the control of the clamping device becomes extremely difficult at high frequencies [8].

The choice of specific converter topology becomes one of the most important factors influencing final system power density, reliability, and cost.. There are various ways of classifying these inverters [9,10]; After evaluating alternatives, the Resonant DC Link Inverters (RDCLI) topology is selected as the most promising configuration for development to meet program objectives.

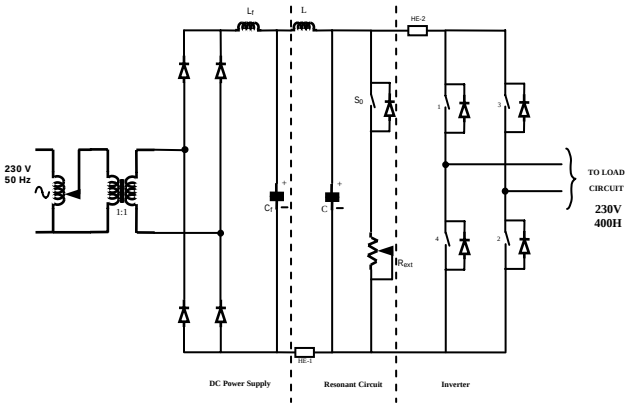

Fig 2. Power Circuit of Resonant DC link Inverter

B. Resonant DC Link Inverters

Resonant dc link inverters promise marked gains for adjustable speed drives, power supplies and active filtering applications. Among the various types of resonant links, the parallel resonant DC link is quite attractive for implementing zero voltage switching (ZVS) [3]. This is based on shunt resonance. This inverter is quite simple in the sense that it needs a minimum number of devices, it is easy to implement and requires simple control. Compared to a regular pulse width modulated (PWM) inverter this inverter requires an additional resonant inductor and a resonant capacitor. The resonant circuit is connected between dc source and the inverter so that the input voltage to the inverter oscillates between zero and to a value that is slightly greater than twice the dc bus voltage. An important consideration for successful operation of RDCLI is that there should not be any zero crossing failure, as link voltage (i.e., voltage across the capacitor C) must go to zero at the end of every resonant cycle for zero voltage switching. This is easily achieved if the resonant inductor L has infinite Q factor. In such a case the circuit will oscillate between zero and 2Vdc with a frequency of $1/2\pi\sqrt{LC}$ Hz. However, in practice an inductor with infinite Q cannot be obtained. Even high quality inductors will have a Q factor around 150 to 200. Zero crossing of the resonant link DC voltage is mandatory in every resonant cycle for successful operation of the inverter. Failure of resonant link tends to occur because of the finite Q of the resonant circuit where

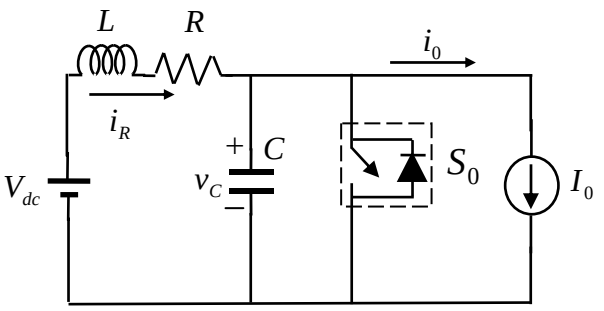

Fig. 3 Equivalent circuit of an RDCLI

the capacitor voltage tends to build up in successive resonant cycles. Therefore an appropriate initial current must be built up in the inverter which would then ensure a zero crossing of the voltage. This must be done in every resonant cycle. The built up of fixed initial inductor current is adopted to ensure zero crossing in every resonant cycle in [3]. However, the initial current is a function of the inverter input current, which depends upon the load current of the inverter. In a practical circuit, the load current would fluctuate and hence the load current seen by the resonant link can be bi-directional. Thus using a fixed initial inductor current concept would not ensure zero crossing in every resonant cycle unless this current is designed on the worst case basis. This approach however would aggravate the voltage overshoot problem. A programmable initial current control technique for RDCLI was reported in [11-12]. This scheme is somewhat complex from the implementation viewpoint. A current prediction scheme is proposed in [8] for finding out the initial current. The functioning of the link depends on the detection of the zero crossing of the resonant capacitor. This scheme requires a sensitive detection of zero voltage crossing.

In this paper we present a new current initialization technique [13, 14] for the resonant circuit which ensures reliable zero voltage switching. The proposed method is based on state transition equation and is simple to implement. The equivalent circuit of a RDCLI is shown in Fig. 3. This contains a resonant circuit generated by an inductor (L) and a capacitor (C) as shown in this figure. The inductor coil has a resistance (R) due to its finite Q-factor. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The switch S_0 shown in Fig. 3 represents the switch across the link. This switch is required to short the link when the voltage v_C is zero for the current i_R to build up. The current i_0 is the input current of the inverter, this act as the load current for the resonant link. It is assumed that the current i_0 remains constant during a resonant oscillation period. Therefore this current is indicated by the current source I_0.

The philosophy is to switch the device only when the voltage across it is zero. For a given set of resonant link parameters, a constant resonant oscillation period is selected. The state vector consists of link capacitor voltage (V_C) and inductor current (i_R) in Fig. 3. The capacitor voltage must be

zero at the start and at the end of every resonant oscillation period for successful ZVS. With this condition, the exact initial value of the inductor current (i_R) is determined. In order to start a resonant cycle with this value of the initial current, the time duration for which the dc bus must be shorted can be calculated. Thus, the initial inductor current is generated by shorting the link and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. This forces the link capacitor voltage to return to zero after a pre-specified resonant oscillation period.

The philosophy of using this soft-switched inverter is to obtain a high current regulator bandwidth as desired. This topology would offer adequate current regulator bandwidth for compensating higher order harmonics because of high frequency switching. Furthermore, this compensator can achieve high efficiency by reducing switching losses. Moreover, the transient response is fast and the control is simple.

The control of RDCLI is different from the conventional PWM inverter. The switching of the devices is carried out when the voltage across the link is zero to achieve ZVS. The current control in this inverter is done through zero-hysteresis bang-bang control. The basic difference from the PWM schemes is the existence of pre-specified permitted switching instants. No computations are necessary for specifying a pulse width. The only decision that needs to be made is which inverter state is to be selected. This decision can be made based on current error (feedback signal). The inverter state selection is done to achieve current regulation objectives.

IV. CURRENT INTIALIZATION SCHEME

The proposed current initialization scheme is explained with the help of waveform of capacitor voltage V_C and link current i_R as shown in Fig. 4. The resonant cycle starts at time t_0 and ends at time t_1. Similarly, the next resonant cycle starts at t_2 and ends at t_3. To ensure that no zero-crossing failure occurs at t_3, the current through the inductor L must be built up to the required value. The choice of the interval $(t_2 - t_1)$ depends on this requirement which, in turn, depends on the output current i_0 and the input dc voltage V_{dC} of the inverter. The instant t_2 is so chosen that the current at this instant is sufficient to bring the capacitor voltage zero again after a resonant cycle.

In this paper we propose a scheme in which the duration $(t_3 - t_2)$ is fixed at ΔT microseconds. Here, the initial inductor current is generated by shorting S_0 in Fig. 3, and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. Thus the link capacitor voltage would return to zero after the pre-specified resonant oscillation period ΔT. Fig. 5 shows curve (e.g., t_0 to t_1) takes the fixed pre-specified time. The state-plane trajectory where the transition along the The transition along the vertical axis ($V_C \cong 0$) takes a variable time (e.g., t_0 to t_1) depending on the load current. It is to be noted that the particular value of ΔT chosen depends on the parameters of the resonant circuit. Since a resonant cycle time is much smaller than the time constant of the load circuit, the load current is assumed to be a constant current equal to I_0 over a particular resonant cycle, i.e., between $\Delta T = t_3 - t_2$.

Referring to Fig. 3, let us define a state vector as $x = \begin{bmatrix} v_c & i_R \end{bmatrix}^T$ and an input vector as $u = \begin{bmatrix} I_0 & V_{dc} \end{bmatrix}^T$. The state space equation of the circuit is then given by

$$\dot{x} = Ax + Bu \tag{1}$$

where the matrices A and B are given by

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & -R/L \end{bmatrix}, \qquad B = \begin{bmatrix} -1/C & 0 \\ 0 & 1/L \end{bmatrix}$$

The solution of (1) at instant t_3 based on the initial condition at instant t_2 is given by

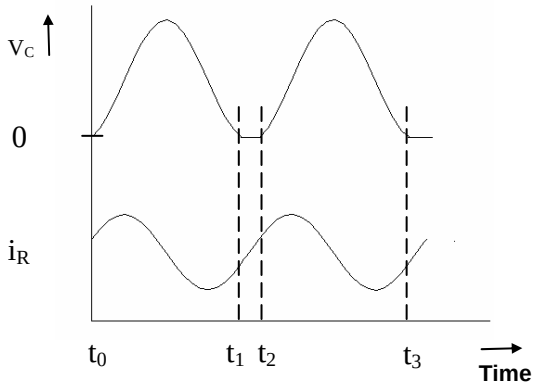

Fig 4. Link voltage and link current waveform

$$x(t_3) = e^{A\Delta T} x(t_0) + \int_0^{\Delta T} e^{A(\Delta T - \tau)} Bu(\tau) d\tau \tag{2}$$

It is to be noted that in the above equation V_{dC} is constant and I_0 is assumed to be known and constant. Also noting that capacitor voltage must be equal to zero at instant t_3, defining a row vector C as $C = \begin{bmatrix} 1 & 0 \end{bmatrix}$, we can write from (2)

$$0 = C\left[\phi x(t_2) + \theta u(t_2)\right] \tag{3}$$

where $\phi = e^{A\Delta T}$ and $\theta = \int_0^{\Delta T} e^{A(\Delta T - \tau)} B d\tau$. Note that since A, B and ΔT are known a priori, the matrices ϕ and θ can be numerically evaluated. The state plane trajectory under this boundary value problem is shown Fig. 5 where V_C is assumed to be approximately zero when S_0 is closed.

We can expand equation (3) as

$$0 = \begin{bmatrix}\phi_{11} & \phi_{12}\end{bmatrix} x(t_2) + \begin{bmatrix}\theta_{11} & \theta_{12}\end{bmatrix} u(t_2)$$

where the subscripts 11 and 12 indicate the particular elements of these matrices. Again from Fig. 4 we get $x^T(t_2) = \begin{bmatrix}0 & i_R(t_2)\end{bmatrix}$. Substituting in the above equation and rearranging we get

$$i_R(t_2) = -\frac{1}{\phi_{21}}\left[\theta_{11} I_0 + \theta_{21} V_{dc}\right] \qquad (4)$$

The above value of current at instant t_2 required to ensure zero crossing of the voltage at instant t_3. Once $i_R(t_2)$ is obtained the time for which the capacitor should be shorted. The computed value of current $i_R(t_2)$, obtained from equation (4), with the actual value link current i_R. The switch S_0 is opened when these two values are equal. This ensures that the link current is built up to the required level of initial current such that the link voltage goes to zero at instant t_3, i.e., at the end of next resonant cycle. A block schematic of the implementation scheme is shown in Fig. 6.

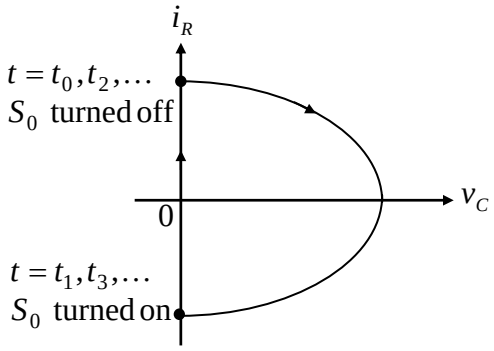

Fig. 5 State plane diagram of link voltage and current

A personal computer (PC) along with its associated high-speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are used for implementing the above scheme. The PC is used for the computation of the initial current from equation (4). In this equation θ_{11}, θ_{21} and ϕ_{21} are constants that are dependent on the circuit parameters and the time ΔT. These are pre-computed and stored. The load current (I_0) and the dc voltage are measured through Hall-effect sensors at the start of every resonant cycle (e.g. t_2) and are converted through ADC. These measured values along with the constants mentioned above are used for the computation of the initial current. This process is repeated for every resonant cycle. It is to be noted that the computation here is fairly simple and can also be achieved through a hardware configuration. However, the arrangement of introducing a PC makes the control circuit much more flexible than a hardwired circuit. Furthermore, due to the presence of the PC, the circuit delays can also be taken into account for an accurate zero-voltage switching.

As soon as the required initial current is computed in the PC, it is converted into an analogue signal through a DAC. The computation time required is much smaller than the resonant cycle time ΔT. This signal is then available to the comparator for comparison with the actual link current. The link current is monitored continuously through a Hall- effect current sensor. When the link current becomes equal to the required initial current, the comparator output becomes zero and the shorting switch is opened. The mono-stable is set for giving a pulse width of ΔT (oscillation period) after which the switch is shorted.

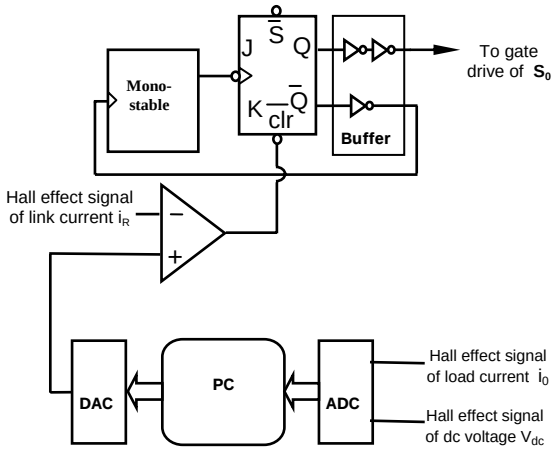

Fig. 6 Block diagram of current initialization

The time for which the link will be shorted will depend on the DAC pre-computed value and the actual current build up. When the link is shorted, the switching transition of switches $S_1 - S_4$ take place and ZVS is achieved.

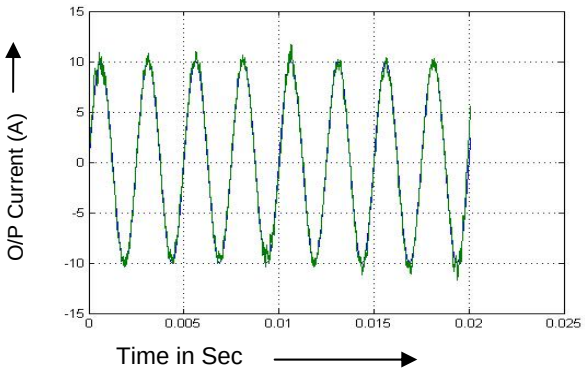

Fig. 7. Output Current Vs. Time

Parameters: L = 52mH, C = 0.89mF, V_{dc}= 400V
Load: R=0.2 Ohms, L=15mH, Voltage = 325sin(2512t)

V. ZERO HYSTERESIS CURRENT REGULATOR

A zero-hysteresis bang-bang control is used for current control of the inverter. however, the switching strategy in this case is somewhat different from a hard-switched pwm current regulated inverter as the switching in this case can only be done when the link voltage is zero. therefore instantaneous operation of appropriate switches when the error crosses the hysteresis band is precluded here. actual currents are compared with reference currents to generate these error signals. depending on the polarity of

these signals a switching decision is taken. for example, if the error signal of phase-a is positive, then the current through this phase has to be increased. this is done by turning on s_1 and simultaneously turning off switch s_4. similar switches in other phases are turned on or off depending on their requirements. since there is no notion of hysteresis band in this case, we will call this as zero-hysteresis bang-bang current control. fig. 7 shows the waveform of load current that is operating at 400 hz. it is clear that waveform is nearly sinusoidal and fft confirms that thd is 2.2 % which satisfies ieee specifications.

VI. CONCLUSION

A new current initialization scheme for resonant dc link inverter is proposed in this paper. This initialization scheme is based on boundary value problem. It is shown that that this current can be predicted very accurately which in turn ensures the zero-crossing of the link voltage at a prescribed time instant. The proposed power supply is subjected to support a 400 Hz load and the performance is found to be excellent in terms of quality and THD. The proposed scheme is validated through extensive simulation studies.

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